TEXAS INSTRUMENTS

SN74AHC595

ZHCSVI9N – MAY 1996 – REVISED JULY 2024

SN74AHC595 具有三态输出寄存器的 8 位移位寄存器

1 特性

- 工作范围：2V 至 5.5V V_{CC}
- 8 位串行输入、并行输出移位寄存器
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 网络交换机
- 电力基础设施
- LED 显示屏
- 服务器

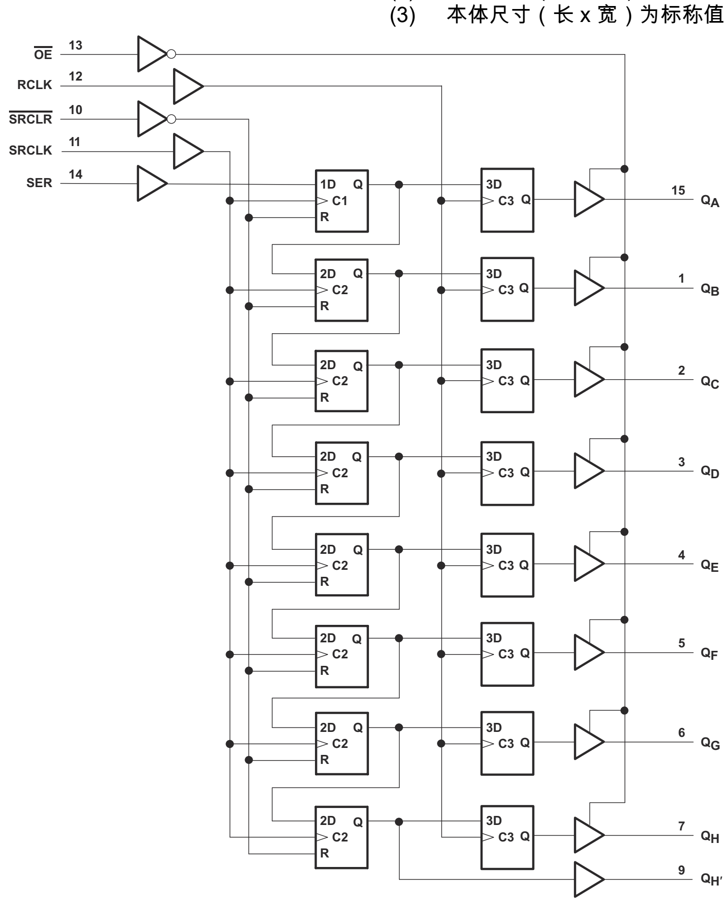
3 说明

SN74AHC595 器件包含一个可对 8 位 D 类存储寄存器进行馈送的 8 位串行输入、并行输出移位寄存器。存储寄存器具有并行三态输出。移位寄存器和存储寄存器各自具有独立时钟。移位寄存器具有直接覆盖清除 (SRCLR) 输入以及用于级联结构的串行 (SER) 输入和串行输出。当输出使能端 (OE) 输入为高电平时，所有输出（QH′ 除外）均处于高阻抗状态。

封装信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SN74AHC595	BQB（WQFN，16）	3.5mm x 2.5mm	3.5mm x 2.5mm
	N（PDIP，16）	19.31mm x 9.4mm	19.31mm x 6.35mm
	D（SOIC，16）	9.90mm x 6mm	9.90mm x 3.90mm
	DB（SSOP，16）	6.20mm x 7.8mm	6.20mm x 5.30mm
	PW（TSSOP，16）	5.00mm x 6.4mm	5.00mm x 4.40mm

(1) 如需了解更多信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 x 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

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4 Pin Configuration and Functions

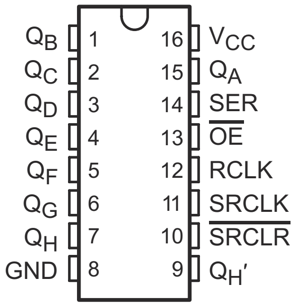


图 4-1. D, DB, N, PW Packages 16-Pin SOIC, SSOP, PDIP, TSSOP (Top View)

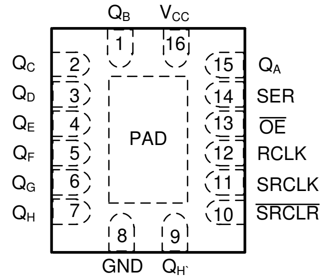


图 4-2. BQB Package, 16-Pin WQFN (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	—	Ground Pin
$\overline{OE}$	13	I	Output Enable
Q_A	15	O	Q_A Output
Q_B	1	O	Q_B Output
Q_C	2	O	Q_C Output
Q_D	3	O	Q_D Output
Q_E	4	O	Q_E Output
Q_F	5	O	Q_F Output
Q_G	6	O	Q_G Output
Q_H	7	O	Q_H Output
$Q_{H'}$	9	O	$Q_{H'}$ Output
RCLK	12	I	RCLK Input
SER	14	I	SER Input
SRCLK	11	I	SRCLK Input
$\overline{SRCLR}$	10	I	$\overline{SRCLR}$ Input
V_{CC}	16	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage[(2)]		–0.5	7	V
V_O	Output voltage[(2)]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2		5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 3 V	2.1			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level Input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 3 V			0.9	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		5.5	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V			–50	µA
		V_{CC} = 3.3 V ± 0.3 V			–4	mA
		V_{CC} = 5 V ± 0.5 V			–8	
I_{OL}	Low-level output current	V_{CC} = 2 V			50	µA
		V_{CC} = 3.3 V ± 0.3 V			4	mA
		V_{CC} = 5 V ± 0.5 V			8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V			100	ns/V
		V_{CC} = 5 V ± 0.5 V			20	

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		SN74AHC595					UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.8	93.8	97.8	47.8	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.7	54.7	48.1	35.1	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.6	50.9	48.5	27.8	81.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.9	20.8	10.0	20.1	22.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.4	50.7	47.9	27.7	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	39.4	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) [1]

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	T_A = 25°C	2 V	1.9	2		V
		T_A = –40°C to 85°C		1.9			
		T_A = –40°C to 125°C Recommended		1.9			
	I_{OH} = –50 µA	T_A = 25°C	3 V	2.9	3		
		T_A = –40°C to 85°C		2.9			
		T_A = –40°C to 125°C Recommended		2.9			
	I_{OH} = –50 µA	T_A = 25°C	4.5 V	4.4	4.5		
		T_A = –40°C to 85°C		4.4			
		T_A = –40°C to 125°C Recommended		4.4			
	I_{OH} = –4 mA	T_A = 25°C	3 V	2.58			
		T_A = –40°C to 85°C		2.48			
		T_A = –40°C to 125°C Recommended		2.48			
	I_{OH} = –8 mA	T_A = 25°C	4.5 V	3.94			
		T_A = –40°C to 85°C		3.8			
		T_A = –40°C to 125°C Recommended		3.8			

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS			V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL} = 50 µA	T_A = 25°C		2 V			0.1	V
		T_A = –40°C to 85°C					0.1	
		T_A = –40°C to 125°C Recommended					0.1	
	I_{OL} = 50 µA	T_A = 25°C		3 V			0.1	
		T_A = –40°C to 85°C					0.1	
		T_A = –40°C to 125°C Recommended					0.1	
	I_{OL} = 50 µA	T_A = 25°C		4.5 V			0.1	
		T_A = –40°C to 85°C					0.1	
		T_A = –40°C to 125°C Recommended					0.1	
	I_{OL} = 4 mA	T_A = 25°C		3 V			0.36	
		T_A = –40°C to 85°C					0.44	
		T_A = –40°C to 125°C Recommended					0.44	
	I_{OL} = 8 mA	T_A = 25°C		4.5 V			0.36	
		T_A = –40°C to 85°C					0.44	
		T_A = –40°C to 125°C Recommended					0.44	
I_I	V_I = 5.5 V or GND	T_A = 25°C		0 V to 5.5 V			±0.1	µA
		T_A = –40°C to 85°C					±1	
		T_A = –40°C to 125°C Recommended					±1	
I_{OZ}	V_I = V_{CC} or GND, V_O = V_{CC} or GND, $\overline{OE}$ = V_{IH} or V_{IL},	$Q_A – Q_H$	T_A = 25°C	5.5 V			±0.25	µA
			T_A = –40°C to 85°C				±2.5	
			T_A = –40°C to 125°C Recommended				±2.5	
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	T_A = 25°C	5.5 V			4	µA
			T_A = –40°C to 85°C				40	
			T_A = –40°C to 125°C Recommended				40	
C_i	V_I = V_{CC} or GND	T_A = 25°C		5 V		3	10	pF
		T_A = –40°C TO 85°C					10	
C_O	V_O = V_{CC} or GND,	T_A = 25°C		5 V		5.5		pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Timing Requirements: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
t_W	Pulse duration	SRCLK high or low	T_A = 25°C	5		ns
			T_A = –40°C to 85°C	5		
			T_A = –40°C to 125°C Recommended	6		
		RCLK high or low	T_A = 25°C	5		
			T_A = –40°C to 85°C	5		
			T_A = –40°C to 125°C Recommended	6		
		$\overline{SRCLR}$ low	T_A = 25°C	5		
			T_A = –40°C to 85°C	5		
			T_A = –40°C to 125°C Recommended	6.5		

over recommended operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
t_{su}	Set-up time	SER before SRCLK↑	T_A = 25°C	3.5		ns
			T_A = –40°C to 85°C	3.5		
			T_A = –40°C to 125°C Recommended	4.5		
		SRCLK↑ before RCLK↑[(1)]	T_A = 25°C	8		
			T_A = –40°C to 85°C	8.5		
			T_A = –40°C to 125°C Recommended	9.5		
		$\overline{SRCLR}$ low before RCLK↑	T_A = 25°C	8		
			T_A = –40°C to 85°C	9		
			T_A = –40°C to 125°C Recommended	10		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	T_A = 25°C	3		
			T_A = –40°C to 85°C	3		
			T_A = –40°C to 125°C Recommended	4		
t_h	Hold time	SER after SRCLK↑	T_A = 25°C	1.5		ns
			T_A = –40°C to 85°C	1.5		
			T_A = –40°C to 125°C Recommended	2.5		

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.7 Timing Requirements: V_{CC} = 5 V ± 0.5 V

				MIN	NOM	MAX	UNIT
t_W	Pulse duration	SRCLK high or low	T_A = 25°C	5			ns
			T_A = –40°C to 85°C	5			
			T_A = –40°C to 125°C Recommended	6			
		RCLK high or low	T_A = 25°C	5			
			T_A = –40°C to 85°C	5			
			T_A = –40°C to 125°C Recommended	6			
		$\overline{SRCLR}$ low	T_A = 25°C	5			
			T_A = –40°C to 85°C	5			
			T_A = –40°C to 125°C Recommended	6.2			
t_{su}	Set-up time	SER before SRCLK↑	T_A = 25°C	3			ns
			T_A = –40°C to 85°C	3			
			T_A = –40°C to 125°C Recommended	4			
		SRCLK↑ before RCLK↑[(1)]	T_A = 25°C	5			
			T_A = –40°C to 85°C	5			
			T_A = –40°C to 125°C Recommended	6			
		$\overline{SRCLR}$ low before RCLK↑	T_A = 25°C	5			
			T_A = –40°C to 85°C	5			
			T_A = –40°C to 125°C Recommended	6			
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	T_A = 25°C	2.5			
			T_A = –40°C to 85°C	2.5			
			T_A = –40°C to 125°C Recommended	3.5			
t_h	Hold time	SER after SRCLK↑	T_A = 25°C	2			ns
			T_A = –40°C to 85°C	2			
			T_A = –40°C to 125°C Recommended	3			

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

5.8 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF	T_A = 25°C	80(1)	120(1)		MHz
				T_A = –40°C to 85°C	70			
				T_A = –40°C to 125°C Recommended	60			
			C_L = 50 pF	T_A = 25°C	55	105		
				T_A = –40°C to 85°C	50			
				T_A = –40°C to 125°C Recommended	40			
t_{PLH}	RCLK	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		6(1)	11.9(1)	ns
				T_A = –40°C to 85°C	1		13.5	
				T_A = –40°C to 125°C Recommended	1		14.9	
t_{PHL}	RCLK	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		6(1)	11.9(1)	ns
				T_A = –40°C to 85°C	1		13.5	
				T_A = –40°C to 125°C Recommended	1		14.9	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		6.6(1)	13(1)	ns
				T_A = –40°C to 85°C	1		15	
				T_A = –40°C to 125°C Recommended	1		16.4	
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		6.6(1)	13(1)	ns
				T_A = –40°C to 85°C	1		15	
				T_A = –40°C to 125°C Recommended	1		16.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		6.2(1)	12.8(1)	ns
				T_A = –40°C to 85°C	1		13.7	
				T_A = –40°C to 125°C Recommended	1		15	
t_{PZH}	$\overline{OE}$	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		6(1)	11.5(1)	ns
				T_A = –40°C to 85°C	1		13.5	
				T_A = –40°C to 125°C Recommended	1		14.9	
t_{PZL}	$\overline{OE}$	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		7.8(1)	11.5(1)	ns
				T_A = –40°C to 85°C	1		13.5	
				T_A = –40°C to 125°C Recommended	1		14.9	
t_{PLH}	RCLK	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		7.9	15.4	ns
				T_A = –40°C to 85°C	1		17	
				T_A = –40°C to 125°C Recommended	1		18.6	
t_{PHL}	RCLK	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		7.9	15.4	ns
				T_A = –40°C to 85°C	1		17	
				T_A = –40°C to 125°C Recommended	1		18.6	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		9.2	16.5	ns
				T_A = –40°C to 85°C	1		18.5	
				T_A = –40°C to 125°C Recommended	1		20	
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		9.2	16.5	ns
				T_A = –40°C to 85°C	1		18.5	
				T_A = –40°C to 125°C Recommended	1		20	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		9	16.3	ns
				T_A = –40°C to 85°C	1		17.2	
				T_A = –40°C to 125°C Recommended	1		18.7	
t_{PZH}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		7.8	15	ns
				T_A = –40°C to 85°C	1		17	
				T_A = –40°C to 125°C Recommended	1		18.6	

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PZL}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		9.6	15	ns
				T_A = –40°C to 85°C	1		17	
				T_A = –40°C to 125°C Recommended	1		18.6	
t_{PHZ}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		8.1	15.7	ns
				T_A = –40°C to 85°C	1		16.2	
				T_A = –40°C to 125°C Recommended	1		17.4	
t_{PLZ}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		9.3	15.7	ns
				T_A = –40°C to 85°C	1		16.2	
				T_A = –40°C to 125°C Recommended	1		17.4	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.9 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF	T_A = 25°C	135[(1)]	170[(1)]		MHz
				T_A = –40°C to 85°C	115			
			C_L = 50 pF	T_A = 25°C	95	140		
				T_A = –40°C to 85°C	85			
t_{PLH}	RCLK	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		4.3[(1)]	7.4[(1)]	ns
				T_A = –40°C to 85°C	1		8.5	
t_{PHL}	RCLK	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		4.3[(1)]	7.4[(1)]	ns
				T_A = –40°C to 85°C	1		8.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		4.5[(1)]	8.2[(1)]	ns
				T_A = –40°C to 85°C	1		9.4	
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		4.5[(1)]	8.2[(1)]	ns
				T_A = –40°C to 85°C	1		9.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 15 pF	T_A = 25°C		4.5[(1)]	8[(1)]	ns
				T_A = –40°C to 85°C	1		9.1	
t_{PZH}	$\overline{OE}$	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		4.3[(1)]	8.6[(1)]	ns
				T_A = –40°C to 85°C	1		10	
t_{PZL}	$\overline{OE}$	$Q_A – Q_H$	C_L = 15 pF	T_A = 25°C		5.4[(1)]	8.6[(1)]	ns
				T_A = –40°C to 85°C	1		10	
t_{PLH}	RCLK	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		5.6	9.4	ns
				T_A = –40°C to 85°C	1		10.5	
t_{PHL}	RCLK	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		5.6	9.4	ns
				T_A = –40°C to 85°C	1		10.5	
t_{PLH}	SRCLK	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		6.4	10.2	ns
				T_A = –40°C to 85°C	1		11.4	
t_{PHL}	SRCLK	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		6.4	10.2	ns
				T_A = –40°C to 85°C	1		11.4	
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	C_L = 50 pF	T_A = 25°C		6.4	10	ns
				T_A = –40°C to 85°C	1		11.1	
t_{PZH}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		5.7	10.6	ns
				T_A = –40°C to 85°C	1		12	
t_{PZL}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		6.8	10.6	ns
				T_A = –40°C to 85°C	1		12	
t_{PHZ}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		3.5	10.3	ns
				T_A = –40°C to 85°C	1		11	
t_{PLZ}	$\overline{OE}$	$Q_A – Q_H$	C_L = 50 pF	T_A = 25°C		3.4	10.3	ns
				T_A = –40°C to 85°C	1		11	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

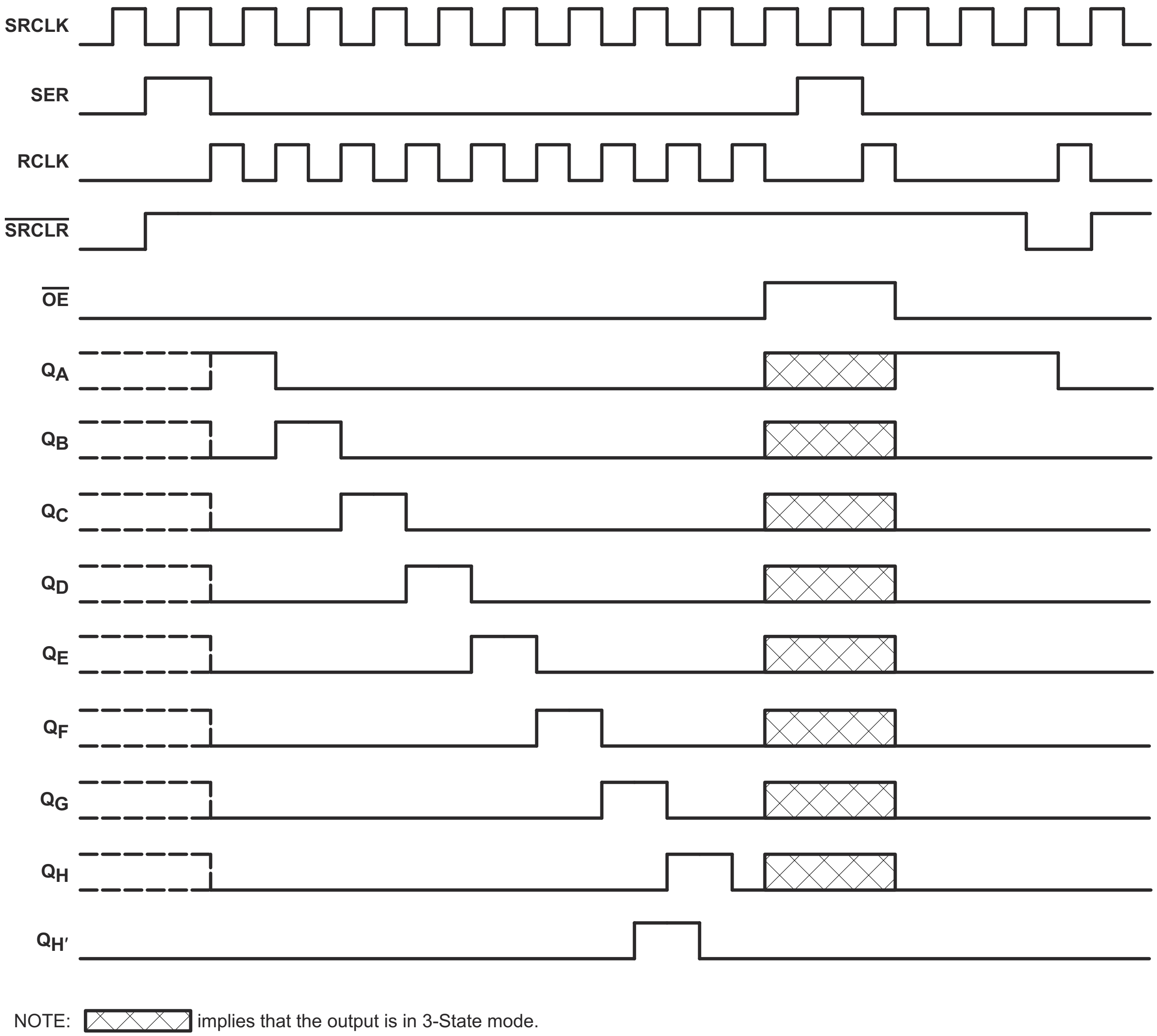


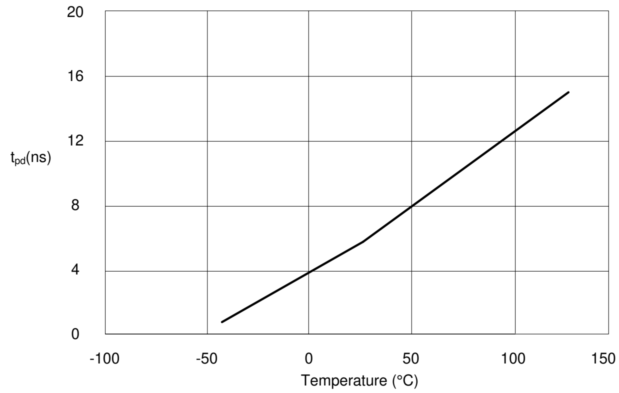
图 5-1. Timing Diagram

5.10 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	25.2	pF

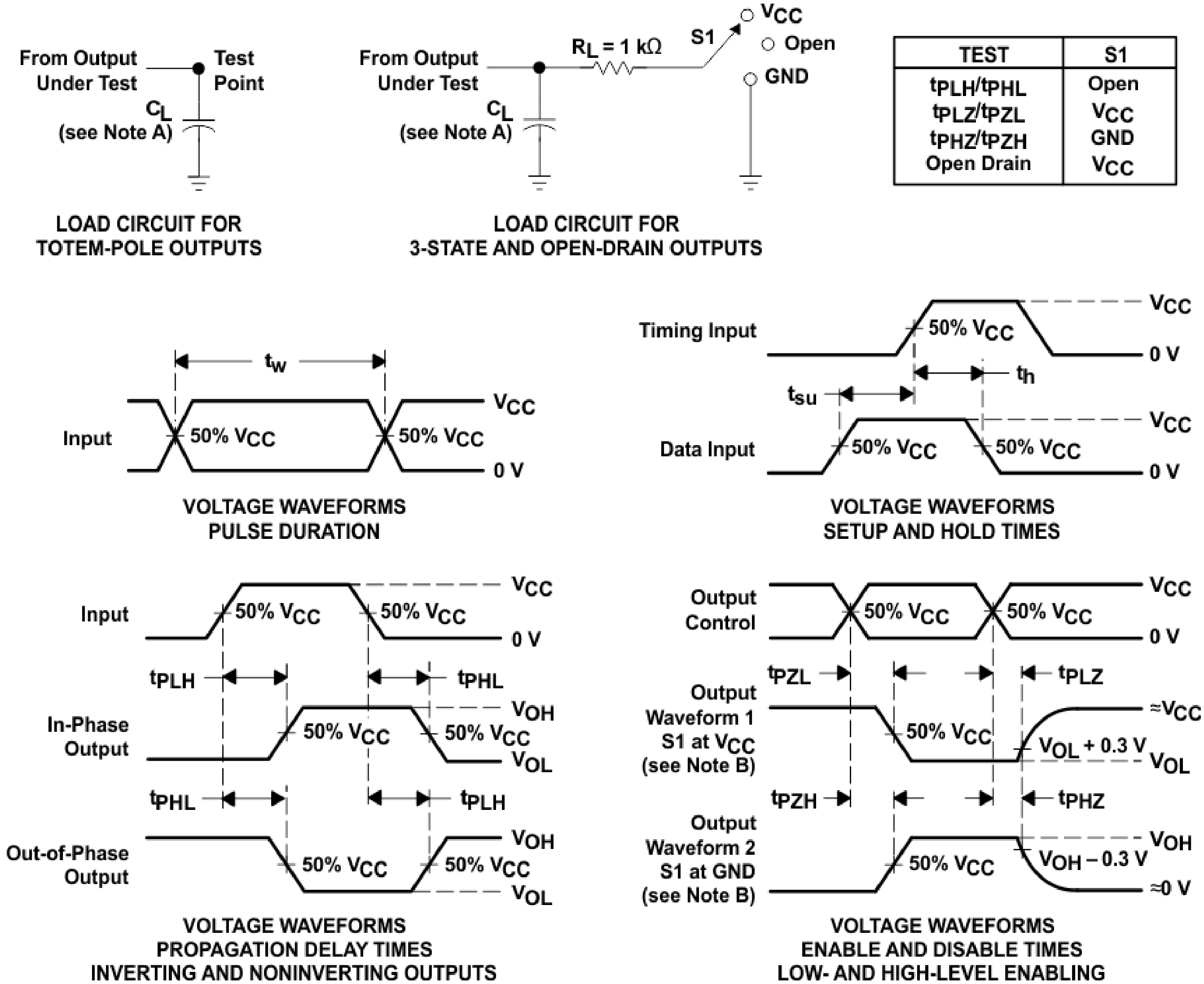
5.11 Typical Characteristics



V_{CC} = 3.3 V　　15-pF Load

图 5-2. SN74AHC595 RCLK to Q TPD vs Temperature

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

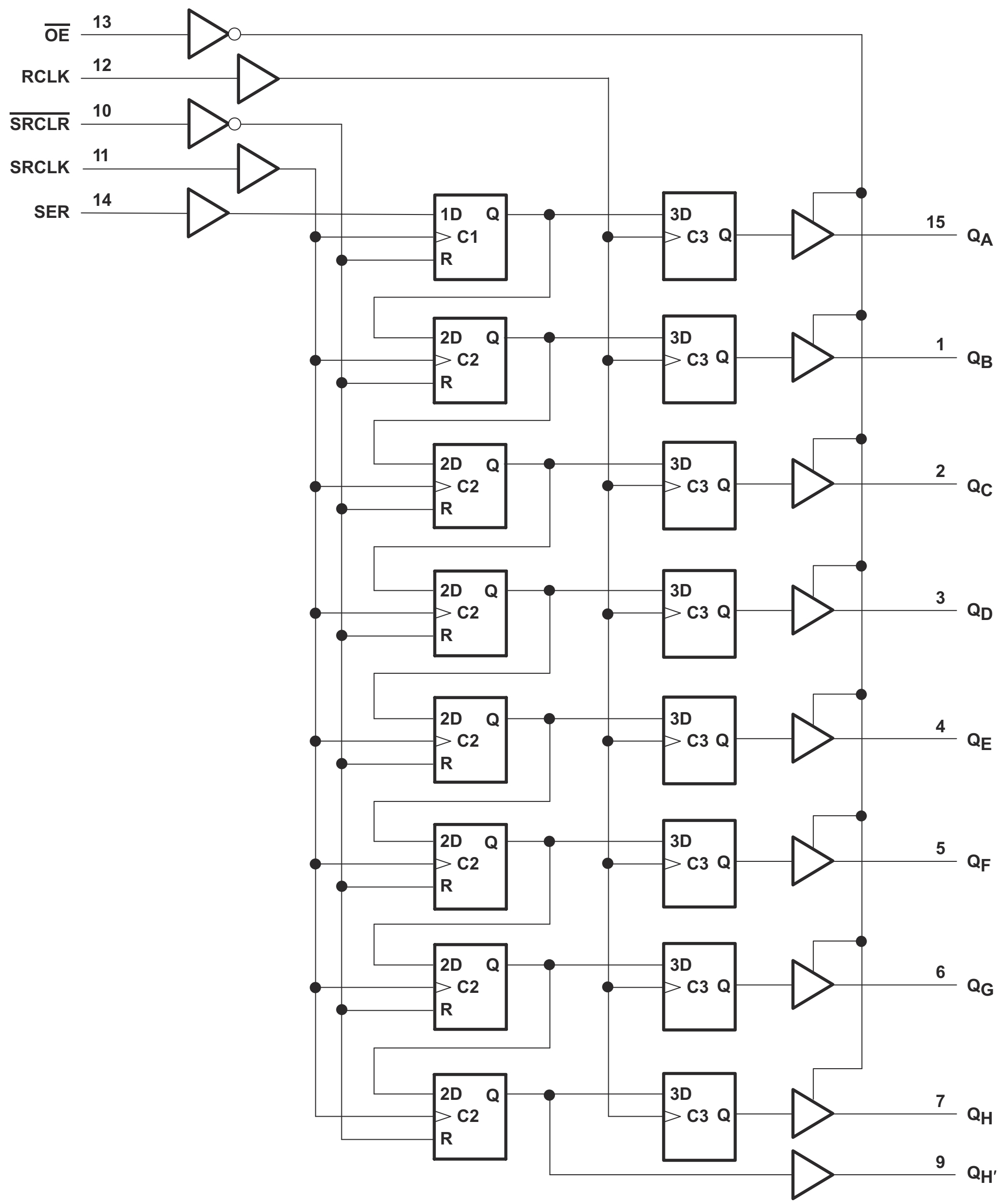
7 Detailed Description

7.1 Overview

The SN74AHC595 device is part of the AHC family of logic devices intended for CMOS applications. The SN74HC595 device is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74AHC595 device is an 8-bit serial-in, parallel-out shift registers that have a wide operating voltage range from 2 V to 5.5 V and a low current consumption of 40-μA (max) I_{CC}.

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A–Q_H are disabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AHC595 device is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. 图 8-1 shows an application where eight LEDs are used to visualize the data bits contained within the shift register.

8.2 Typical Application

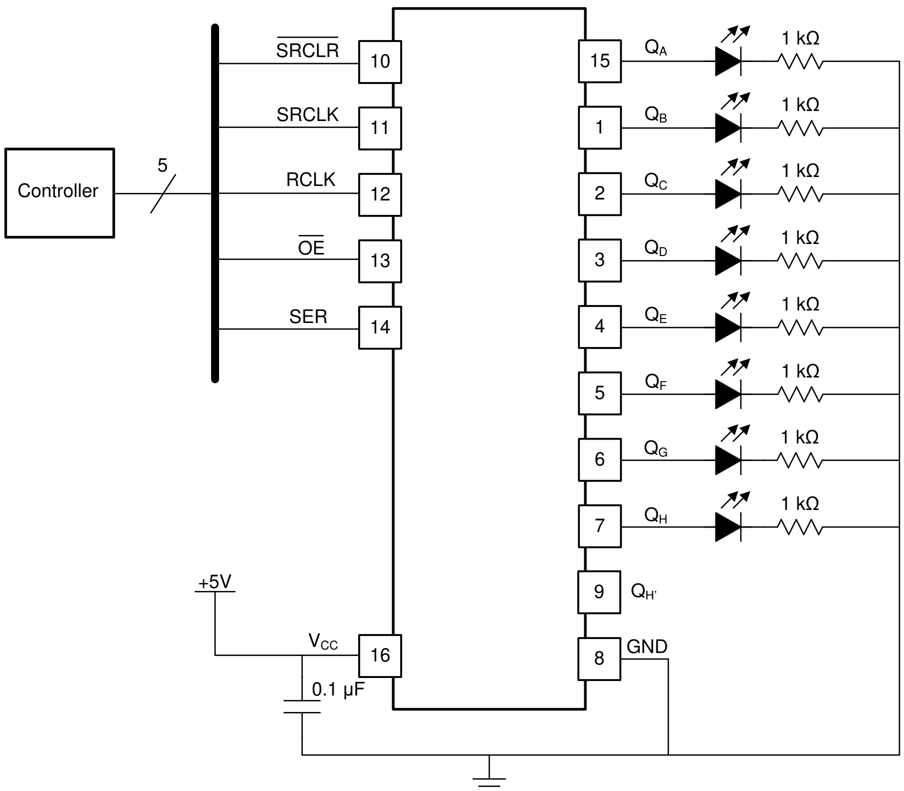


图 8-1. Shift Register Display of 8 bits

8.2.1 Design Requirements

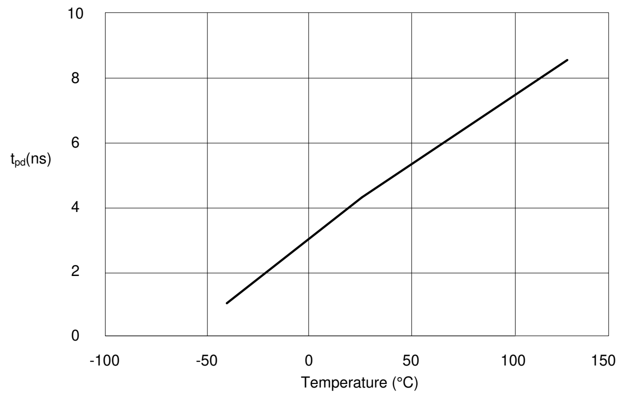
This device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 6.0 V at any valid V_{CC}
- Recommend output conditions:
  - Load currents must not exceed 25 mA per output and 75 mA total for the part

– Outputs must not be pulled above V_{CC}

8.2.3 Application Curve



V_{CC} = 5 V 15-pF Load

图 8-2. SN74AHC595 RCLK to Q TPD vs Temperature

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply-voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1-µf capacitor is recommended; if there are multiple V_{CC} pins, then a 0.01-µf or a 0.022-µf capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µf and a 1-µf capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must **not** be left unconnected because the undefined voltages at the outside connections results in undefined operational states. 图 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, these unused inputs will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output-enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8.4.2 Layout Example

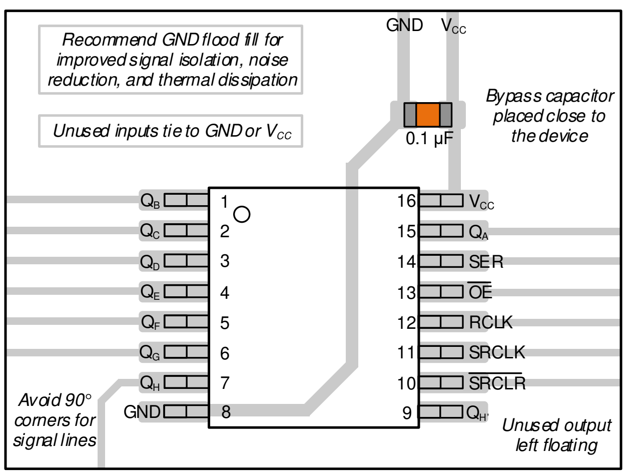


图 8-3. Example Layout for the SN74AHC595

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, wee the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (April 2024) to Revision N (July 2024) — **Page**

- Updated RθJA value: D = 73 to 93.8, all values in °C/W 5

Changes from Revision L (March 2024) to Revision M (April 2024) — **Page**

- Updated thermal values for PW package from RθJA = 106.1 to 135.9, RθJC(top) = 40.8 to 70.3, RθJB = 51.1 to 81.3, ΨJT = 3.8 to 22.5, ΨJB = 50.6 to 80.8, all values in °C/W.......... 5
- Added *Typical Characteristics* 12
- Updated *Layout Example* 18

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC595BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC595
SN74AHC595BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC595
SN74AHC595D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	AHC595
SN74AHC595DBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595
SN74AHC595DBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595
SN74AHC595DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC595
SN74AHC595DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC595
SN74AHC595N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC595N
SN74AHC595N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC595N
SN74AHC595PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 125	HA595
SN74AHC595PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA595
SN74AHC595PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595
SN74AHC595PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595
SN74AHC595PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC595 :

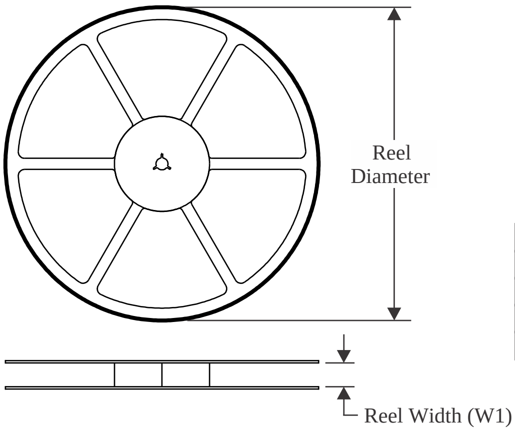
- Automotive : SN74AHC595-Q1

NOTE: Qualified Version Definitions:

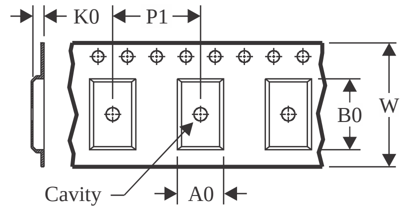
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

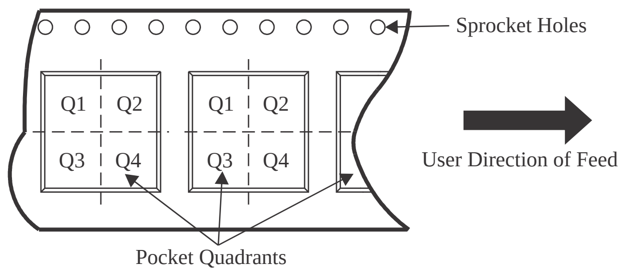


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

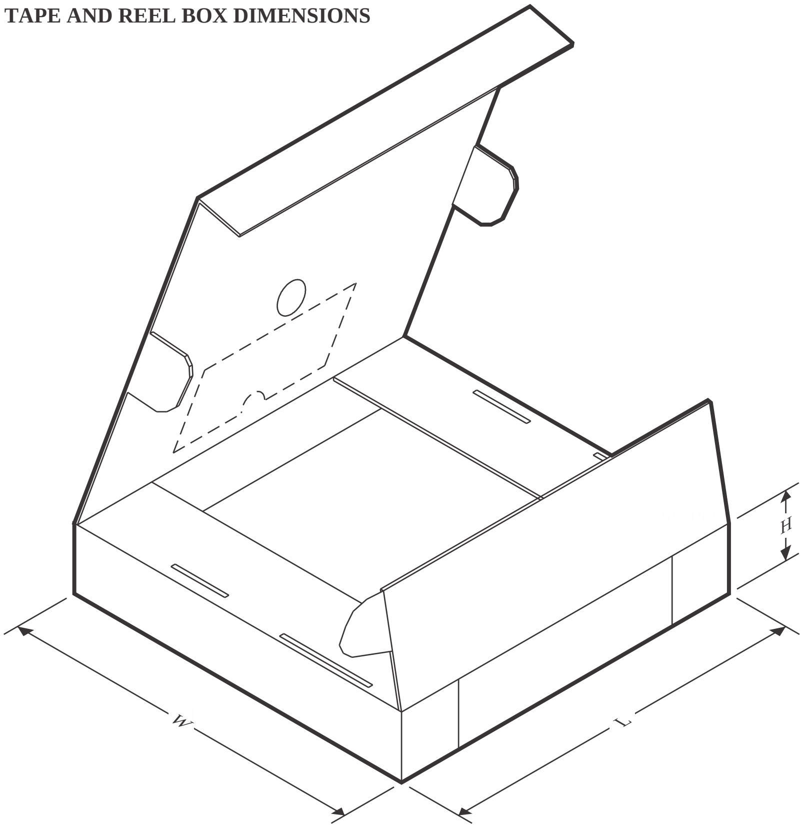
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC595BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AHC595DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC595DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC595PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

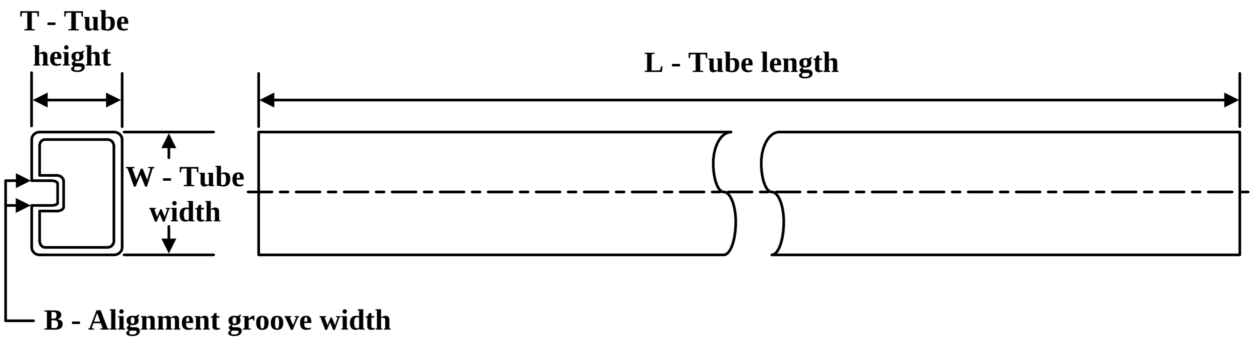
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC595BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AHC595DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHC595DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHC595DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC595PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC595PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHC595PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AHC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC595N.A	N	PDIP	16	25	506	13.97	11230	4.32

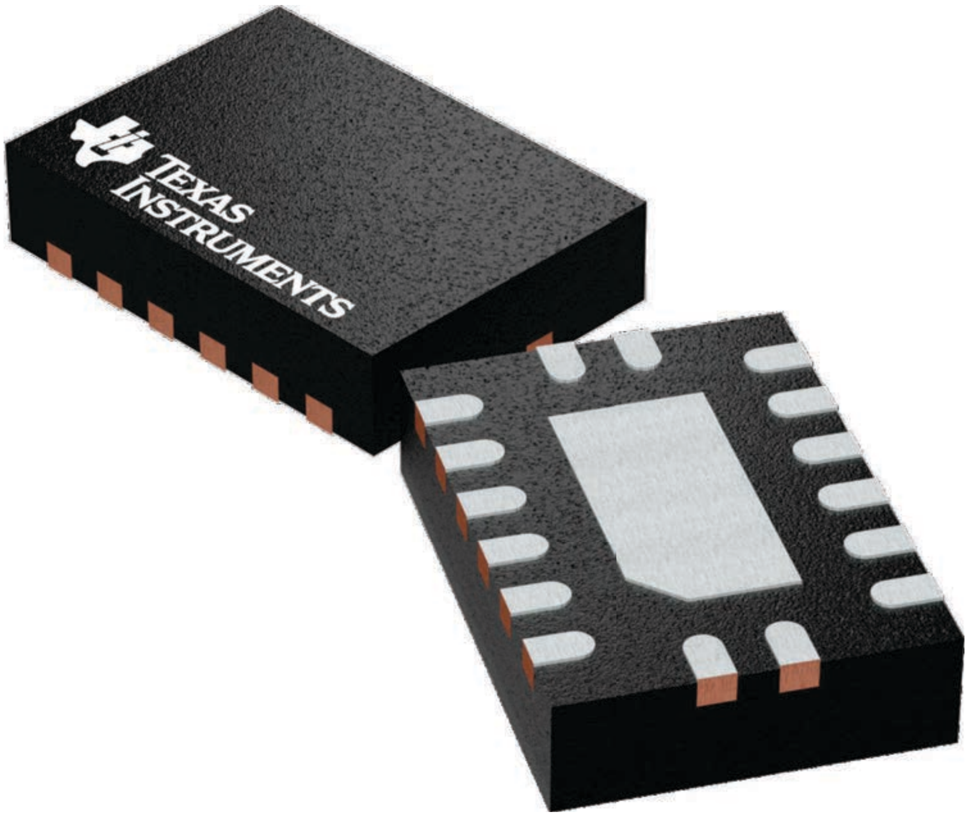
BQB 16

WQFN - 0.8 mm max height

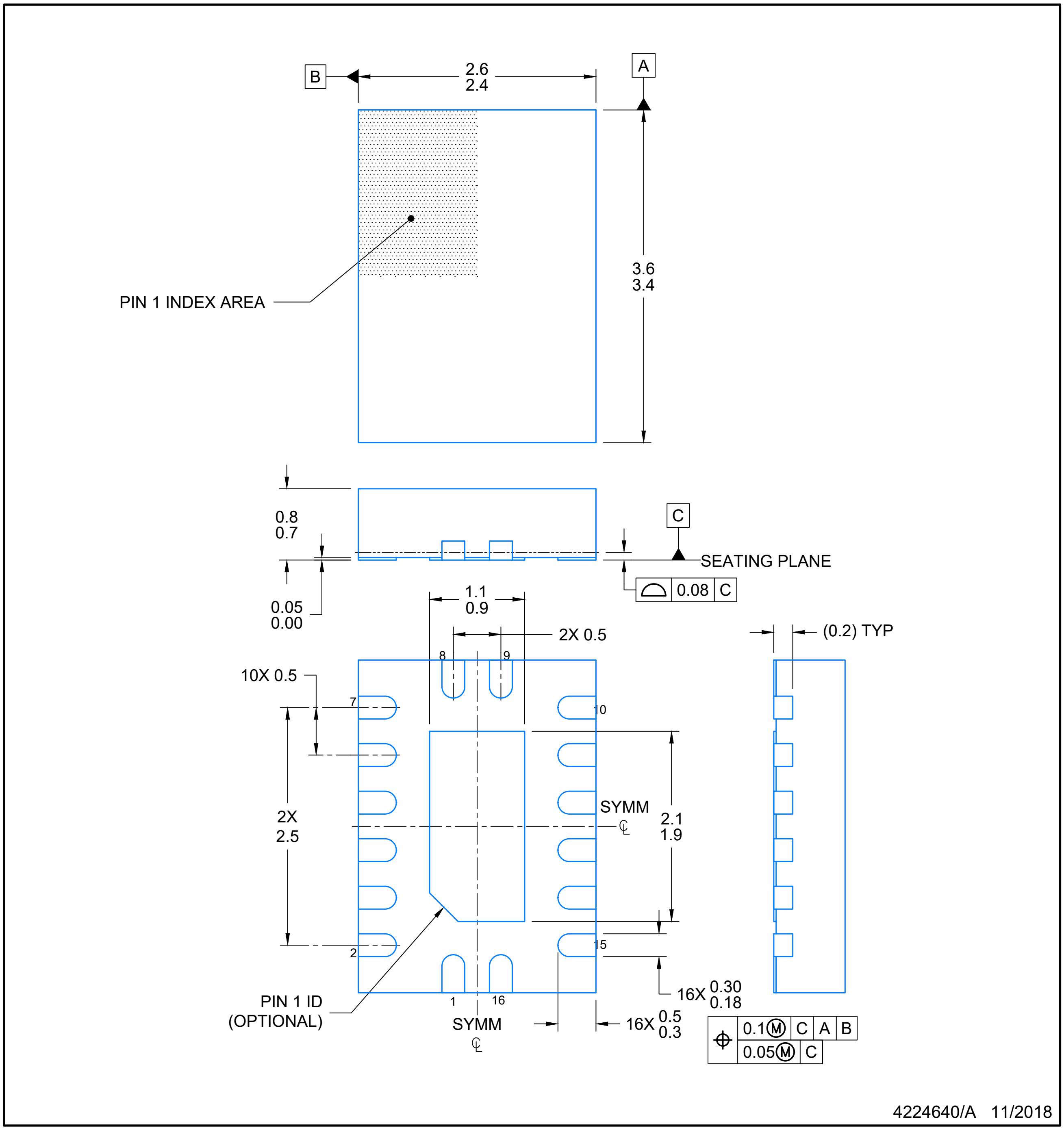
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

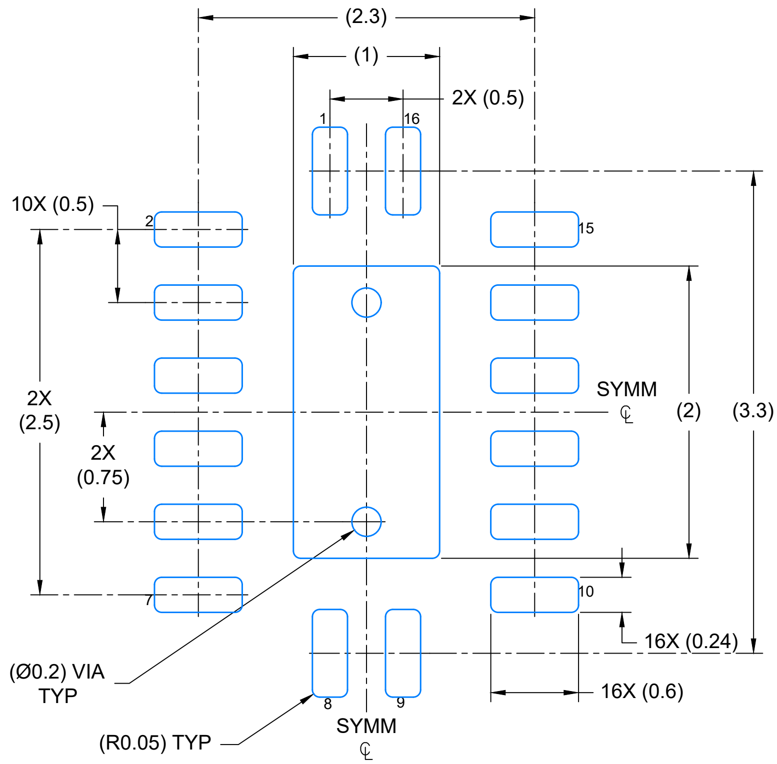


4226161/A

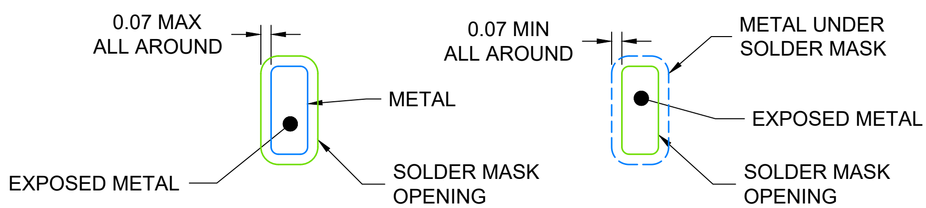


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



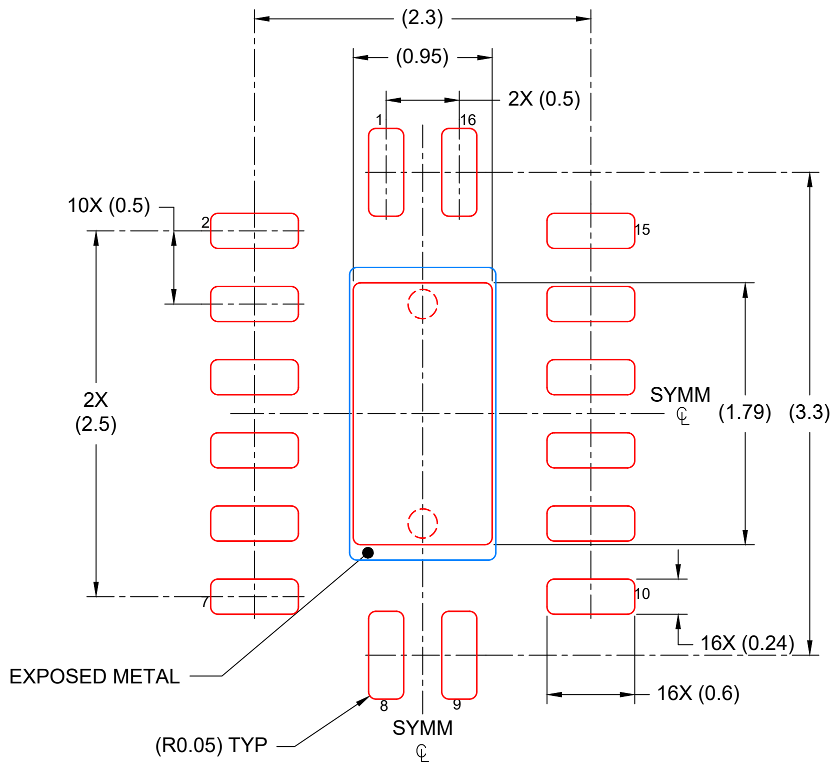
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



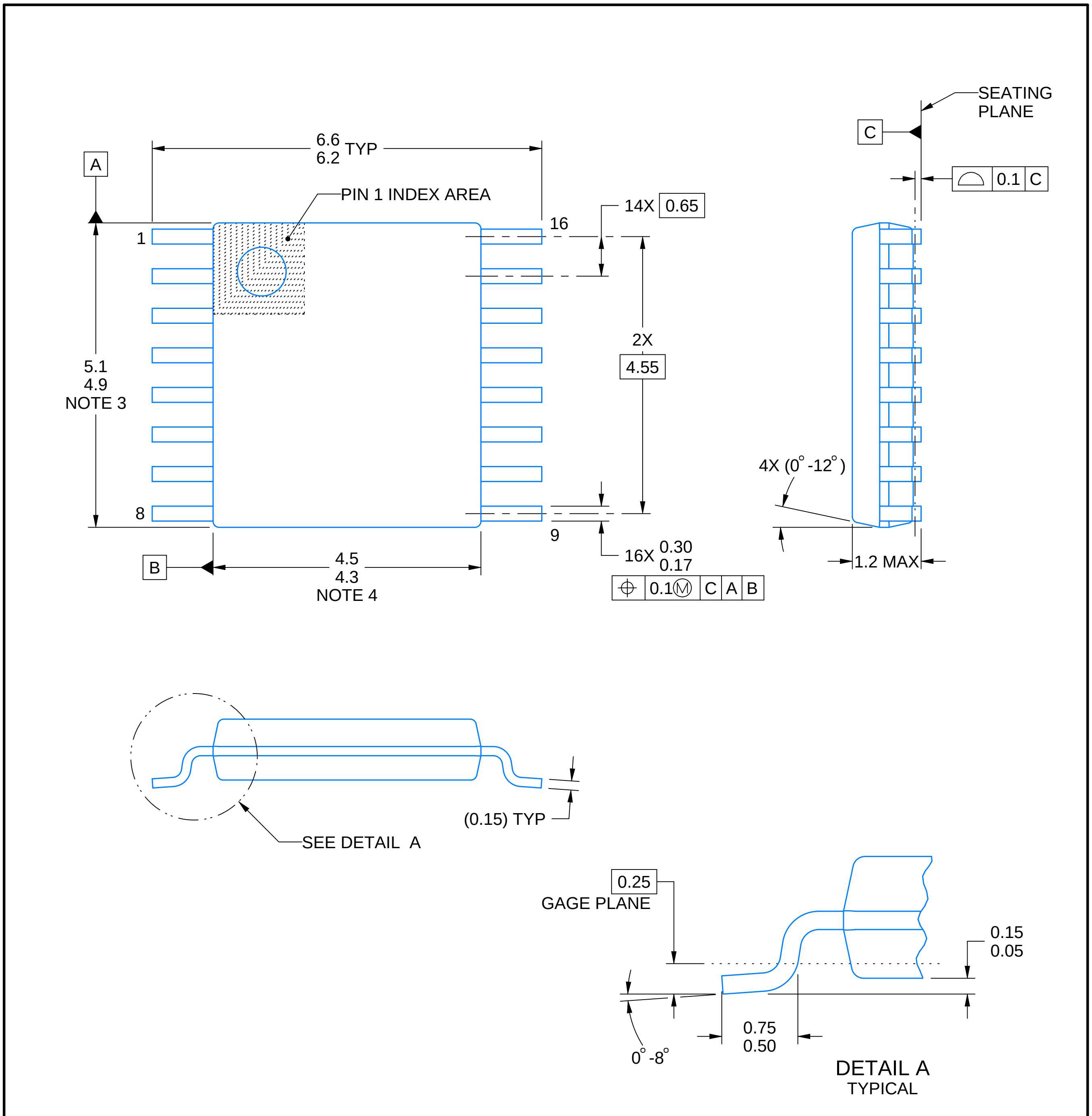
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

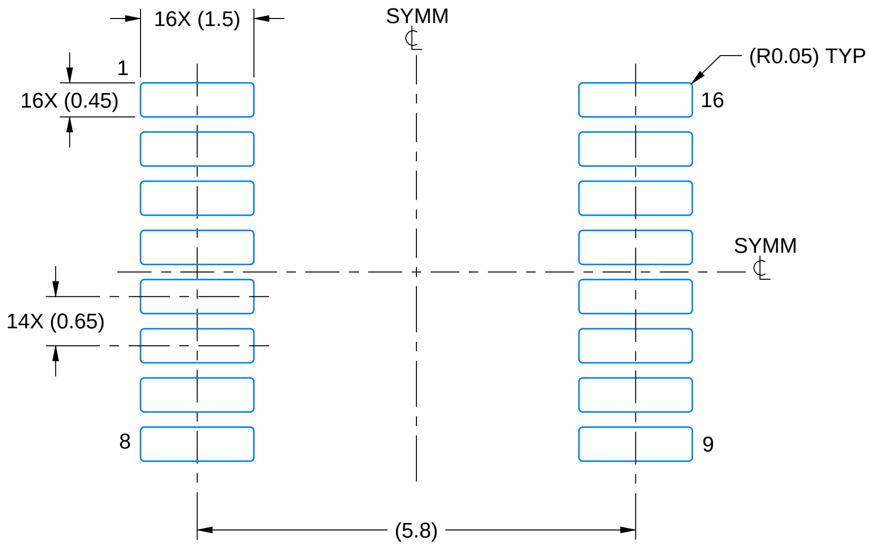
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



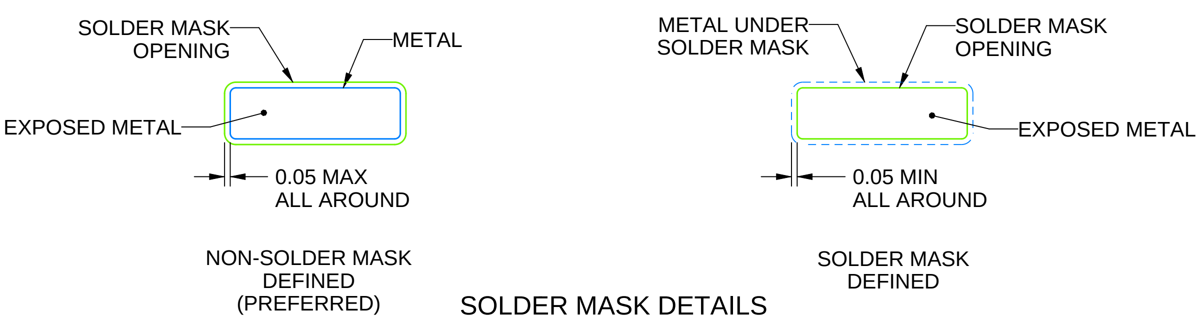
4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

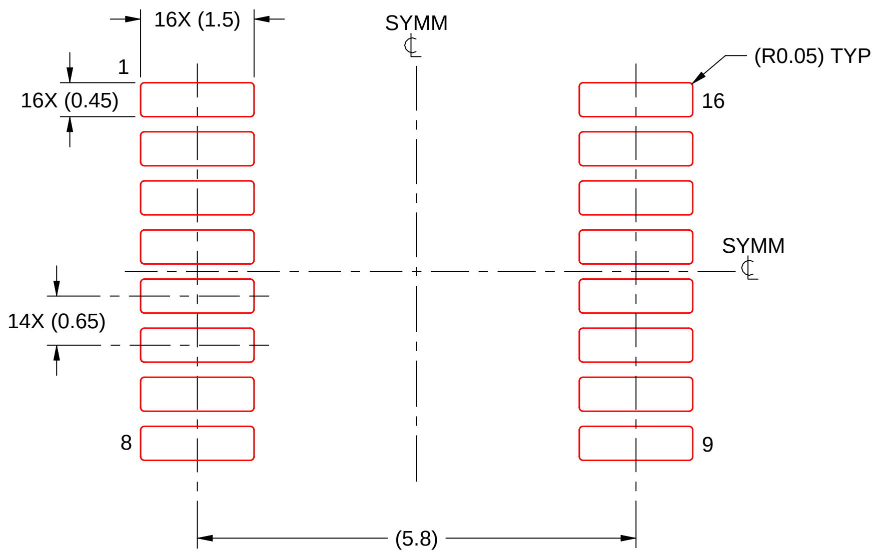


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

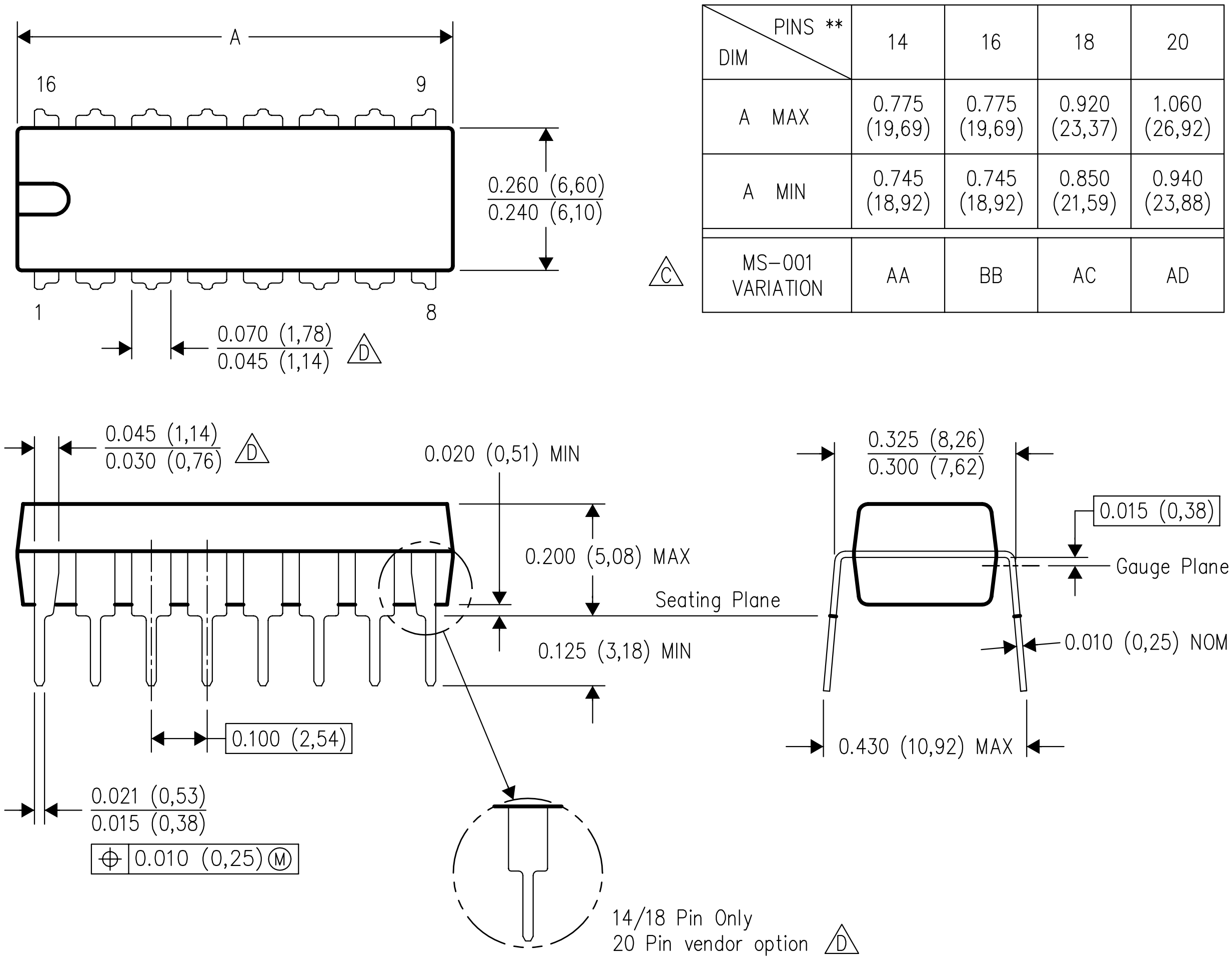
4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

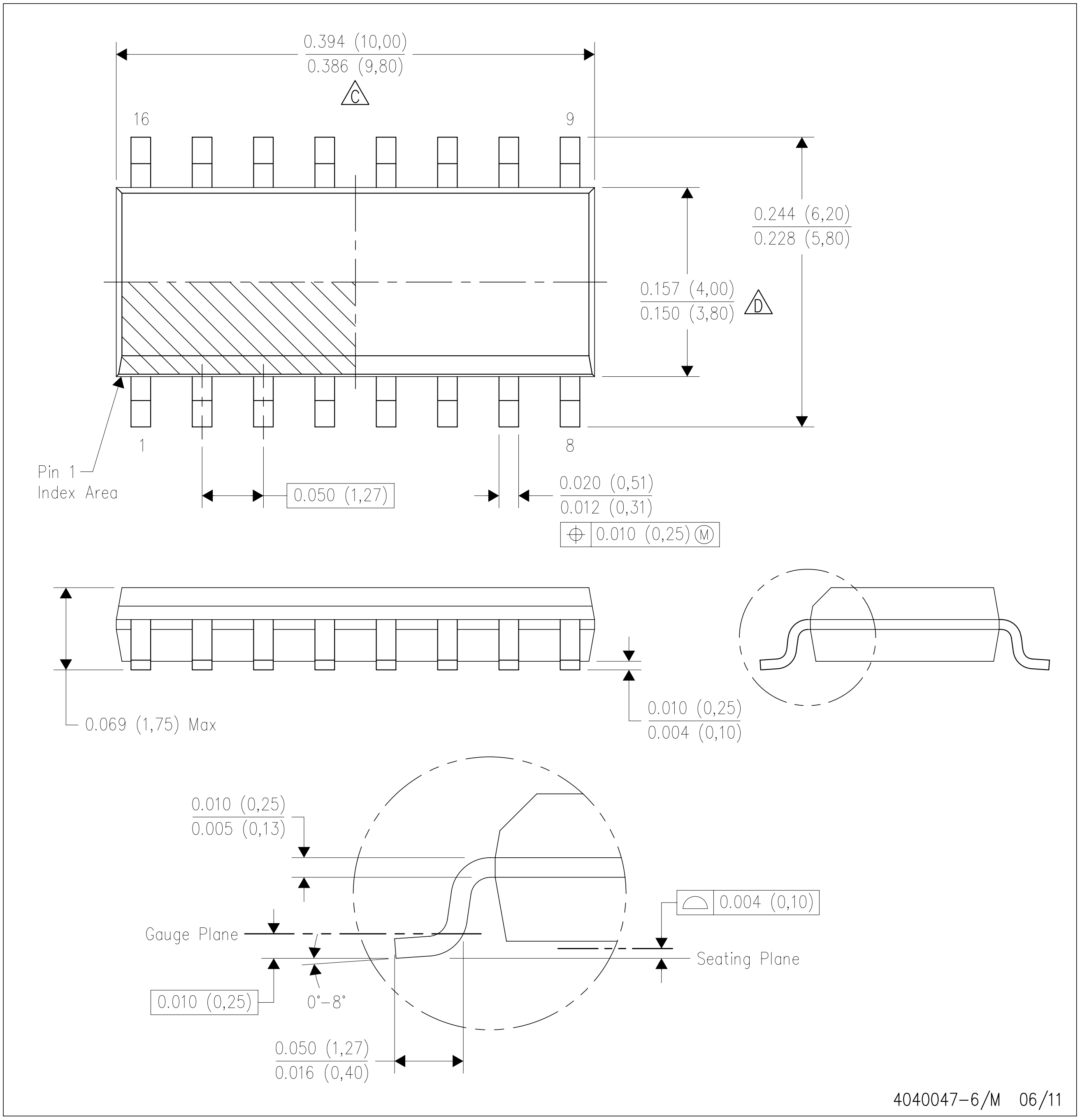


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD

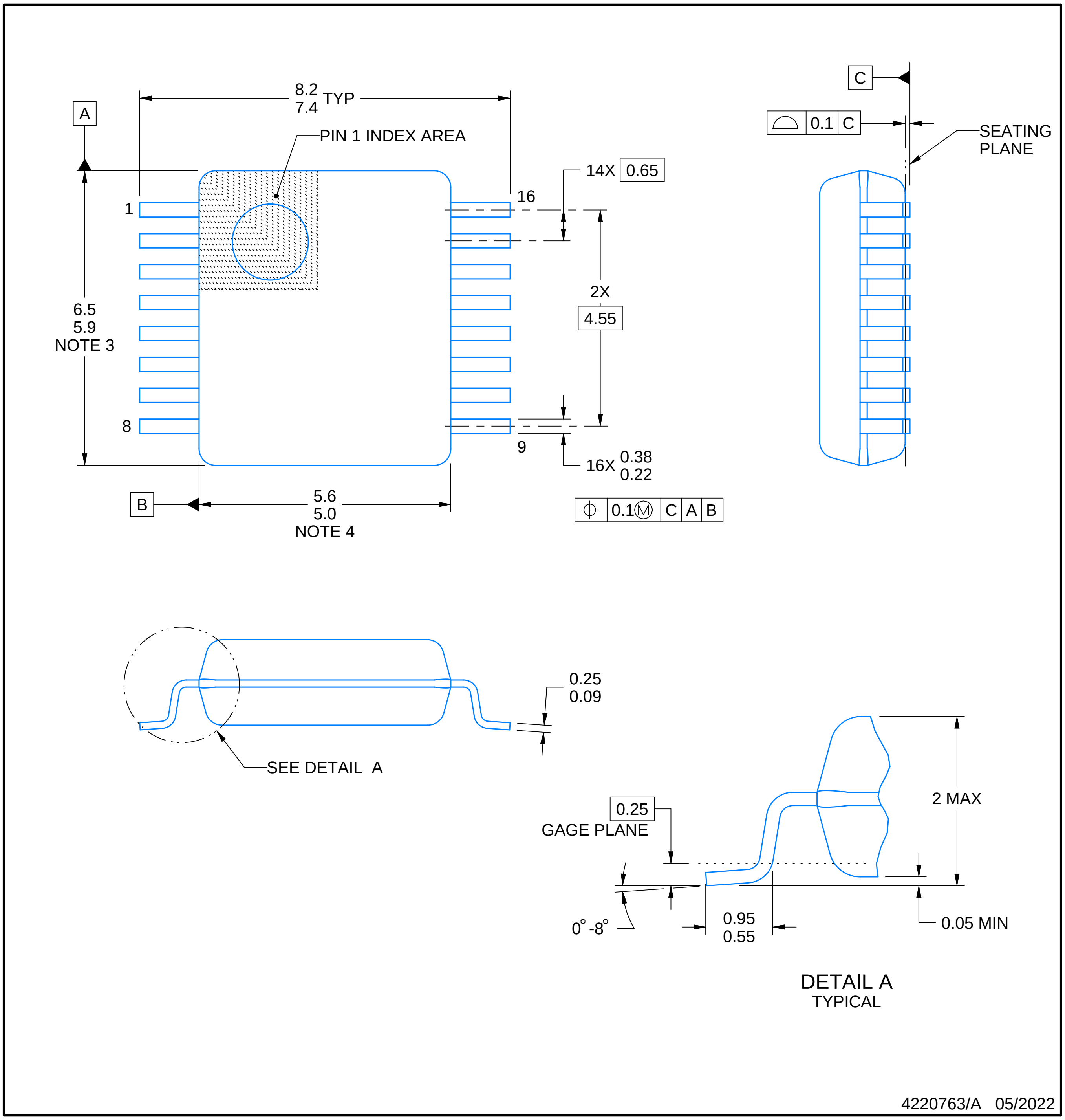
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE

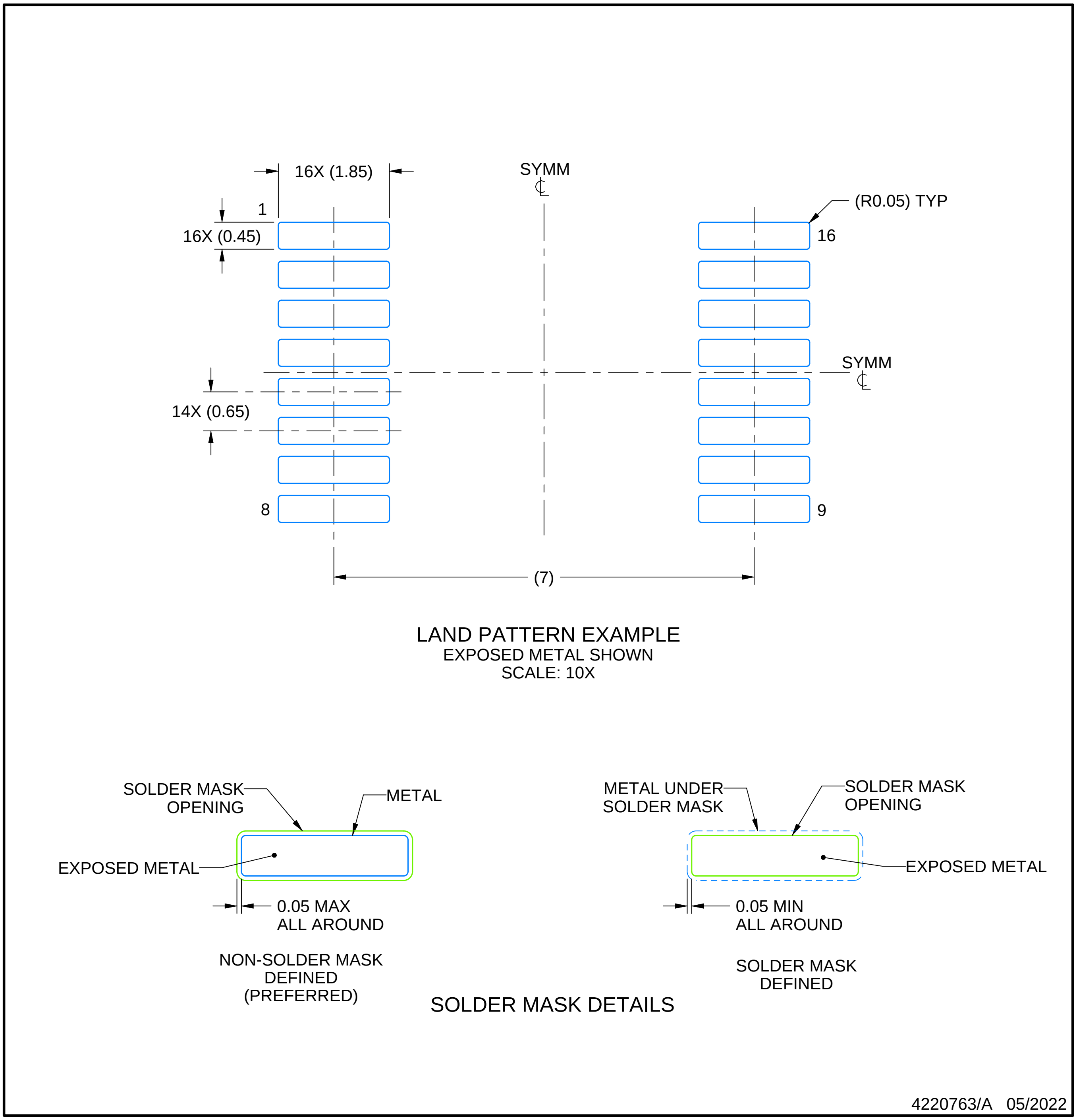


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.



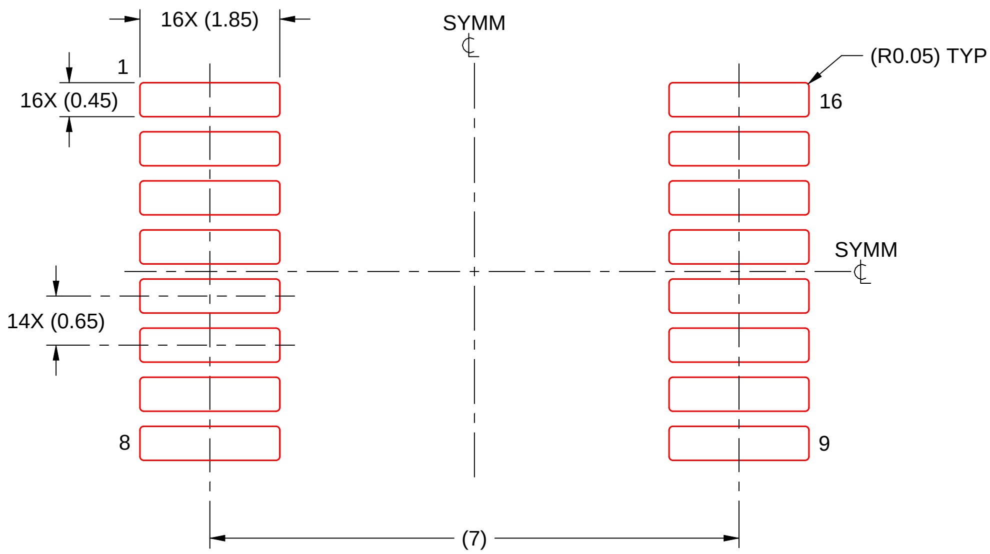
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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