

# LP5862 2 x 18 LED 矩阵驱动器，8 位模拟和 8 位/16 位 PWM 调光

## 1 特性

- LED 矩阵拓扑：
  - 18 个恒定电流阱，具有 2 个扫描开关，可实现 36 个 LED 点
  - 可针对 1 至 2 个扫描开关进行配置
- 工作电压范围：
  - $V_{CC}/V_{LED}$  范围：2.7V 至 5.5V
  - 逻辑引脚兼容 1.8V、3.3V 和 5V 电压
- 18 个高精度恒定电流阱：
  - 当  $V_{CC} \geq 3.3V$  时，每个电流阱的电流为 0.1mA - 50mA
  - 器件间误差： $\pm 5\%$
  - 通道间误差： $\pm 5\%$
  - 相移可平衡瞬态功耗
- 超低功耗：
  - 关断模式：当 EN 为低电平时  $I_{CC} \leq 2\mu A$
  - 待机模式：当 EN 为高电平且 CHIP\_EN 为 0（保留数据）时  $I_{CC} \leq 10\mu A$
  - 工作模式：当通道电流为 5mA 时  $I_{CC} = 3mA$ （典型值）
- 灵活的调光选项：
  - 对每个 LED 点进行单独的开关控制
  - 模拟调光（电流增益控制）
    - 为所有 LED 点提供全局 3 位最大电流 (MC) 设置
    - 为红色、绿色和蓝色提供 3 组 7 位颜色电流 (CC) 设置
    - 为每个 LED 点提供单独的 8 位点电流 (DC) 设置
  - 以无可闻噪声的频率进行 PWM 调光
    - 为所有 LED 点实现全局 8 位 PWM 调光
    - 为 LED 点任意映射实现 3 组可编程 8 位 PWM 调光
    - 为每个 LED 点实现单独的 8 位或 16 位 PWM 调光
- 完整的可寻址 SRAM，可更大限度地减少数据流量
- 针对各个 LED 点进行开路和短路检测
- 提供重影消除和低亮度补偿功能
- 接口选项：
  - 当 IFS 为低电平时采用 1MHz（最大值）I<sup>2</sup>C 接口
  - 当 IFS 为高电平时采用 12MHz（最大值）SPI 接口

## 2 应用

- 用于以下设备的 LED 动画和指示：
  - 键盘、鼠标和游戏附件

- 大型和智能家用电器
  - 智能音箱、有线和无线音箱
  - 混音器、DJ 设备和广播
  - 接入设备、交换机和服务器
- 用于光学模块的恒定电流阱

## 3 说明

电子设备变得越来越智能，而且需要使用更多的 LED 提供动画效果和指示功能，因此需要使用高性能 LED 矩阵驱动器以小尺寸解决方案改善用户体验。

LP586x 器件是高性能 LED 矩阵驱动器系列。该系列器件集成了 18 个具有 N (N = 1/2/4/6/8/11) 个开关 MOSFET 的恒定电流阱，以支持 N × 18 个 LED 点或 N × 6 个 RGB LED。LP5862 集成了 2 个 MOSFET，从而支持多达 36 个 LED 点或 12 个 RGB LED。

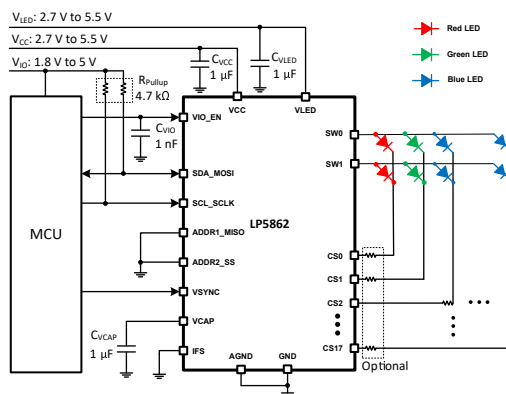
LP5862 同时支持模拟调光和 PWM 调光方法。对于模拟调光，能够以 256 个阶跃来调节每个 LED 点。对于 PWM 调光，集成式 8 位或 16 位可配置 PWM 发生器可实现平滑且无可闻噪声的调光控制。也可以将每个 LED 点任意映射到 8 位组 PWM，以实现共同调光控制。

LP5862 器件实现了完整的可寻址 SRAM，可更大限度减少数据流量。集成了重影消除电路以消除上下重影。LP5862 还支持 LED 开路和短路检测功能。LP5862 同时支持 1MHz（最大值）I<sup>2</sup>C 和 12MHz（最大值）SPI。

### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸（标称值）
LP5862	VQFN (32)	4mm × 4mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

## Table of Contents

<b>1 特性</b> .....	1	8.5 Programming.....	24
<b>2 应用</b> .....	1	8.6 Register Maps.....	27
<b>3 说明</b> .....	1	<b>9 Application and Implementation</b> .....	32
<b>4 Revision History</b> .....	2	9.1 Application Information.....	32
<b>5 Device Comparison</b> .....	3	9.2 Typical Application.....	32
<b>6 Pin Configuration and Functions</b> .....	4	<b>10 Power Supply Recommendations</b> .....	35
<b>7 Specifications</b> .....	6	<b>11 Layout</b> .....	36
7.1 Absolute Maximum Ratings.....	6	11.1 Layout Guidelines.....	36
7.2 ESD Ratings.....	6	11.2 Layout Example.....	36
7.3 Recommended Operating Conditions.....	6	<b>12 Device and Documentation Support</b> .....	37
7.4 Thermal Information.....	6	12.1 Documentation Support.....	37
7.5 Electrical Characteristics.....	7	12.2 接收文档更新通知.....	37
7.6 Timing Requirements.....	8	12.3 支持资源.....	37
7.7 Typical Characteristics.....	11	12.4 Trademarks.....	37
<b>8 Detailed Description</b> .....	13	12.5 Electrostatic Discharge Caution.....	37
8.1 Overview.....	13	12.6 术语表.....	37
8.2 Functional Block Diagram.....	13	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	38
8.3 Feature Description.....	13		
8.4 Device Functional Modes.....	23		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2021	*	Initial release

## 5 Device Comparison

PART NUMBER	MATERIAL	LED DOT NUMBER	PACKAGE <sup>(2)</sup>	SOFTWARE COMPATIBLE
LP5861	LP5861RSMR	18 × 1 = 18	VQFN-32	Yes
LP5862	LP5862RSMR	18 × 2 = 36	VQFN-32	
	LP5862DBTR		TSSOP-38	
LP5864	LP5864RSMR	18 × 4 = 72	VQFN-32	
	LP5864MRSMR <sup>(1)</sup>			
LP5866	LP5866RKPR	18 × 6 = 108	VQFN-40	
	LP5866DBTR		TSSOP-38	
	LP5866MDBTR <sup>(1)</sup>			
LP5868	LP5868RKPR	18 × 8 = 144	VQFN-40	
LP5860	LP5862RKPR	18 × 11 = 198	VQFN-40	
	LP5862MRKPR <sup>(1)</sup>			

- (1) Extended Temperature devices, supporting - 55°C to approximately 125°C operating ambient temperature.  
(2) The same packages are hardware compatible.

## 6 Pin Configuration and Functions

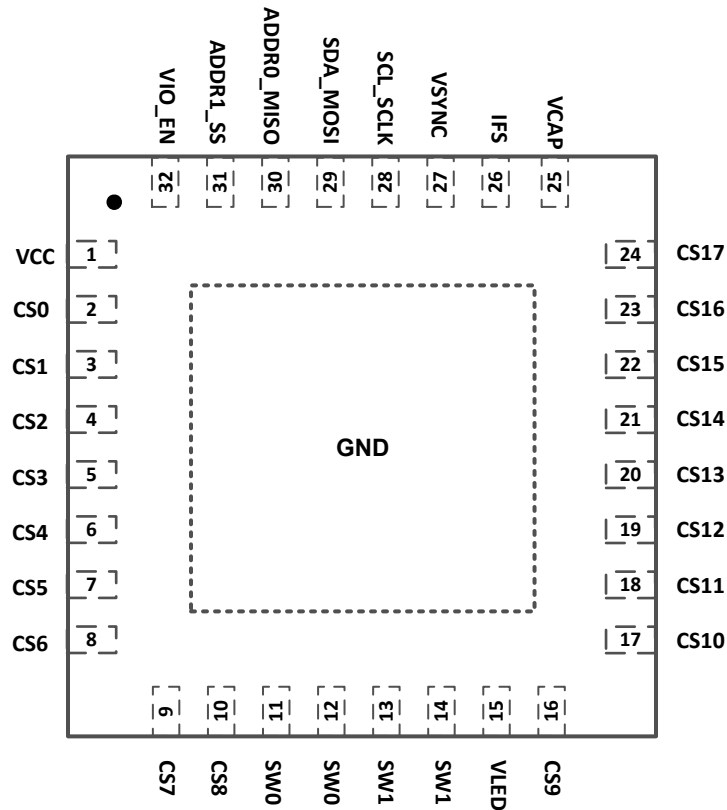


图 6-1. LP5862 RKP Package 40-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	Power	Power supply for device. A 1- $\mu$ F capacitor must be connected between this pin with GND and be placed as close to the device as possible.
2	CS0	O	Current sink 0. If not used, this pin must be left floating.
3	CS1	O	Current sink 1. If not used, this pin must be left floating.
4	CS2	O	Current sink 2. If not used, this pin must be left floating.
5	CS3	O	Current sink 3. If not used, this pin must be left floating.
6	CS4	O	Current sink 4. If not used, this pin must be left floating.
7	CS5	O	Current sink 5. If not used, this pin must be left floating.
8	CS6	O	Current sink 6. If not used, this pin must be left floating.
9	CS7	O	Current sink 7. If not used, this pin must be left floating.
10	CS8	O	Current sink 8. If not used, this pin must be left floating.
11/12	SW0	O	High-side PMOS switch output 0. Both 2 pins must be tied together. If not used, this pin must be left floating.
13/14	SW1	O	High-side PMOS switch output 1. Both 2 pins must be tied together. If not used, this pin must be left floating.
15	VLED	Power	Power input for high-side switches
16	CS9	O	Current sink 9. If not used, this pin must be left floating.
17	CS10	O	Current sink 10. If not used, this pin must be left floating.
18	CS11	O	Current sink 11. If not used, this pin must be left floating.

**表 6-1. Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NO.	NAME		
19	CS12	O	Current sink 12. If not used, this pin must be left floating.
20	CS13	O	Current sink 13. If not used, this pin must be left floating.
21	CS14	O	Current sink 14. If not used, this pin must be left floating.
22	CS15	O	Current sink 15. If not used, this pin must be left floating.
23	CS16	O	Current sink 16. If not used, this pin must be left floating.
24	CS17	O	Current sink 17. If not used, this pin must be left floating.
25	VCAP	O	Internal LDO output. An 1- $\mu$ F capacitor must be connected between this pin with GND. Place the capacitor as close to the device as possible.
26	IFS	I	Interface type select. I <sup>2</sup> C is selected when IFS is low. SPI is selected when IFS is high. A resistor must be connected between VIO and this pin.
27	VSYNC	I	External synchronize signal for display mode 2 and mode 3
28	SCL_SCLK	I	I <sup>2</sup> C clock input or SPI clock input. Pull up to VIO when configured as I <sup>2</sup> C.
29	SDA_MOSI	I/O	I <sup>2</sup> C data input or SPI leader output follower input. Pull up to VIO when configured as I <sup>2</sup> C.
30	ADDR0_MISO	I/O	I <sup>2</sup> C address select 0 or SPI leader input follower output
31	ADDR1_SS	I	I <sup>2</sup> C address select 1 or SPI follower select
32	VIO_EN	Power,I	Power supply for digital circuits and chip enable. A 1-nF capacitor must be connected between this pin with GND and be placed as close to the device as possible.
Exposed Thermal Pad	GND	Ground	Common ground plane

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage on V <sub>CC</sub> / V <sub>LED</sub> / V <sub>IO</sub> / EN / CS / SW / SDA / SCL / SCLK / MOSI / MISO / SS / ADDR0 / ADDR1 / VSYNC / IFS		- 0.3	6	V
Voltage on VCAP		- 0.3	2	V
T <sub>J</sub>	Junction temperature	- 55	150	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±3000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage on V <sub>CC</sub>	Supply voltage	2.7		5.5	V
Input voltage on V <sub>LED</sub>	LED supply voltage	2.7		5.5	V
Input voltage on V <sub>IO_EN</sub>		1.65		5.5	V
Voltage on SDA / SCL / SCLK / MOSI / MISO / SS / ADDR <sub>x</sub> / VSYNC / IFS				V <sub>IO</sub>	V
T <sub>A</sub>	Operating ambient temperature	- 40		85	°C
T <sub>A</sub>	Operating ambient temperature - LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR only	- 55		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LP5864, LP5862, LP5861	UNIT
		RSM (VQFN)	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	32.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	29.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	12.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

$V_{CC} = 3.3V$ ,  $V_{LED} = 3.8V$ ,  $V_{IO} = 1.8V$  and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  ( $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR); Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power supplies</b>						
$V_{CC}$	Device supply voltage		2.7		5.5	V
$V_{UVR}$	Undervoltage restart	$V_{CC}$ rising, Test mode			2.5	V
$V_{UVF}$	Undervoltage shutdown	$V_{CC}$ falling, Test mode	1.9			V
$V_{UV\_HYS}$	Undervoltage shutdown hysteresis			0.3		V
$V_{CAP}$	Internal LDO output	$V_{CC} = 2.7 V$ to $5.5 V$		1.78		V
$I_{CC}$	Shutdown supply current $I_{SHUTDOWN}$	$V_{EN} = 0 V$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$		0.1	1	$\mu A$
	Standby supply current $I_{STANDBY}$	$V_{EN} = 3.3 V$ , $CHIP\_EN = 0$ (bit), measure the total current from $V_{CC}$ and $V_{LED}$		5.5	10	$\mu A$
	Active mode supply current $I_{NORMAL}$	$V_{EN} = 3.3 V$ , $CHIP\_EN = 1$ (bit), all channels $I_{OUT} = 5 mA$ ( $MC = 1$ , $CC = 127$ , $DC = 256$ ), measure the current from $V_{CC}$		4.3	6	mA
$V_{LED}$	LED supply voltage		2.7		5.5	V
$V_{VIO}$	VIO supply voltage		1.65		5.5	V
$I_{VIO}$	VIO supply current	Interface idle			5	$\mu A$
<b>Output Stages</b>						
$I_{CS}$	Constant current sink output range (CS0 - CS17)	$2.7 V \leq V_{CC} < 3.3 V$ , PWM = 100%	0.1		40	mA
		$V_{CC} \geq 3.3 V$ PWM = 100%	0.1		50	mA
$I_{LKG}$	Leakage current (CS0 - CS17)	channels off, up_degghost = 0, $V_{CS} = 5 V$		0.1	1	$\mu A$
$I_{ERR\_DD}$	Device to device current error, $I_{ERR\_DD} = (I_{AVE} - I_{SET}) / I_{SET} \times 100\%$	All channels ON. Current set to 0.1 mA. $MC = 0$ $CC = 42$ $DC = 25$ PWM = 100%	- 7		7	%
		All channels ON. Current set to 1 mA. $MC = 2$ $CC = 127$ $DC = 25$ PWM = 100%	- 5		5	%
		All channels ON. Current set to 10 mA. $MC = 2$ $CC = 127$ $DC = 255$ PWM = 100%	- 3.5		3.5	%
		All channels ON. Current set to 25 mA. $MC = 7$ $CC = 64$ $DC = 255$ PWM = 100%	- 3.5		3.5	%
		All channels ON. Current set to 50 mA. $MC = 7$ $CC = 127$ $DC = 255$ PWM = 100%	- 3		3	%
$I_{ERR\_CC}$	Channel to channel current error, $I_{ERR\_CC} = (I_{OUTX} - I_{AVE}) / I_{AVE} \times 100\%$	All channels ON. Current set to 0.1 mA. $MC = 0$ $CC = 42$ $DC = 25$ PWM = 100%	- 5.5		5.5	%
		All channels ON. Current set to 1 mA. $MC = 2$ $CC = 127$ $DC = 25$ PWM = 100%	- 5		5	%
		All channels ON. Current set to 10 mA. $MC = 2$ $CC = 127$ $DC = 255$ PWM = 100%	- 4		4	%
		All channels ON. Current set to 25 mA. $MC = 7$ $CC = 64$ $DC = 255$ PWM = 100%	- 3.5		3.5	%
		All channels ON. Current set to 50 mA. $MC = 7$ $CC = 127$ $DC = 255$ PWM = 100%	- 3		3	%
$f_{PWM}$	LED PWM frequency	PWM_Fre = 1, PWM = 100%		62.5		KHz
		PWM_Fre = 0, PWM = 100%		125		KHz

## 7.5 Electrical Characteristics (continued)

$V_{CC} = 3.3V$ ,  $V_{LED} = 3.8V$ ,  $V_{IO} = 1.8V$  and  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  ( $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR); Typical values are at  $T_A = 25^{\circ}C$  (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SAT}$	Output saturation voltage	$I_{OUT} = 50$ mA, decreasing output voltage, when the LED current has dropped 5%			0.45	V
		$I_{OUT} = 30$ mA, decreasing output voltage, when the LED current has dropped 5%			0.4	V
		$I_{OUT} = 10$ mA, decreasing output voltage, when the LED current has dropped 5%			0.35	V
$R_{SW}$	High-side PMOS ON resistance	$V_{LED} = 2.7$ V, $I_{SW} = 200$ mA		450	550	m $\Omega$
		$V_{LED} = 2.7$ V, $I_{SW} = 200$ mA, LP5860MRKPR and LP5864MRSMR		450	570	m $\Omega$
		$V_{LED} = 3.8$ V, $I_{SW} = 200$ mA		380	500	m $\Omega$
		$V_{LED} = 3.8$ V, $I_{SW} = 200$ mA, LP5860MRKPR and LP5864MRSMR		380	520	m $\Omega$
		$V_{LED} = 5$ V, $I_{SW} = 200$ mA		310	450	m $\Omega$
		$V_{LED} = 5$ V, $I_{SW} = 200$ mA, LP5860MRKPR and LP5864MRSMR		310	490	m $\Omega$
<b>Logic Interfaces</b>						
$V_{LOGIC\_IL}$	Low-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS			$0.3 \times V_{IO}$		V
$V_{LOGIC\_IH}$	High-level input voltage, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub> , VSYNC, IFS		$0.7 \times V_{IO}$			V
$V_{EN\_IL}$	Low-level input voltage of EN			0.4		V
$V_{EN\_IH}$	High-level input voltage of EN	When $V_{CAP}$ powered up	1.4			V
$I_{LOGIC\_I}$	Input current, SDA, SCL, SCLK, MOSI, SS, ADDR <sub>x</sub>		- 1		1	$\mu$ A
$V_{LOGIC\_OL}$	Low-level output voltage, SDA, MISO	$I_{PULLUP} = 3$ mA			0.4	V
$V_{LOGIC\_OH}$	High-level output voltage, MISO	$I_{PULLUP} = - 3$ mA	$0.7 \times V_{IO}$			V
<b>Protection Circuits</b>						
$V_{LOD\_TH}$	Threshold for channel open detection			0.25		V
$V_{LSD\_TH}$	Threshold for channel short detection			$V_{LED} - 1$		V
$T_{TSD}$	Thermal-shutdown junction temperature			150		$^{\circ}C$
$T_{HYS}$	Thermal shutdown temperature hysteresis			15		$^{\circ}C$

## 7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>MISC. Timing Requirements</b>					
$f_{OSC}$	Internal oscillator frequency		31.2		MHz
$f_{OSC\_ERR}$	Device to device oscillator frequency error	- 3%		3%	
$t_{POR\_H}$	Wait time from UVLO disactive to device NORMAL			500	$\mu$ s
$t_{CHIP\_EN}$	Wait time from setting Chip_EN (Register) = 1 to device NORMAL			100	$\mu$ s
$t_{RISE}$	LED output rise time		10		ns
$t_{FALL}$	LED output fall time		15		ns
$t_{VSYNC\_H}$	The minimum high-level pulse width of VSYNC	200			$\mu$ s
<b>SPI timing requirements</b>					
$f_{SCLK}$	SPI Clock frequency			12	MHz
1	Cycle time	83.3			ns

## 7.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
2	SS active lead-time	50			ns
3	SS active leg time	50			ns
4	SS inactive time	50			ns
5	SCLK low time	36			ns
6	SCLK high time	36			ns
7	MOSI set-up time	20			ns
8	MOSI hold time	20			ns
9	MISO disable time			30	ns
10	MISO data valid time			35	ns
$C_b$	Bus capacitance	5		40	pF
<b>I<sup>2</sup>C fast mode timing requirements</b>					
$f_{SCL}$	I <sup>2</sup> C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	600			ns
2	Clock low time	1300			ns
3	Clock high time	600			ns
4	Set-up time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data set-up time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Set-up time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			$\mu$ s
<b>I<sup>2</sup>C fast mode plus timing requirements</b>					
$f_{SCL}$	I <sup>2</sup> C clock frequency	0		400	KHz
1	Hold time (repeated) START condition	600			ns
2	Clock low time	1300			ns
3	Clock high time	600			ns
4	Setup time for a repeated START condition	600			ns
5	Data hold time	0			ns
6	Data setup time	100			ns
7	Rise time of SDA and SCL			300	ns
8	Fall time of SDA and SCL			300	ns
9	Set-up time for STOP condition	600			ns
10	Bus free time between a STOP and a START condition	1.3			$\mu$ s

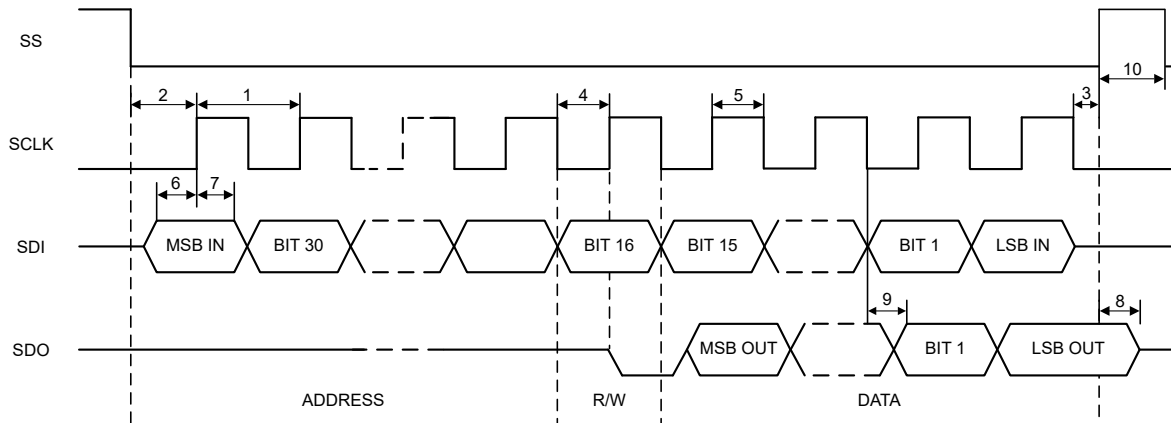


图 7-1. SPI Timing Parameters

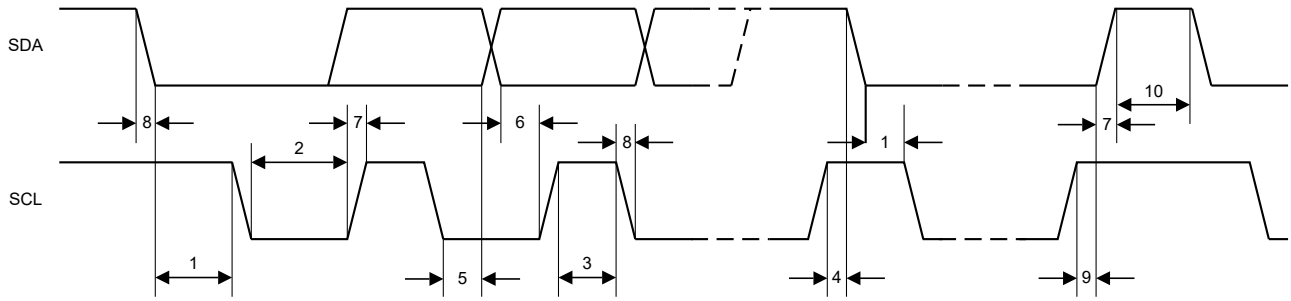


图 7-2. I<sup>2</sup>C Timing Parameters

## 7.7 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$  for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR while  $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$  for the other devices),  $V_{CC} = 3.3\text{ V}$ ,  $V_{IO} = 3.3\text{ V}$ ,  $V_{LED} = 5\text{ V}$ ,  $I_{LED\_Peak} = 50\text{ mA}$ ,  $C_{VLED} = 1\ \mu\text{F}$ ,  $C_{VCC} = 1\ \mu\text{F}$ .

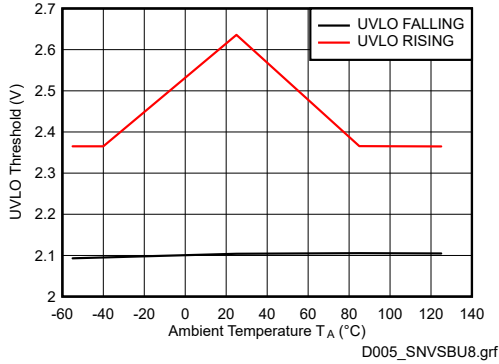


图 7-3.  $V_{CC}$  UVLO Rising and Falling Thresholds

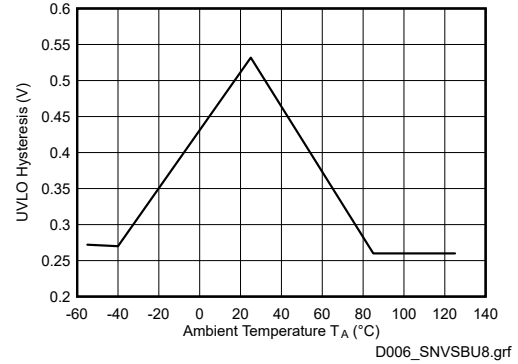


图 7-4.  $V_{CC}$  UVLO Hysteresis

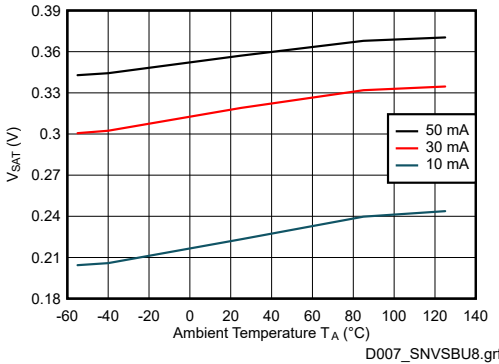


图 7-5.  $V_{SAT}$  vs Temperature

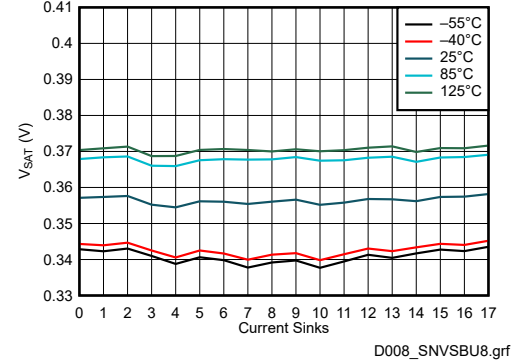


图 7-6.  $V_{SAT}$  vs Current Sinks (50 mA)

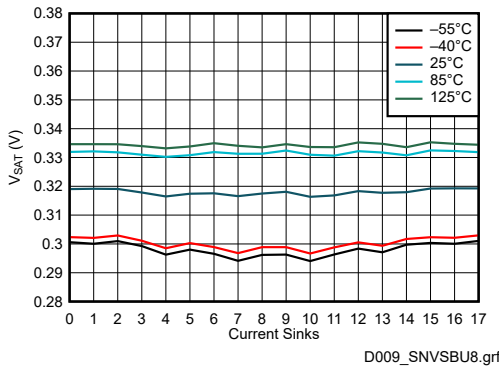


图 7-7.  $V_{SAT}$  vs Current Sinks (30 mA)

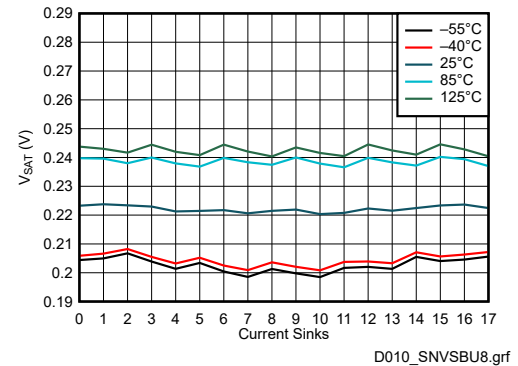
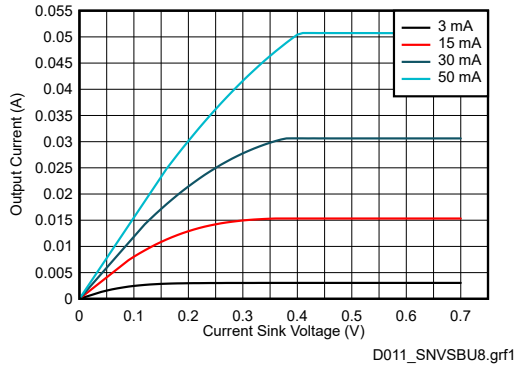


图 7-8.  $V_{SAT}$  vs Current Sinks (10 mA)

### 7.7 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range ( $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$  for LP5860MRKPR, LP5864MRSMR, and LP5866MDBTR while  $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$  for the other devices),  $V_{CC} = 3.3\text{ V}$ ,  $V_{IO} = 3.3\text{ V}$ ,  $V_{LED} = 5\text{ V}$ ,  $I_{LED\_Peak} = 50\text{ mA}$ ,  $C_{VLED} = 1\ \mu\text{F}$ ,  $C_{VCC} = 1\ \mu\text{F}$ .



$T_A = 25^{\circ}\text{C}$

图 7-9. Current Sinks Voltage vs Current

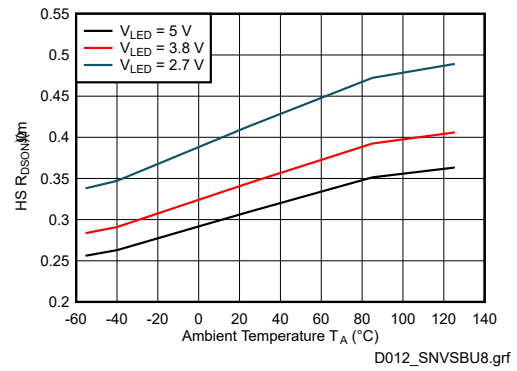


图 7-10. High Side Switch  $R_{DS(on)}$

## 8 Detailed Description

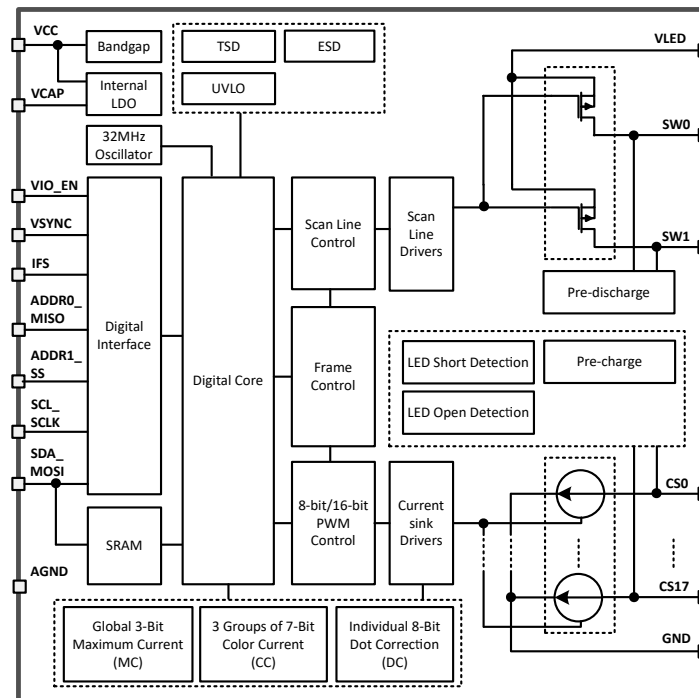
### 8.1 Overview

The LP5862 is an  $2 \times 18$  LED matrix driver. The device integrates 2 switching FETs with 18 constant current sinks. One LP5862 device can drive up to 36 LED dots or 12 RGB pixels by using time-multiplexing matrix scheme.

The LP5862 supports both analog dimming and PWM dimming methods. For analog dimming, the current gain of each individual LED dot can be adjusted with 256 steps through 8-bits dot correction. For PWM dimming, the integrated 8-bits or 16-bits configurable, > 20-KHz PWM generators for each LED dot enable smooth, vivid animation effects without audible noise. Each LED can also be mapped into a 8-bits group PWM to achieve the group control with minimum data traffic.

The LP5862 device implements full addressable SRAM. The device supports entire SRAM data refresh and partial SRAM data update on demand to minimize the data traffic. The LP5862 implements the ghost cancellation circuit to eliminate both upside and downside ghosting. The LP5862 also uses low brightness compensation technology to support high density LED pixels. Both 1-MHz (maximum) I<sup>2</sup>C and 12-MHz (maximum) SPI interfaces are available in the LP5862.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Time-Multiplexing Matrix

The LP5862 device uses time-multiplexing matrix scheme to support up to 36 LED dots with a single chip. The device integrates 18 current sinks with 2 scan lines to drive  $18 \times 2 = 36$  LED dots or  $6 \times 2 = 12$  RGB pixels. In matrix control scheme, the device scans from Line 0 to Line 1 sequentially as shown in [图 8-1](#). Current gain and PWM duty registers are programmable for each LED dot to support individual analog and PWM dimming.

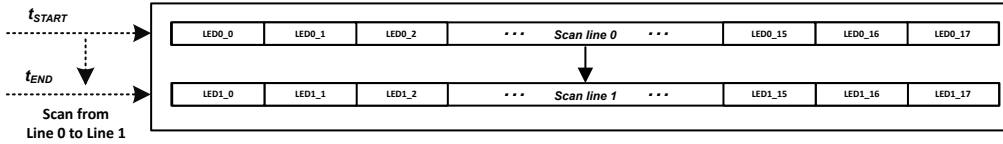


图 8-1. Scan Line Control Scheme

There are two high-side p-channel MOSFETs (PMOS) integrated in LP5862 device. Users can flexibly set the active scan numbers from 1 to 2 by configuring the 'Max\_Line\_Num' in Dev\_initial register. The time-multiplexing matrix timing sequence follows the 图 8-2.

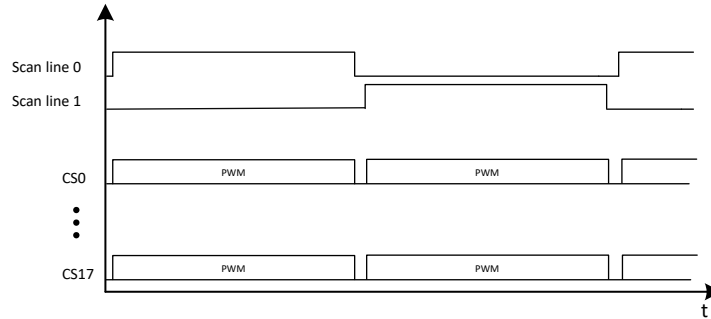


图 8-2. Time-Multiplexing Matrix Timing Sequence

One cycle time of the line switching can be calculated as below:

$$t_{line\_switch} = t_{PWM} + t_{SW\_BLK} + 2 \times t_{phase\_shift} \tag{1}$$

- $t_{PWM}$  is the current sink active time, which equals to 8 us (PWM frequency set at 125 kHz) or 16 us (PWM frequency set at 62.5 kHz) by configuring 'PWM\_Fre' in Dev\_initial register.
- $t_{SW\_BLK}$  is the switch blank time, which equals to 1 us or 0.5 us by configuring 'SW\_BLK' in Dev\_config1 register.
- $t_{phase\_shift}$  is the PWM phase shift time, which equals to 0 or 125 ns by configuring 'PWM\_Phase\_Shift' in Dev\_config1 register.

Total display time for one complete sub-period is  $t_{sub\_period}$  and it can be calculated by the following equation:

$$t_{sub\_period} = t_{line\_switch} \times Scan\_line\# \tag{2}$$

- Scan\_line# is the scan line number determined by 'Max\_Line\_Num' in Dev\_initial register.

The time-multiplexing matrix scheme time diagram is shown in 图 8-3. The  $t_{CS\_ON\_Shift}$  is the current sink turning on shift by configuring 'CS\_ON\_Shift' bit in Dev\_config1 register.

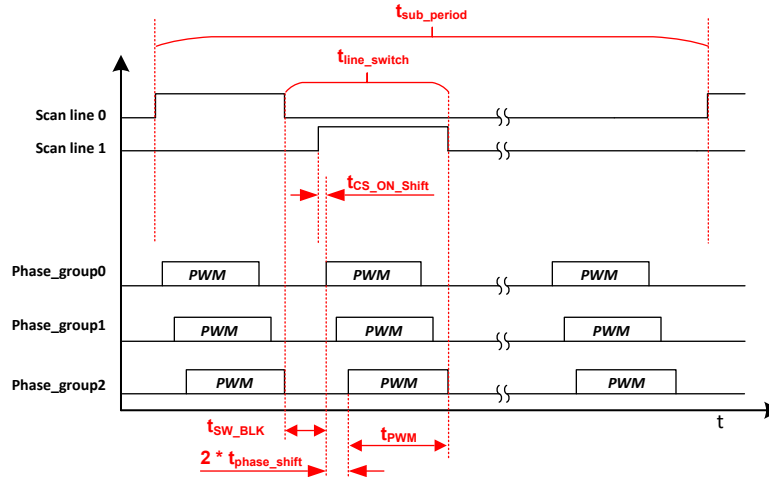


图 8-3. Time-Multiplexing Matrix Timing Diagram

The LP5862 device implements deghosting and low brightness compensation to remove the side effects of matrix topology:

- **Deghosting:** both upside deghosting and downside deghosting are implemented to eliminate the LED's unexpected weak turn-on.
  - Upside\_deghosting: discharge each scan line during its off state. By configuring the 'Up\_Deghost' in Dev\_config3 register, the LP5862 discharges and clamps the scan line switch to a certain voltage.
  - Downside\_deghosting: pre-charge each current sink voltage during its off state. The deghosting capability can be adjusted through the 'Down\_Deghost' in Dev\_config3 register.
- **Low Brightness Compensation:** three groups compensation are implemented to overcome the color-shift and non-uniformity in low brightness conditions. The compensation capability can be through 'Comp\_Group1', 'Comp\_Group2', and 'Comp\_Group3' in Dev\_config2 register.
  - Compensation\_group 1: CS0, CS3, CS6, CS9, CS12, CS15
  - Compensation\_group 2: CS1, CS4, CS7, CS10, CS13, CS16
  - Compensation\_group 3: CS2, CS5, CS8, CS11, CS14, CS17

### 8.3.2 Analog Dimming (Current Gain Control)

Analog dimming of LP5862 is achieved by configuring the current gain control. There are several methods to control the current gain of each LED.

- Global 3-bits Maximum Current (MC) setting without external resistor
- 3 Groups of 7-bits Color Current (CC) setting
- Individual 8-bit Dot Current (DC) setting

#### Global 3-Bits Maximum Current (MC) Setting

The MC is used to set the maximum current,  $I_{OUT\_MAX}$ , for each current sink, and this current is the maximum peak current for each LED dot. The MC can be set with 3 bits (8 steps) from 3 mA to 50 mA. When the device is powered on, the MC data is set to default value, which is 15 mA.

For data refresh **Mode 1**, MC data is effective immediately after new data updated. For **Mode 2** and **Mode 3**, to avoid unexpected MC data change during high speed data refreshing, MC data must be changed when all channels are off and new MC data is only be updated when the 'Chip\_EN' bit in Chip\_en register is set to 0, and after the 'Chip\_EN' returns to 1, the new MC data is effective. 'Down\_Deghost' and 'Up\_Deghost' in Dev\_config3 work in the similar way with MC.

表 8-1. Maximum Current (MC) Register Setting

3-BITS MAXIMUM_CURRENT REGISTER		I <sub>OUT_MAX</sub>
Binary	Decimal	mA
000	0	3
001	1	5
010	2	10
011 (default)	3 (default)	15 (default)
100	4	20
101	5	30
110	6	40
111	7	50

### 3 Groups of 7-Bits Color Current (CC) Setting

The LP5862 device is able to adjust the output current of three color groups separately. For each color, it has 7-bits data in 'CC\_Group1', 'CC\_Group2', and 'CC\_Group3'. Thus, all color group currents can be adjusted in 128 steps from 0% to 100% of the maximum output current, I<sub>OUT\_MAX</sub>.

The 18 current sinks have fixed mapping to the three color groups:

- CC-Group 1: CS0, CS3, CS6, CS9, CS12, CS15
- CC-Group 2: CS1, CS4, CS7, CS10, CS13, CS16
- CC-Group 3: CS2, CS5, CS8, CS11, CS14, CS17

表 8-2. 3 Groups of 7-bits Color Current (CC) Setting

7-BITS CC_GROUP1/CC_GROUP2/CC_GROUP3 REGISTER		RATIO OF OUTPUT CURRENT TO I <sub>OUT_MAX</sub>
Binary	Decimal	%
000 0000	0	0
000 0001	1	0.79
000 0010	2	1.57
---	---	---
100 0000 (default)	64 (default)	50.4 (default)
---	---	---
111 1101	125	98.4
111 1110	126	99.2
111 1111	127	100

### Individual 8-bit Dot Current (DC) Setting

The LP5862 can individually adjust the output current of each LED by using dot current function through DC setting. The device allows the brightness deviations of the LEDs to adjusted be individually. Each output DC is programmed with a 8-bit depth, so the value can be adjusted with 256 steps within the range from 0% to 100% of (I<sub>OUT\_MAX</sub> × CC/127).

表 8-3. Individual 8-bit Dot Current (DC) Setting

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO I <sub>OUT_MAX</sub> × CC/127
Binary	Decimal	%
0000 0000	0	0
0000 0001	1	0.39
0000 0010	2	0.78
---	---	---
1000 0000 (default)	128 (default)	50.2 (default)

表 8-3. Individual 8-bit Dot Current (DC) Setting (continued)

8-BIT DC REGISTER		RATIO OF OUTPUT CURRENT TO $I_{OUT\_MAX} \times CC/127$	
Binary	Decimal	%	
---	---	---	
1111 1101	253	99.2	
1111 1110	254	99.6	
1111 1111	255	100	

In summary, the current gain of each current sink can be calculated as below:

$$I_{OUT} \text{ (mA)} = I_{OUT\_MAX} \times (CC/127) \times (DC/255) \quad (3)$$

For time-multiplexing scan scheme, if the scan number is N, each LED dot's average current  $I_{AVG}$  is shown as below:

$$I_{AVG} \text{ (mA)} = I_{OUT} / N = I_{OUT\_MAX} \times (CC/127) \times (DC/255)/N \quad (4)$$

### 8.3.3 PWM Dimming

There are several methods to control the PWM duty cycle of each LED dot.

- **Individual 8-bit / 16-bit PWM for Each LED Dot**

Every LED has an individual 8-bit or 16-bit PWM register that is used to change the LED brightness by PWM duty. The LP5862 uses an enhanced spectrum PWM (ES-PWM) algorithm to achieve 16-bit depth with high refresh rate and this can avoid flicker under high speed camera. Comparing with conventional 8-bit PWM, 16-bit PWM can help to achieve ultimate high dimming resolution in LED animation applications.

- **3 Programmable Groups of 8-bit PWM Dimming**

The group PWM Control is used to select LEDs into 1 to 3 groups where each group has a separate register for duty cycle control. Every LED has 2-bit selection in LED\_DOT\_GROUP Registers ( $x = 0, 1, \dots, 9$ ) to select whether it belongs to one of the three groups or not:

- 00: not a member of any group
- 01: member of group 1
- 10: member of group 2
- 11: member of group 3

- **8-bit PWM for Global Dimming**

The Global PWM Control function affects all LEDs simultaneously.

The final PWM duty cycle can be calculated as below:

$$PWM\_Final(8 \text{ bit}) = PWM\_Individual(8 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(-\text{bit}) \quad (5)$$

$$PWM\_Final(16 \text{ bit}) = PWM\_Individual(16 \text{ bit}) \times PWM\_Group(8 \text{ bit}) \times PWM\_Global(8 \text{ bit}) \quad (6)$$

The LP5862 supports 125-kHz or 62.5-kHz PWM output frequency. The PWM frequency is selected by configuring the 'PWM\_Fre' in Dev\_initial register. An internal 32-MHz oscillator is used for generating PWM outputs. The oscillator's high accuracy design ( $f_{OSC\_ERR} \leq \pm 2\%$ ) enables a better synchronization if multiple LP5862 devices are connected together.

A PWM phase-shifting scheme is implemented in each current sink to avoid the current overshoot when turning on simultaneously. As the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. This scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases. By configuring the 'PWM\_Phase\_Shift' in Dev\_config1 register, which is default off, the LP5862 supports  $t_{\text{phase\_shift}} = 125\text{-ns}$  shifting time shown in 图 8-4.

- Phase 1: CS0, CS3, CS6, CS9, CS12, CS15
- Phase 2: CS1, CS4, CS7, CS10, CS13, CS16
- Phase 3: CS2, CS5, CS8, CS11, CS14, CS17

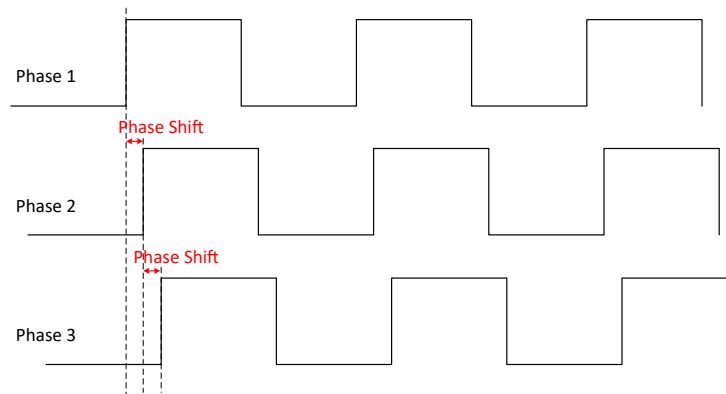


图 8-4. Phase Shift

To avoid high current sinks output ripple during line switching, current sinks can be configured to turn on with 1 clock delay (62.5 ns or 31.25 ns according to the PWM frequency) after lines turn on, as shown in 图 8-3. This function can be configured by 'CS\_ON\_Shift' in Dev\_config1 register.

The LP5862 allows users to configure the dimming scale either exponentially (Gamma Correction) or linearly through the 'PWM\_Scale\_Mode' in Dev\_config1 register. If a human-eye-friendly dimming curve is desired, using the internal fixed exponential scale is an easy approach. If a special dimming curve is desired, using the linear scale with software correction is recommended. The LP5862 supports both linear and exponential dimming curves under 8-bit and 16-bit PWM depth. 图 8-5 is an example of 8-bit PWM depth.

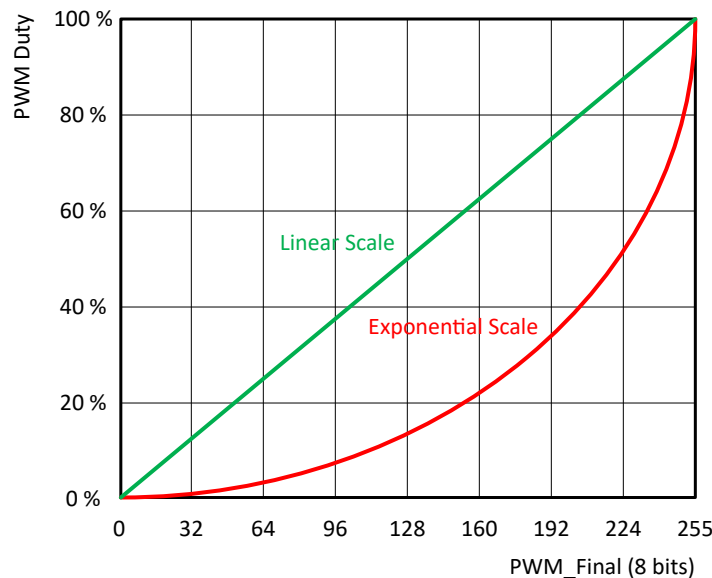


图 8-5. Linear and Exponential Dimming Curves

In summary, the PWM control method is illustrated as 图 8-6:

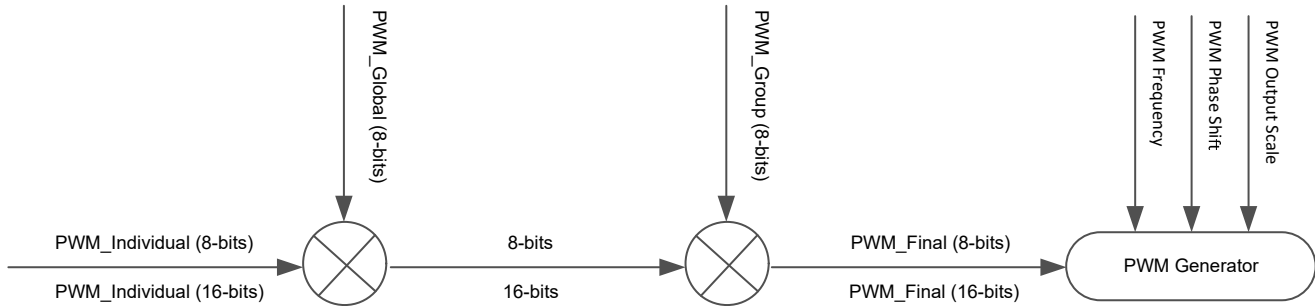


图 8-6. PWM Control Scheme

### 8.3.4 ON and OFF Control

The LP5862 device supports the individual ON and OFF control of each LED. For indication purpose, users can turn on and off the LED directly by writing 1-bit ON and OFF data to the corresponding Dot\_onoffx (x = 0, 1, ..., 5) register.

### 8.3.5 Data Refresh Mode

The LP5862 supports three data refresh modes: Mode 1, Mode 2, and Mode 3, by configuring 'Data\_Ref\_Mode' in Dev\_initial register.

**Mode 1:** 8-bit PWM data without VSYNC command. Data is sent out for display instantly after received. With Mode 1, users can refresh the corresponding dots' data only instead of updating the whole SRAM. It is called 'on demand data refresh', which can save the total data volume effectively. As shown in 图 8-7, the red LED dots can be refreshed after sending the corresponding data while the others kept the same with last frame.

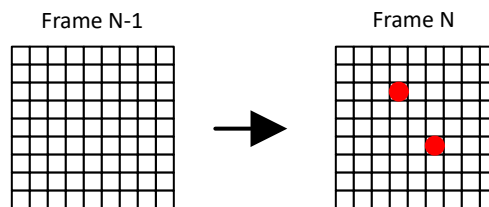


图 8-7. On Demand Data Refresh - Mode 1

**Mode 2:** 8-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

**Mode 3:** 16-bit PWM data with VSYNC command. Data is held and sent out simultaneously by frame after receiving the VSYNC command.

Frame control is implemented in Mode 2 and Mode 3. Instead of refreshing the output instantly after data is received (Mode 1), the device holds the data and refreshes the whole frame data by a fixed frame rate,  $f_{VSYNC}$ . Usually, 24 Hz, 50 Hz, 60 Hz, 120 Hz or even higher frame rate is selected to achieve vivid animation effects. Whole SRAM Data Refresh is shown in 图 8-8, a new frame is updated after receiving the VSYNC command.

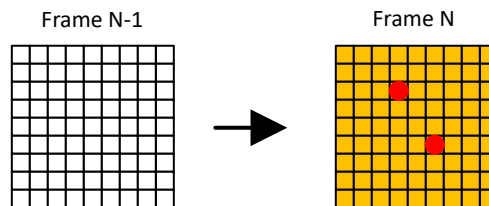


图 8-8. Whole SRAM Data Refresh

Comparing with Mode 1, Mode 2 and Mode 3 provide a better synchronization when multiple LP5862 devices used together. A high-level pulse width longer than  $t_{\text{SYNC\_H}}$  is required at the beginning of each VSYNC frame.

图 8-9 shows the VSYNC connections and 图 8-10 shows the timing requirements.

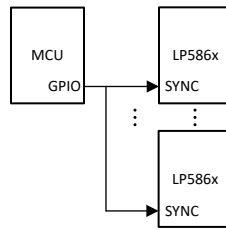


图 8-9. Multiple Devices Sync

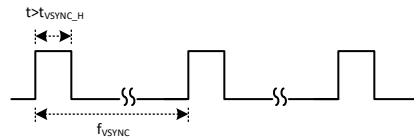


图 8-10. VSYNC Timing

Table 8-4 is the summary of the three data refresh modes.

表 8-4. Data Refresh Mode

MODE TYPE	PWM RESOLUTION	PWM OUTPUT	EXTERNAL VSYNC
Mode 1	8 bits	Data update instantly	No
Mode 2	8 bits	Data update by frame	Yes
Mode 3	16 bits		

### 8.3.6 Full Addressable SRAM

SRAM is implemented inside the LP5862 device to support data writing and reading at the same time.

Although data refresh mechanisms are not the same for Mode 1 and Mode 2 and 3, the data writing and reading follow the same method. Users can update partial of the SRAM data only or the whole SRAM page simultaneously. The LP5862 supports auto-increment function to minimize data traffic and increase data transfer efficiency.

Please be noted that 16-bit PWM (Mode 3) and 8-bit PWM (Mode 1 and Mode 2) are assigned with different SRAM addresses.

### 8.3.7 Protections and Diagnostics

#### LED Open Detection

The LP5862 includes LED open detection (LOD) for the fault caused by any opened LED dot. The threshold for LED open is 0.25-V typical. LED open detection is only performed when  $PWM \geq 25$  (Mode 1 and Mode 2) or  $PWM \geq 6400$  (Mode 3) and voltage on CSn is detected lower than open threshold for continuously 4 sub-periods.

图 8-11 shows the detection circuit of LOD function. When open fault is detected, 'Global\_LOD' bit in Fault\_state register is set to 1 and detailed fault state for each LED is also monitored in register Dot\_lodx ( $x = 0, 1, \dots, 5$ ). All open fault indicator bits can be cleared by setting LOD\_clear = 0Fh after the open condition is removed.

LOD removal function can be enabled by setting 'LOD\_removal' bit in Dev\_config2 register to 1. This function turns off the current sink of the open channel when scanning to the line where the opened LED is included.

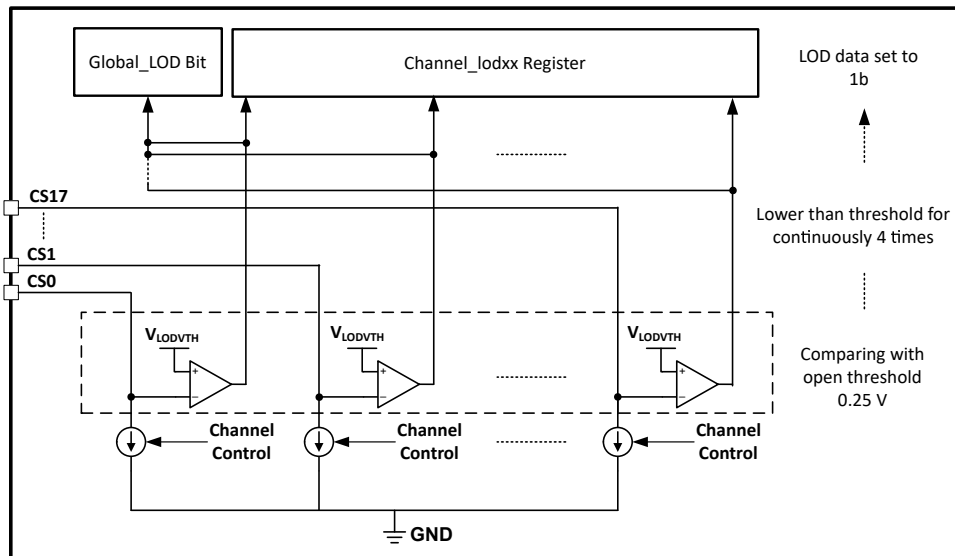


图 8-11. LOD Circuits

#### LED Short Detection

The LP5862 includes LED short detection (LSD) for the fault caused by any shorted LED. Threshold for channel short is  $(V_{LED} - 1)$  V typical. LED short detection only performed when  $PWM \geq 25$  (Mode 1 and Mode 2) or  $PWM \geq 6400$  (Mode 3) and voltage on CSn is detected higher than short threshold for continuously 4 sub-

periods. As there is parasitic capacitance for the current sink, to make sure the LSD result is correct, TI recommends to set the LED current higher than 0.5 mA.

图 8-12 shows the detection circuit of LSD function. When short fault is detected, 'Global\_LSD bit' in Fault\_state register is set to 1 and detailed fault state for every channel is also monitored in register Dot\_Isdx ( $x = 0, 1, \dots, 5$ ). All short fault indicator bits can be cleared by setting LSD\_clear = 0Fh after the short condition is removed.

LSD removal function can be enabled by setting 'LSD\_removal' bit in Dev\_config2 register to 1. This function turns off the upside deghosting function of the scan line where short LED is included.

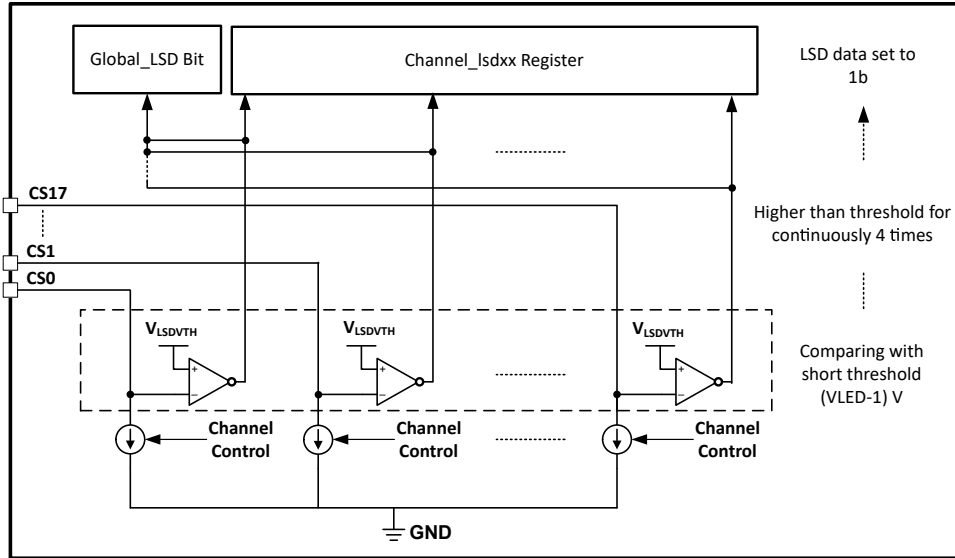


图 8-12. LSD Circuit

### Thermal Shutdown

The LP5862 device implements thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 160 °C (typical) and above, the device switches into shutdown mode. The LP5862 exits thermal shutdown when the junction temperature of the device drops to 145°C (typical) and below.

### UVLO (Undervoltage Lock Out)

The LP5862 has an internal comparator that monitors the voltage at VCC. When VCC is below V<sub>UVF</sub>, reset is active and the LP5862 enters INITIALIZATION state.

## 8.4 Device Functional Modes

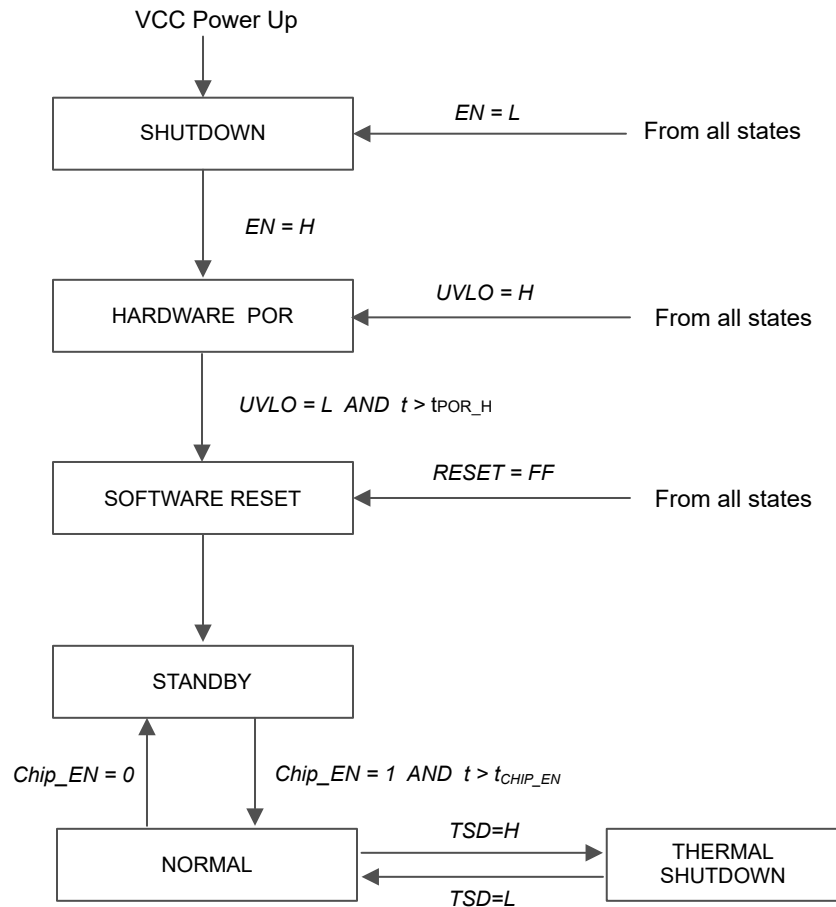


图 8-13. Device Functional Modes

- Shutdown: The device enters into shutdown mode from all states on VCC power up or EN pin is low.
- Hardware POR: The device enters into hardware POR when Enable pin is high or VCC fall under  $V_{UVF}$  causing  $UVLO = H$  from all states.
- Software reset: The device enters into software reset mode when VCC rise higher than  $V_{UVR}$  with the time  $t > t_{POR\_H}$ . In this mode, all the registers are reset. Entry can also be from any state when the RESET (register) = FFh or UVLO is low.
- Standby: The device enters the standby mode when Chip\_EN (register) = 0. In this mode, the device enters into low power mode, but the I<sup>2</sup>C/SPI are still available for Chip\_EN only and the registers' data are retained.
- Normal: The device enters the normal mode when 'Chip\_EN' = 1 with the time  $t > t_{CHIP\_EN}$ .
- Thermal shutdown: The device automatically enters the thermal shutdown mode when the junction temperature exceeds 160°C (typical). If the junction temperature decreases below 145°C (typical), the device returns to the normal mode.

## 8.5 Programming

### Interface Selection

The LP5862 supports two communication interfaces: I<sup>2</sup>C and SPI. If IFS is high, the device enters into SPI mode. If IFS is low, the device enters into I<sup>2</sup>C mode.

表 8-5. Interface Selection

INTERFACE TYPE	ENTRY CONDITION
I <sup>2</sup> C	IFS = Low
SPI	IFS = High

### I<sup>2</sup>C Interface

The LP5862 is compatible with I<sup>2</sup>C standard specification. The device supports both fast mode (400-KHz maximum) and fast plus mode (1-MHz maximum).

#### I<sup>2</sup>C Data Transactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, it must indicate to the transmitter an end of data by not acknowledging (*negative acknowledge*) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

#### I<sup>2</sup>C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 5-bits of the chip address, 2 higher bits of the register address, and 1 read and write bit. The other 8 lower bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

表 8-6. I<sup>2</sup>C Data Format

Address Byte 1	Chip Address					Register Address		R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	1	0	0	ADDR1	ADDR0	9 <sup>th</sup> bit	8 <sup>th</sup> bit	R: 1 W: 0
Broadcast	1	0	1	0	1			
Address Byte 2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit	1 <sup>th</sup> bit	0 <sup>th</sup> bit

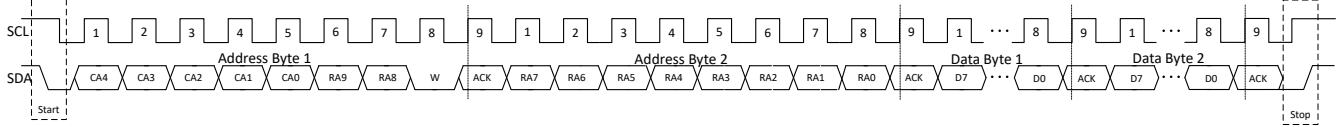


图 8-14. I<sup>2</sup>C Write Timing

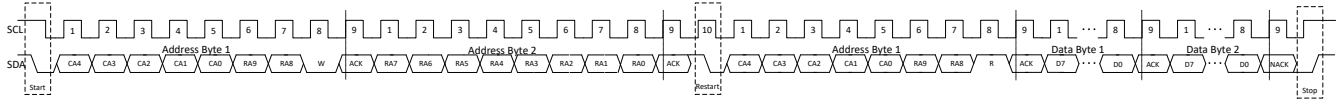


图 8-15. I<sup>2</sup>C Read Timing

### Multiple Devices Connection

The LP5862 enters into I<sup>2</sup>C mode if IFS is connected to GND. The ADDR0/1 pin is used to select the unique I<sup>2</sup>C follower address for each device. The SCL and SDA lines must each have a pullup resistor (4.7 K $\Omega$  for 400 KHz, 2 K $\Omega$  for 1 MHz) placed somewhere on the line and remain HIGH even when the bus is idle. VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO\_EN pin as possible. Up to four LP5862 follower devices can share the same I<sup>2</sup>C bus by the different ADDR configurations.

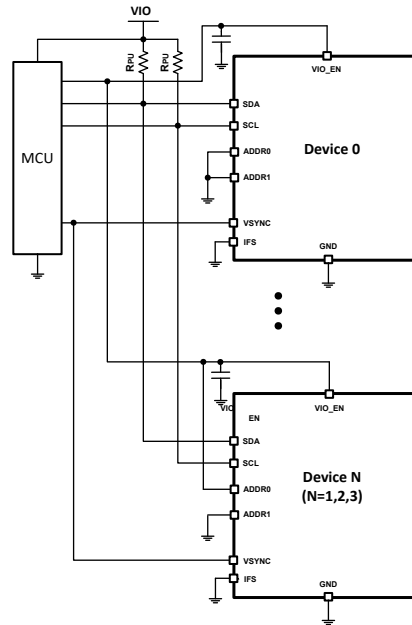


图 8-16. I<sup>2</sup>C Multiple Devices Connection

### SPI Interface

The LP5862 is compatible with SPI serial-bus specification, and it operates as a follower. The maximum frequency supported by LP5862 is 12 MHz.

### SPI Data Transactions

MISO output is normally in a high impedance state. When the follower-select pin SS for the device is active (low) the MISO output is pulled low for read only. During write cycle MISO stays in high-impedance state. The follower-select signal SS must be low during the cycle transmission. SS resets the interface when high. Data is clocked in on the rising edge of the SCLK clock signal, while data is clocked out on the falling edge of SCLK.

### SPI Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which contains 8 higher bits of the register address. The Address Byte 2 is started with 2 lower bits of the register address and 1 read and write bit. The auto-increment feature allows writing and reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

表 8-7. SPI Data Format

Address Byte 1	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	9 <sup>th</sup> bit	8 <sup>th</sup> bit	7 <sup>th</sup> bit	6 <sup>th</sup> bit	5 <sup>th</sup> bit	4 <sup>th</sup> bit	3 <sup>th</sup> bit	2 <sup>th</sup> bit
Address Byte 2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	1 <sup>th</sup> bit	0 <sup>th</sup> bit	R: 0 W: 1	Do not care				

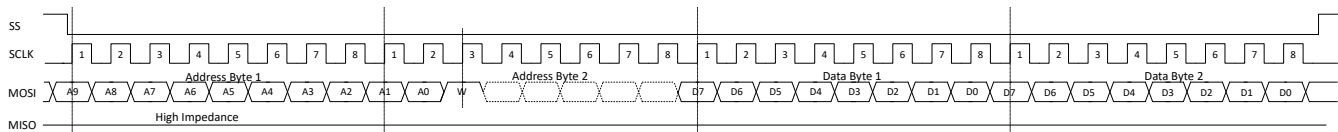


图 8-17. SPI Write Timing

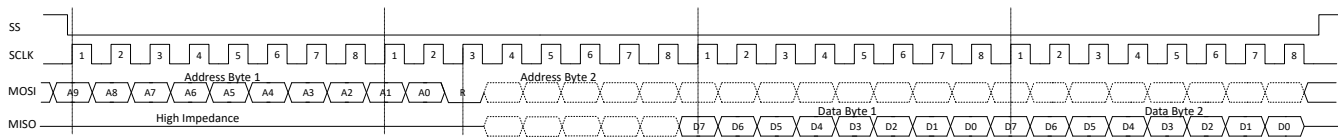


图 8-18. SPI Read Timing

**Multiple Devices Connection**

The device enters into SPI mode if IFS is pulled high to VIO through a pullup resistor (4.7 KΩ recommended). VIO\_EN can either be connected with VIO power supply or GPIO. TI suggests to put one 1-nF cap as closer to VIO\_EN pin as possible. In SPI mode host can address as many devices as there are follower select pins on host.

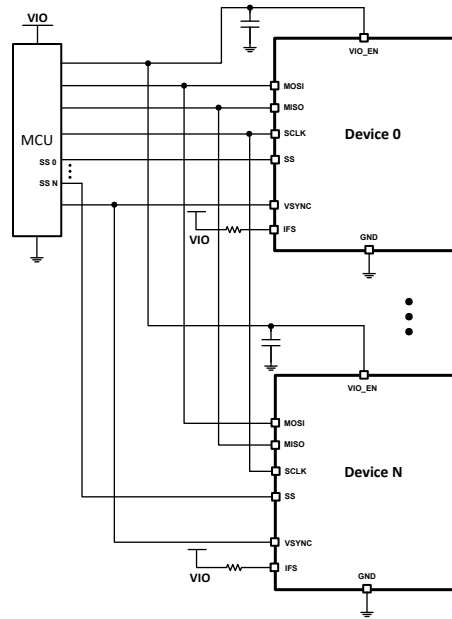


图 8-19. SPI Multiple Devices Connection

## 8.6 Register Maps

This section provides a summary of the register maps. For detailed register functions and descriptions, please refer to [LP5860 11x18 LED Matrix Driver Register Maps](#).

表 8-8. Register Section/Block Access Type Codes

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
<b>Write Type</b>		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

Register Acronym	Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
Chip_en	000h	R/W	Reserved							Chip_EN	00h
Dev_initial	001h	R/W	Reserved	Max_Line_Num				Data_Ref_Mode		PWM_Fre	5Eh
Dev_config1	002h	R/W	Reserved	Reserved	Reserved	Reserved	SW_BLK	PWM_Sc ale_Mode	PWM_Ph ase_Shift	CS_ON_ Shift	00h
Dev_config2	003h	R/W	Comp_Group3		Comp_Group2		Comp_Group1		LOD_rem oval	LSD_rem oval	00h
Dev_config3	004h	R/W	Down_Deghost		Up_Deghost		Maximum_Current			Up_Degh ost_enabl e	47h

<b>Global_bri</b>	005h	R/W	PWM_Global							FFh	
<b>Group0_bri</b>	006h	R/W	PWM_Group1							FFh	
<b>Group1_bri</b>	007h	R/W	PWM_Group2							FFh	
<b>Group2_bri</b>	008h	R/W	PWM_Group3							FFh	
<b>R_current_set</b>	009h	R/W	Reserved	CC_Group1						40h	
<b>G_current_set</b>	00Ah	R/W	Reserved	CC_Group2						40h	
<b>B_current_set</b>	00Bh	R/W	Reserved	CC_Group3						40h	
<b>Dot_grp_sel0</b>	00Ch	R/W	Dot L0-CS3 group		Dot L0-CS2 group		Dot L0-CS1 group		Dot L0-CS0 group		00h
<b>Dot_grp_sel1</b>	00Dh	R/W	Dot L0-CS7 group		Dot L0-CS6 group		Dot L0-CS5 group		Dot L0-CS4 group		00h
<b>Dot_grp_sel2</b>	00Eh	R/W	Dot L0-CS11 group		Dot L0-CS10 group		Dot L0-CS9 group		Dot L0-CS8 group		00h
<b>Dot_grp_sel3</b>	00Fh	R/W	Dot L0-CS15 group		Dot L0-CS14 group		Dot L0-CS13 group		Dot L0-CS12 group		00h
<b>Dot_grp_sel4</b>	010h	R/W	Reserved				Dot L0-CS17 group		Dot L0-CS16 group		00h
<b>Dot_grp_sel5</b>	011h	R/W	Dot L1-CS3 group		Dot L1-CS2 group		Dot L1-CS1 group		Dot L1-CS0 group		00h
<b>Dot_grp_sel6</b>	012h	R/W	Dot L1-CS7 group		Dot L1-CS6 group		Dot L1-CS5 group		Dot L1-CS4 group		00h
<b>Dot_grp_sel7</b>	013h	R/W	Dot L1-CS11 group		Dot L1-CS10 group		Dot L1-CS9 group		Dot L1-CS8 group		00h
<b>Dot_grp_sel8</b>	014h	R/W	Dot L1-CS15 group		Dot L1-CS14 group		Dot L1-CS13 group		Dot L1-CS12 group		00h
<b>Dot_grp_sel9</b>	015h	R/W	Reserved				Dot L1-CS17 group		Dot L1-CS16 group		00h
<b>Dot_onoff0</b>	043h	R/W	Dot L0-CS7 onoff	Dot L0-CS6 onoff	Dot L0-CS5 onoff	Dot L0-CS4 onoff	Dot L0-CS3 onoff	Dot L0-CS2 onoff	Dot L0-CS1 onoff	Dot L0-CS0 onoff	FFh
<b>Dot_onoff1</b>	044h	R/W	Dot L0-CS15 onoff	Dot L0-CS14 onoff	Dot L0-CS13 onoff	Dot L0-CS12 onoff	Dot L0-CS11 onoff	Dot L0-CS10 onoff	Dot L0-CS9 onoff	Dot L0-CS8 onoff	FFh
<b>Dot_onoff2</b>	045h	R/W	Reserved						Dot L0-CS17 onoff	Dot L0-CS16 onoff	03h
<b>Dot_onoff3</b>	046h	R/W	Dot L1-CS7 onoff	Dot L1-CS6 onoff	Dot L1-CS5 onoff	Dot L1-CS4 onoff	Dot L1-CS3 onoff	Dot L1-CS2 onoff	Dot L1-CS1 onoff	Dot L1-CS0 onoff	FFh
<b>Dot_onoff4</b>	047h	R/W	Dot L1-CS15 onoff	Dot L1-CS14 onoff	Dot L1-CS13 onoff	Dot L1-CS12 onoff	Dot L1-CS11 onoff	Dot L1-CS10 onoff	Dot L1-CS9 onoff	Dot L1-CS8 onoff	FFh
<b>Dot_onoff5</b>	048h	R/W	Reserved						Dot L1-CS17 onoff	Dot L1-CS16 onoff	03h
<b>Fault_state</b>	064h	R	Reserved						Global_L OD	Global_L SD	00h
<b>Dot_lod0</b>	065h	R	Dot L0-CS7 LOD	Dot L0-CS6 LOD	Dot L0-CS5 LOD	Dot L0-CS4 LOD	Dot L0-CS3 LOD	Dot L0-CS2 LOD	Dot L0-CS1 LOD	Dot L0-CS0 LOD	00h
<b>Dot_lod1</b>	066h	R	Dot L0-CS15 LOD	Dot L0-CS14 LOD	Dot L0-CS13 LOD	Dot L0-CS12 LOD	Dot L0-CS11 LOD	Dot L0-CS10 LOD	Dot L0-CS9 LOD	Dot L0-CS8 LOD	00h
<b>Dot_lod2</b>	067h	R	Reserved						Dot L0-CS17 LOD	Dot L0-CS16 LOD	00h
<b>Dot_lod3</b>	068h	R	Dot L1-CS7 LOD	Dot L1-CS6 LOD	Dot L1-CS5 LOD	Dot L1-CS4 LOD	Dot L1-CS3 LOD	Dot L1-CS2 LOD	Dot L1-CS1 LOD	Dot L1-CS0 LOD	00h
<b>Dot_lod4</b>	069h	R	Dot L1-CS15 LOD	Dot L1-CS14 LOD	Dot L1-CS13 LOD	Dot L1-CS12 LOD	Dot L1-CS11 LOD	Dot L1-CS10 LOD	Dot L1-CS9 LOD	Dot L1-CS8 LOD	00h
<b>Dot_lod5</b>	06Ah	R	Reserved						Dot L1-CS17 LOD	Dot L1-CS16 LOD	00h
<b>Dot_lsd0</b>	086h	R	Dot L0-CS7 LSD	Dot L0-CS6 LSD	Dot L0-CS5 LSD	Dot L0-CS4 LSD	Dot L0-CS3 LSD	Dot L0-CS2 LSD	Dot L0-CS1 LSD	Dot L0-CS0 LSD	00h

<b>Dot_Isd1</b>	087h	R	Dot L0- CS15 LSD	Dot L0- CS14 LSD	Dot L0- CS13 LSD	Dot L0- CS12 LSD	Dot L0- CS11 LSD	Dot L0- CS10 LSD	Dot L0- CS9 LSD	Dot L0- CS8 LSD	00h
<b>Dot_Isd2</b>	088h	R	Reserved						Dot L0- CS17 LSD	Dot L0- CS16 LSD	00h
<b>Dot_Isd3</b>	089h	R	Dot L1- CS7 LSD	Dot L1- CS6 LSD	Dot L1- CS5 LSD	Dot L1- CS4 LSD	Dot L1- CS3 LSD	Dot L1- CS2 LSD	Dot L1- CS1 LSD	Dot L1- CS0 LSD	00h
<b>Dot_Isd4</b>	08Ah	R	Dot L1- CS15 LSD	Dot L1- CS14 LSD	Dot L1- CS13 LSD	Dot L1- CS12 LSD	Dot L1- CS11 LSD	Dot L1- CS10 LSD	Dot L1- CS9 LSD	Dot L1- CS8 LSD	00h
<b>Dot_Isd5</b>	08Bh	R	Reserved						Dot L1- CS17 LSD	Dot L1- CS16 LSD	00h
<b>LOD_clear</b>	0A7h	W	Reserved				LOD_Clear				00h
<b>LSD_clear</b>	0A8h	W	Reserved				LSD_Clear				00h
<b>Reset</b>	0A9h	W	Reset								00h
<b>DC0</b>	100h	R/W	LED dot current setting for Dot L0-CS0								80h
<b>DC1</b>	101h	R/W	LED dot current setting for Dot L0-CS1								80h
<b>DC2</b>	102h	R/W	LED dot current setting for Dot L0-CS2								80h
<b>DC3</b>	103h	R/W	LED dot current setting for Dot L0-CS3								80h
<b>DC4</b>	104h	R/W	LED dot current setting for Dot L0-CS4								80h
<b>DC5</b>	105h	R/W	LED dot current setting for Dot L0-CS5								80h
<b>DC6</b>	106h	R/W	LED dot current setting for Dot L0-CS6								80h
<b>DC7</b>	107h	R/W	LED dot current setting for Dot L0-CS7								80h
<b>DC8</b>	108h	R/W	LED dot current setting for Dot L0-CS8								80h
<b>DC9</b>	109h	R/W	LED dot current setting for Dot L0-CS9								80h
<b>DC10</b>	10Ah	R/W	LED dot current setting for Dot L0-CS10								80h
<b>DC11</b>	10Bh	R/W	LED dot current setting for Dot L0-CS11								80h
<b>DC12</b>	10Ch	R/W	LED dot current setting for Dot L0-CS12								80h
<b>DC13</b>	10Dh	R/W	LED dot current setting for Dot L0-CS13								80h
<b>DC14</b>	10Eh	R/W	LED dot current setting for Dot L0-CS14								80h
<b>DC15</b>	10Fh	R/W	LED dot current setting for Dot L0-CS15								80h
<b>DC16</b>	110h	R/W	LED dot current setting for Dot L0-CS16								80h
<b>DC17</b>	111h	R/W	LED dot current setting for Dot L0-CS17								80h
<b>DC18</b>	112h	R/W	LED dot current setting for Dot L1-CS0								80h
<b>DC19</b>	113h	R/W	LED dot current setting for Dot L1-CS1								80h
<b>DC20</b>	114h	R/W	LED dot current setting for Dot L1-CS2								80h
<b>DC21</b>	115h	R/W	LED dot current setting for Dot L1-CS3								80h
<b>DC22</b>	116h	R/W	LED dot current setting for Dot L1-CS4								80h
<b>DC23</b>	117h	R/W	LED dot current setting for Dot L1-CS5								80h
<b>DC24</b>	118h	R/W	LED dot current setting for Dot L1-CS6								80h
<b>DC25</b>	119h	R/W	LED dot current setting for Dot L1-CS7								80h
<b>DC26</b>	11Ah	R/W	LED dot current setting for Dot L1-CS8								80h
<b>DC27</b>	11Bh	R/W	LED dot current setting for Dot L1-CS9								80h
<b>DC28</b>	11Ch	R/W	LED dot current setting for Dot L1-CS10								80h
<b>DC29</b>	11Dh	R/W	LED dot current setting for Dot L1-CS11								80h
<b>DC30</b>	11Eh	R/W	LED dot current setting for Dot L1-CS12								80h
<b>DC31</b>	11Fh	R/W	LED dot current setting for Dot L1-CS13								80h
<b>DC32</b>	120h	R/W	LED dot current setting for Dot L1-CS14								80h

<b>DC33</b>	121h	R/W	LED dot current setting for Dot L1-CS15	80h
<b>DC34</b>	122h	R/W	LED dot current setting for Dot L1-CS16	80h
<b>DC35</b>	123h	R/W	LED dot current setting for Dot L1-CS17	80h
<b>pwm_bri0</b>	200h	R/W	8-bits PWM for Dot L0-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS0	00h
<b>pwm_bri1</b>	201h	R/W	8-bits PWM for Dot L0-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS0	00h
<b>pwm_bri2</b>	202h	R/W	8-bits PWM for Dot L0-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS1	00h
<b>pwm_bri3</b>	203h	R/W	8-bits PWM for Dot L0-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS1	00h
<b>pwm_bri4</b>	204h	R/W	8-bits PWM for Dot L0-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS2	00h
<b>pwm_bri5</b>	205h	R/W	8-bits PWM for Dot L0-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS2	00h
<b>pwm_bri6</b>	206h	R/W	8-bits PWM for Dot L0-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS3	00h
<b>pwm_bri7</b>	207h	R/W	8-bits PWM for Dot L0-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS3	00h
<b>pwm_bri8</b>	208h	R/W	8-bits PWM for Dot L0-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS4	00h
<b>pwm_bri9</b>	209h	R/W	8-bits PWM for Dot L0-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS4	00h
<b>pwm_bri10</b>	20Ah	R/W	8-bits PWM for Dot L0-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS5	00h
<b>pwm_bri11</b>	20Bh	R/W	8-bits PWM for Dot L0-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS5	00h
<b>pwm_bri12</b>	20Ch	R/W	8-bits PWM for Dot L0-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS6	00h
<b>pwm_bri13</b>	20Dh	R/W	8-bits PWM for Dot L0-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS6	00h
<b>pwm_bri14</b>	20Eh	R/W	8-bits PWM for Dot L0-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS7	00h
<b>pwm_bri15</b>	20Fh	R/W	8-bits PWM for Dot L0-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS7	00h
<b>pwm_bri16</b>	210h	R/W	8-bits PWM for Dot L0-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS8	00h
<b>pwm_bri17</b>	211h	R/W	8-bits PWM for Dot L0-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS8	00h
<b>pwm_bri18</b>	212h	R/W	8-bits PWM for Dot L1-CS0 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS9	00h
<b>pwm_bri19</b>	213h	R/W	8-bits PWM for Dot L1-CS1 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS9	00h
<b>pwm_bri20</b>	214h	R/W	8-bits PWM for Dot L1-CS2 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS10	00h
<b>pwm_bri21</b>	215h	R/W	8-bits PWM for Dot L1-CS3 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS10	00h
<b>pwm_bri22</b>	216h	R/W	8-bits PWM for Dot L1-CS4 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS11	00h
<b>pwm_bri23</b>	217h	R/W	8-bits PWM for Dot L1-CS5 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS11	00h
<b>pwm_bri24</b>	218h	R/W	8-bits PWM for Dot L1-CS6 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS12	00h
<b>pwm_bri25</b>	219h	R/W	8-bits PWM for Dot L1-CS7 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS12	00h
<b>pwm_bri26</b>	21Ah	R/W	8-bits PWM for Dot L1-CS8 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS13	00h
<b>pwm_bri27</b>	21Bh	R/W	8-bits PWM for Dot L1-CS9 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS13	00h
<b>pwm_bri28</b>	21Ch	R/W	8-bits PWM for Dot L1-CS10 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS14	00h
<b>pwm_bri29</b>	21Dh	R/W	8-bits PWM for Dot L1-CS11 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS14	00h
<b>pwm_bri30</b>	21Eh	R/W	8-bits PWM for Dot L1-CS12 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS15	00h
<b>pwm_bri31</b>	21Fh	R/W	8-bits PWM for Dot L1-CS13 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS15	00h
<b>pwm_bri32</b>	220h	R/W	8-bits PWM for Dot L1-CS14 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS16	00h
<b>pwm_bri33</b>	221h	R/W	8-bits PWM for Dot L1-CS15 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS16	00h
<b>pwm_bri34</b>	222h	R/W	8-bits PWM for Dot L1-CS16 OR 16-bits PWM lower 8 bits [7:0] for Dot L0-CS17	00h
<b>pwm_bri35</b>	223h	R/W	8-bits PWM for Dot L1-CS17 OR 16-bits PWM higher 8 bits [15:8] for Dot L0-CS17	00h
<b>pwm_bri36</b>	224h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS0	00h
<b>pwm_bri37</b>	225h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS0	00h
<b>pwm_bri38</b>	226h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS1	00h
<b>pwm_bri39</b>	227h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS1	00h
<b>pwm_bri40</b>	228h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS2	00h
<b>pwm_bri41</b>	229h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS2	00h
<b>pwm_bri42</b>	22Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS3	00h
<b>pwm_bri43</b>	22Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS3	00h

<b>pwm_bri44</b>	22Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS4	00h
<b>pwm_bri45</b>	22Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS4	00h
<b>pwm_bri46</b>	22Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS5	00h
<b>pwm_bri47</b>	22Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS5	00h
<b>pwm_bri48</b>	230h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS6	00h
<b>pwm_bri49</b>	231h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS6	00h
<b>pwm_bri50</b>	232h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS7	00h
<b>pwm_bri51</b>	233h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS7	00h
<b>pwm_bri52</b>	234h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS8	00h
<b>pwm_bri53</b>	235h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS8	00h
<b>pwm_bri54</b>	236h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS9	00h
<b>pwm_bri55</b>	237h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS9	00h
<b>pwm_bri56</b>	238h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS10	00h
<b>pwm_bri57</b>	239h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS10	00h
<b>pwm_bri58</b>	23Ah	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS11	00h
<b>pwm_bri59</b>	23Bh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS11	00h
<b>pwm_bri60</b>	23Ch	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS12	00h
<b>pwm_bri61</b>	23Dh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS12	00h
<b>pwm_bri62</b>	23Eh	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS13	00h
<b>pwm_bri63</b>	23Fh	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS13	00h
<b>pwm_bri64</b>	240h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS14	00h
<b>pwm_bri65</b>	241h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS14	00h
<b>pwm_bri66</b>	242h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS15	00h
<b>pwm_bri67</b>	243h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS15	00h
<b>pwm_bri68</b>	244h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS16	00h
<b>pwm_bri69</b>	245h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS16	00h
<b>pwm_bri70</b>	246h	R/W	16-bits PWM lower 8 bits [7:0] for Dot L1-CS17	00h
<b>pwm_bri71</b>	247h	R/W	16-bits PWM higher 8 bits [15:8] for Dot L1-CS17	00h

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The LP5862 integrates 18 constant current sinks with 2 switching FETs and one LP5862 can drive up to 36 LED dots or 12 RGB pixels and achieve great dimming effect. In smart home, gaming keyboards, and other human-machine interaction applications, the device can greatly improve user experience with small amount of components.

### 9.2 Typical Application

#### 9.2.1 Application

图 9-1 shows an example of typical application, which uses one LP5862 to drive 12 common-anode RGB LEDs through I<sup>2</sup>C communication.

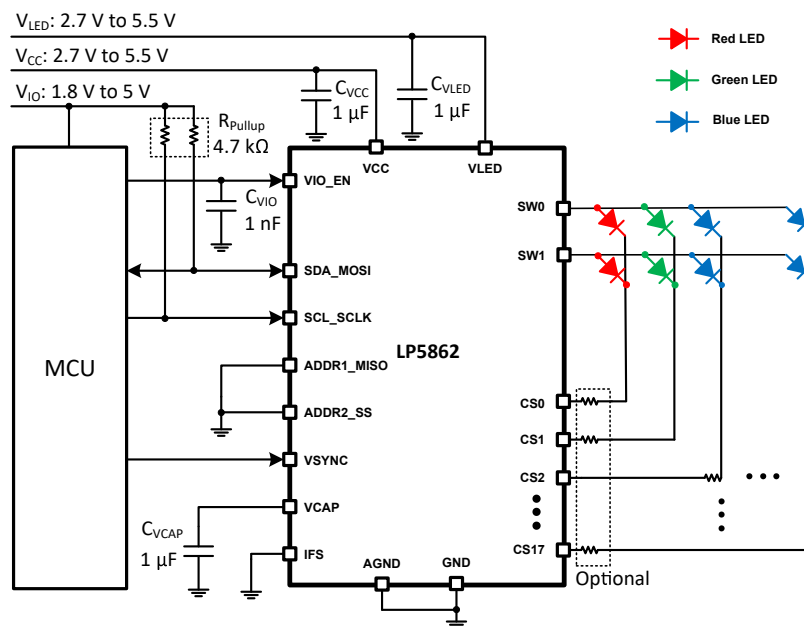


图 9-1. Typical Application - LP5862 Driving 36 RGB LEDs (12 LED Dots)

#### 9.2.2 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
VCC / VIO	3.3 V
VLED	5 V
RGB LED count	12
Scan number	2
Interface	I <sup>2</sup> C
LED maximum average current (red, green, blue)	22 mA, 16.5 mA, 11 mA
LED maximum peak current (red, green, blue)	44 mA, 33 mA, 22 mA

### 9.2.3 Detailed Design Procedure

LP5862 requires an external capacitor  $C_{V_{CAP}}$ , whose value is  $1 \mu F$  connected from  $V_{CAP}$  to GND for proper operation of internal LDO. The external capacitor must be placed as close to the device as possible.

TI recommends  $1-\mu F$  capacitors be placed between  $VCC / V_{LED}$  with GND, and  $1-nF$  capacitor placed between  $VIO$  with GND. Place the capacitors as close to the device as possible.

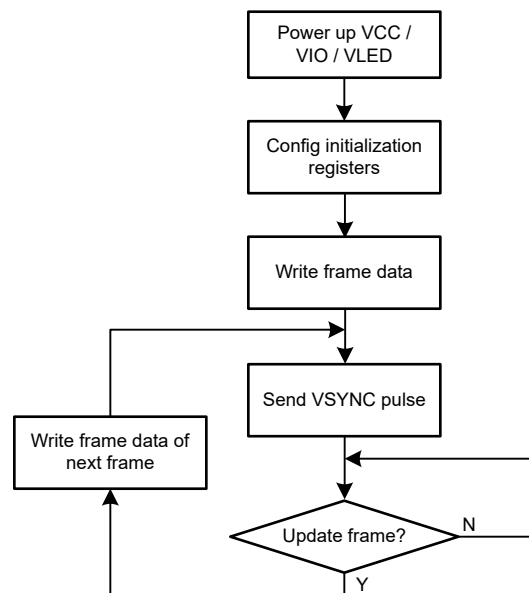
Pullup resistors  $R_{pull-up}$  are requirement for SCL and SDA when using  $I^2C$  as communication method. In typical applications, TI recommends  $1.8-k\Omega$  to  $4.7-k\Omega$  resistors.

To decrease thermal dissipation from device to ambient, resistors  $R_{CS}$  can optionally be placed in serial with the LED. Voltage drop on these resistors must leave enough margins for  $V_{SAT}$  to ensure the device works normally.

### 9.2.4 Program Procedure

When selecting data refresh Mode 1, outputs are refreshed instantly after data is received.

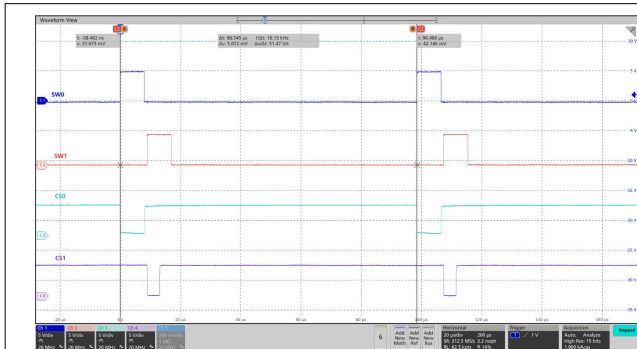
When selecting data refresh Mode 2 and 3,  $V_{SYNC}$  signal is required for synchronized display. Programming flow is showed as [图 9-2](#). To display full pixel of last frame,  $V_{SYNC}$  pulse must be sent to the device after the end of last PWM. Time between two pulses  $t_{SYNC}$  must be larger than the whole PWM time of all Dots  $t_{frame}$ . Common selection like 60 Hz, 90 Hz, 120 Hz or even higher refresh frequency an be supported. High pulse width longer than  $t_{SYNC\_H}$  is required at the beginning of each  $V_{SYNC}$  frame, and data must not be write to PWM registers during high pulse width.



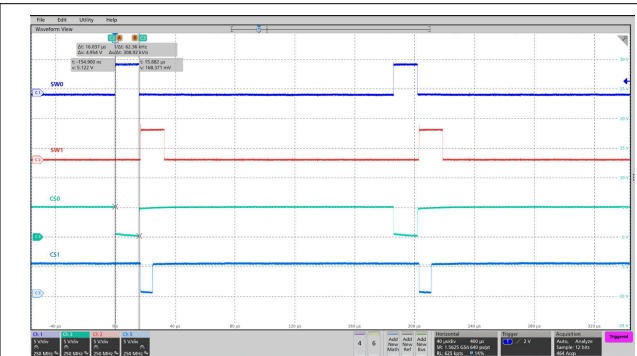
**图 9-2. Program Procedure**

### 9.2.5 Application Performance Plots

The following figures show the application performance plots.

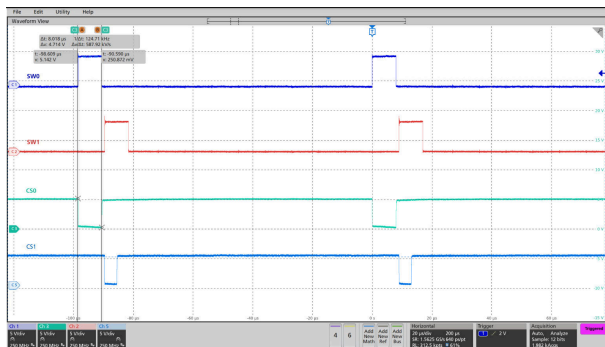


**图 9-3. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



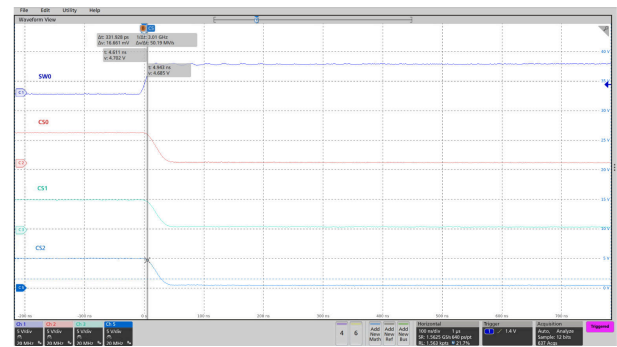
PWM frequency = 62.5 kHz

**图 9-4. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



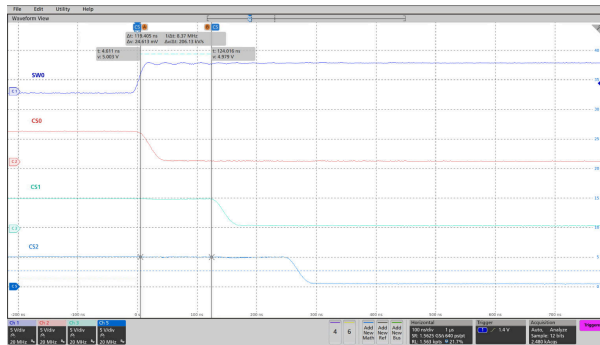
PWM frequency = 125 kHz

**图 9-5. Scan Lines and Current Sinks Waveforms of SW0, SW1, CS0, CS1**



PWM\_Phase\_Shift = 0h

**图 9-6. PWM Phase Shift Disabled**



PWM\_Phase\_Shift = 1h

**图 9-7. PWM Phase Shift Enabled**

## 10 Power Supply Recommendations

### VDD Input Supply Recommendations

LP5862 is designed to operate from a 2.7-V to 5.5-V VDD voltage supply. This input supply must be well regulated and be able to provide the peak current required by the LED matrix. The resistance of the VDD supply rail must be low enough such that the input current transient does not cause the LP5862 VDD supply voltage to drop below the maximum POR voltage.

### VLED Input Supply Recommendations

LP5862 is designed to operate with a 2.7-V to 5.5-V VLED voltage supply. The VLED supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop, under load transients like start-up or rapid brightness change. The resistance of the input supply rail must be low enough so that the input current transient does not cause the VLED supply voltage to drop below LED  $V_f + V_{SAT}$  voltage.

### VIO Input Supply Recommendations

LP5862 is designed to operate with a 1.65-V to 5.5-V VIO\_EN voltage supply. The VIO\_EN supply must be well regulated and able to provide the peak current required by the LED configuration without voltage drop under load transients like start-up or rapid brightness change.

## 11 Layout

### 11.1 Layout Guidelines

the below guidelines for layout design can help to get a better on-board performance.

- The decoupling capacitors  $C_{VCC}$  and  $C_{VLED}$  for power supply must be close to the chip to have minimized the impact of high-frequency noise and ripple from power.  $C_{VCAP}$  for internal LDO must be put as close to chip as possible. GND plane connections to  $C_{VLED}$  and GND pins must be on TOP layer copper with multiple vias connecting to system ground plane.  $C_{VIO}$  for internal enable block also must be put as close to chip as possible.
- The exposed thermal pad must be well soldered to the board, which can have better mechanical reliability. This action can optimize heat transfer so that increasing thermal performance. AGND pin must be connected to thermal pad and system ground.
- The major heat flow path from the package to the ambient is through copper on the PCB. Several methods can help thermal performance. Below exposed thermal pad of IC, putting much vias through the PCB to other ground layer can dissipate more heat. Maximizing the copper coverage on the PCB can increase the thermal conductivity of the board.
- Low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of VLED - SWx must be short and wide and avoid parallel wiring and narrow trace. Transient current in SWx pins is much larger than CSy pins, so that trace for SWx must be wider than CSy.

### 11.2 Layout Example

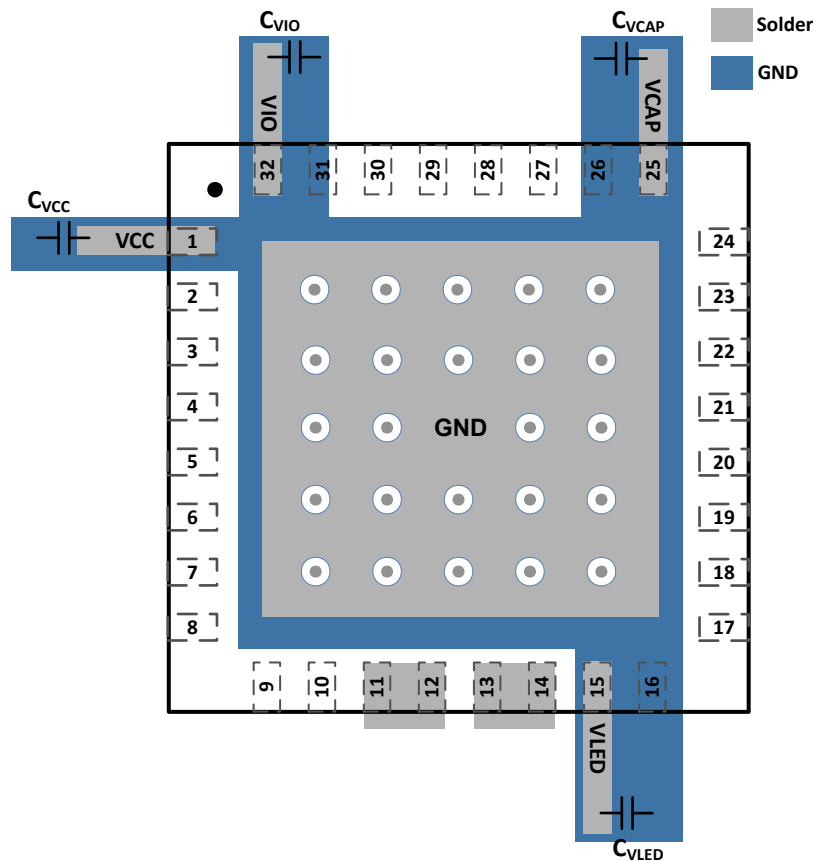


图 11-1. LP5862 Layout Example

## 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 12.1 Documentation Support

#### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 12.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

#### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5862DBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5862DBTR	<a href="#">Samples</a>
LP5862RSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LP5862	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## GENERIC PACKAGE VIEW

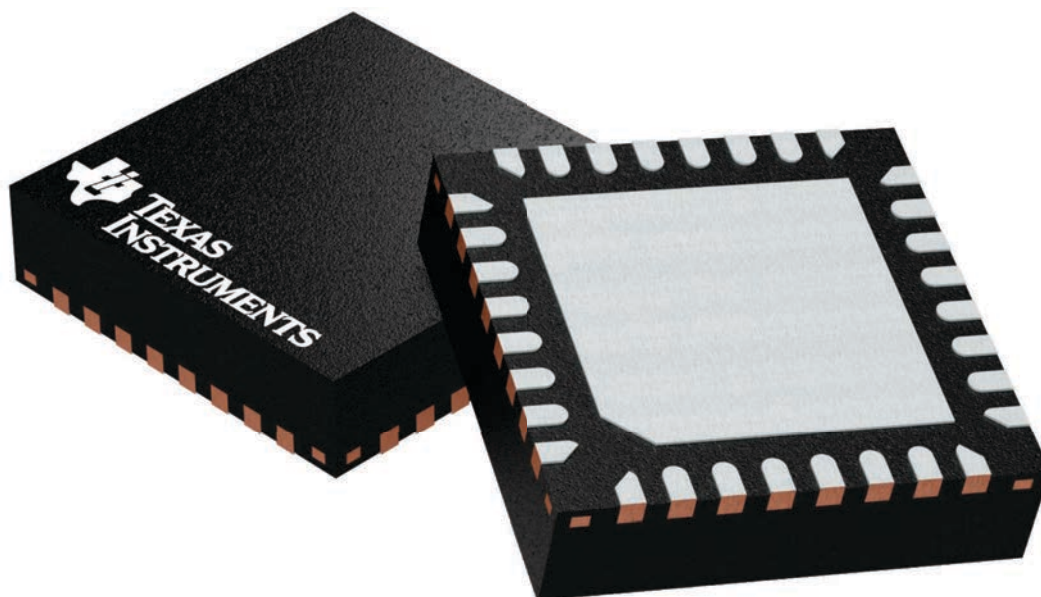
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

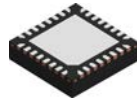
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

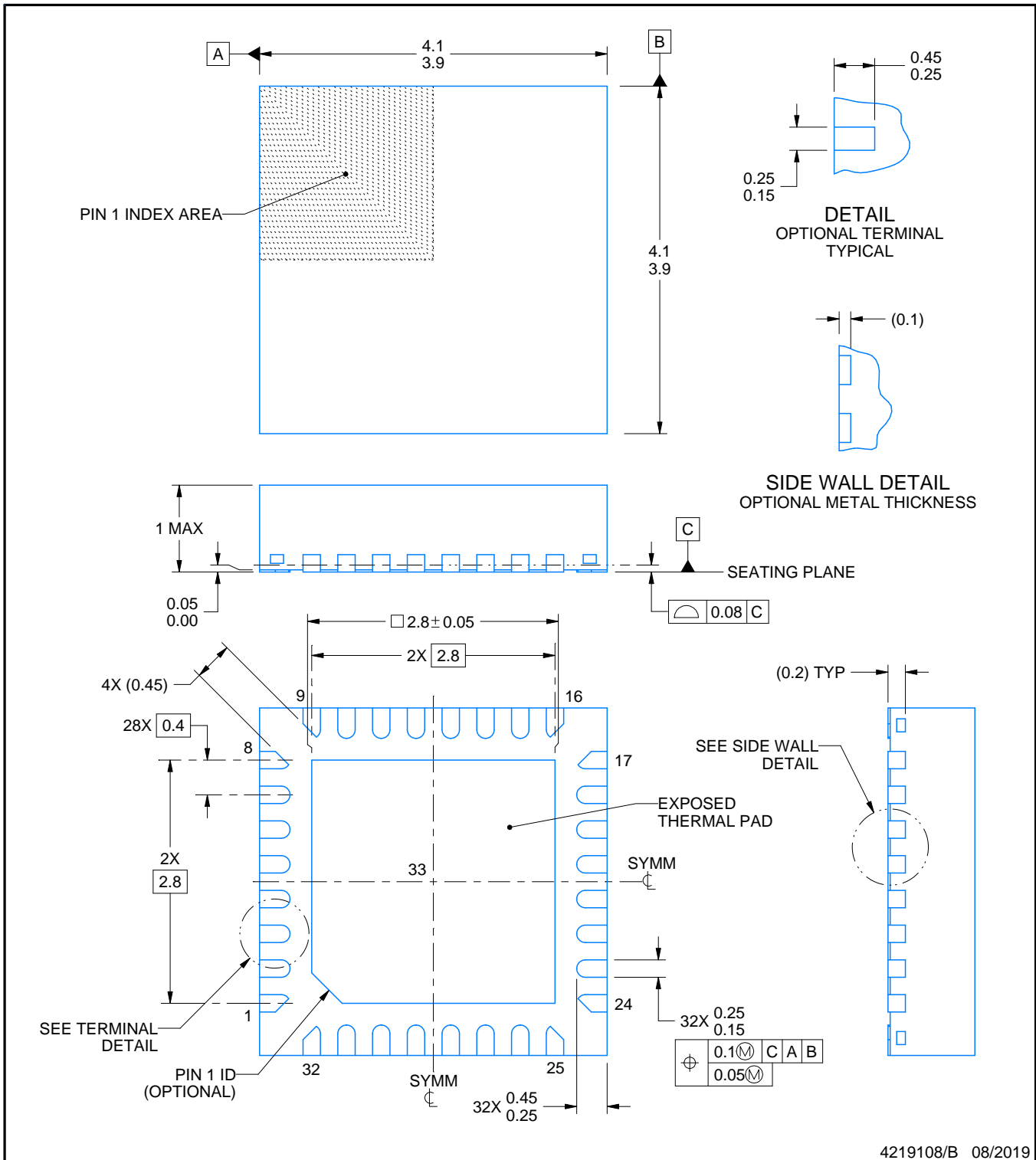
# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219108/B 08/2019

### NOTES:

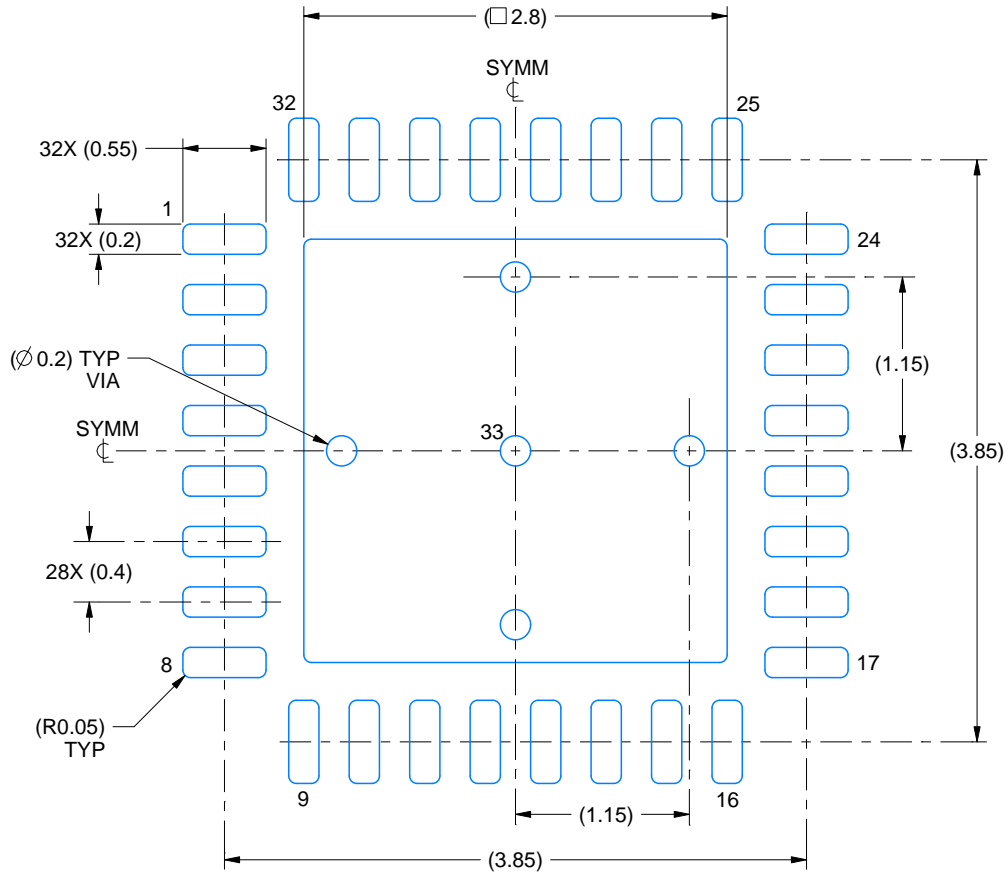
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

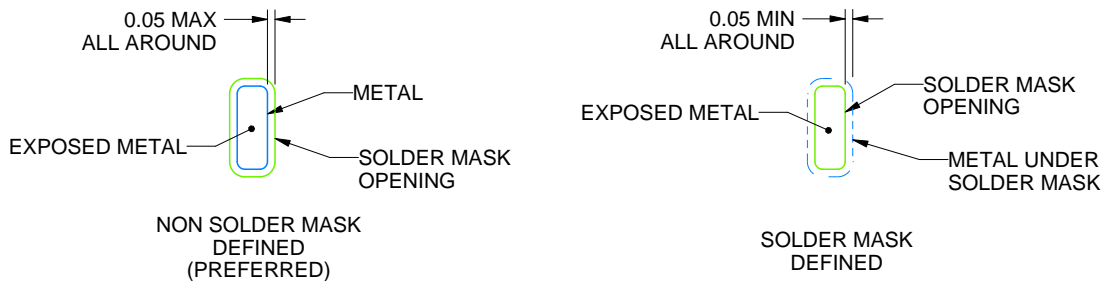
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

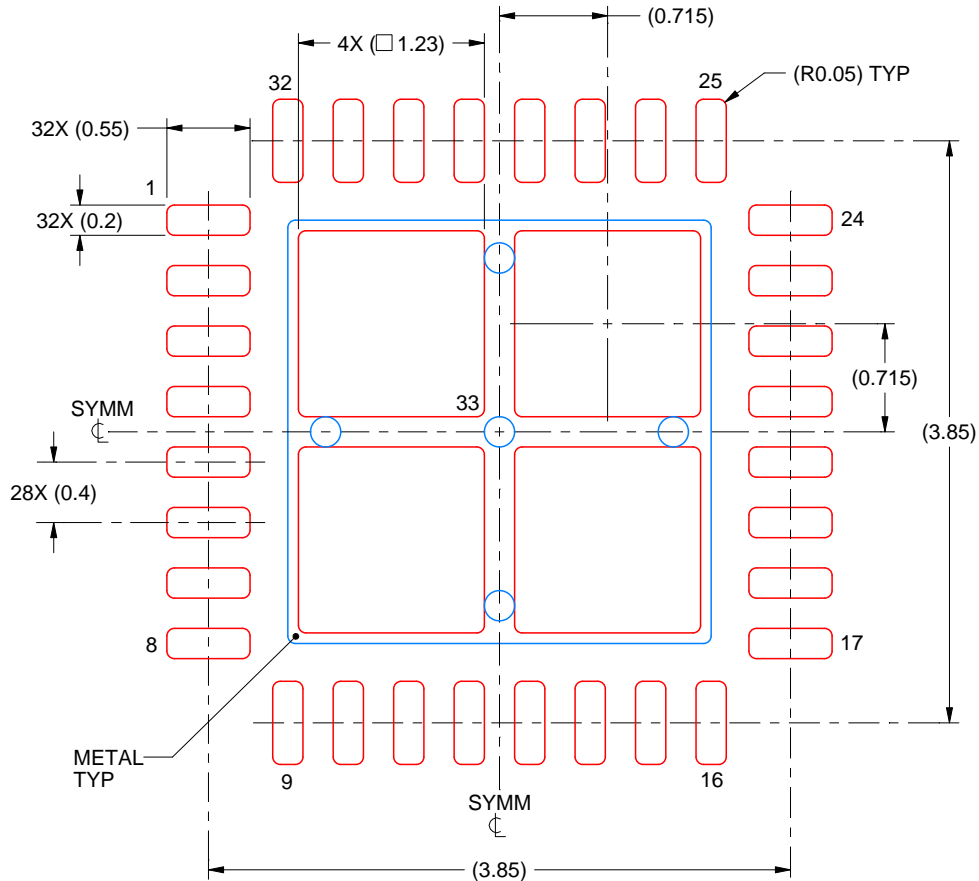
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

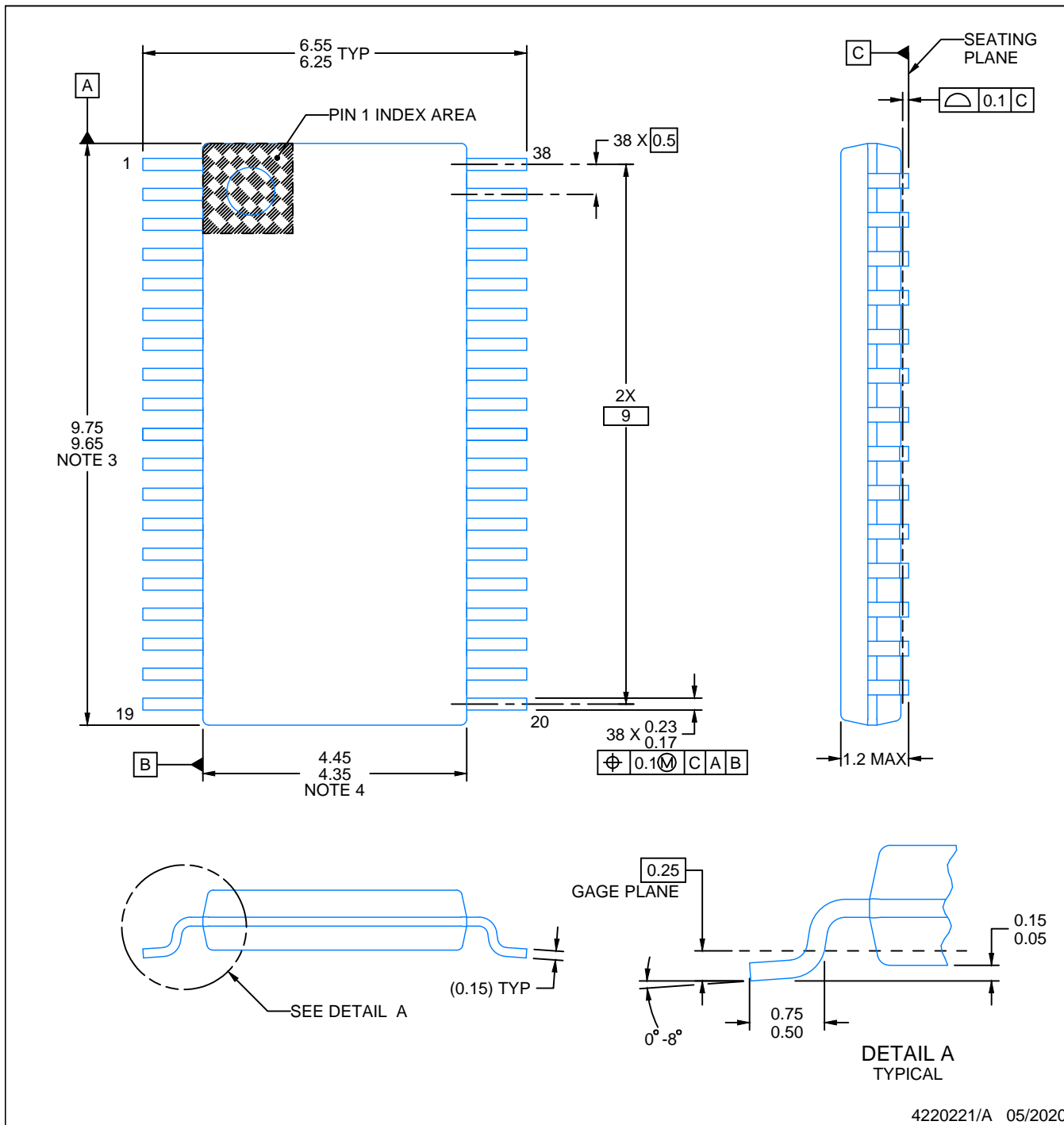
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

**DBT0038A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



**NOTES:**

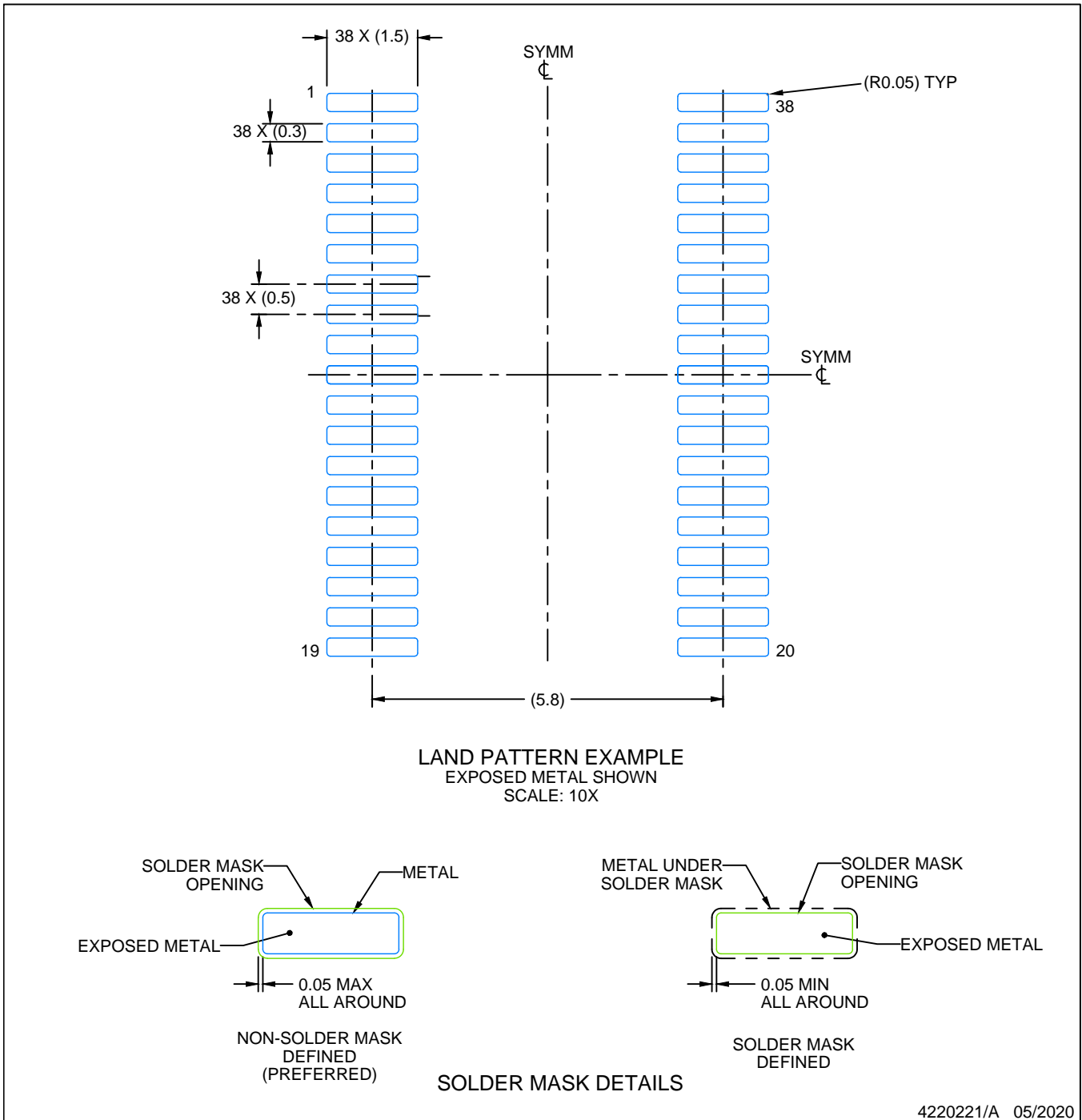
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

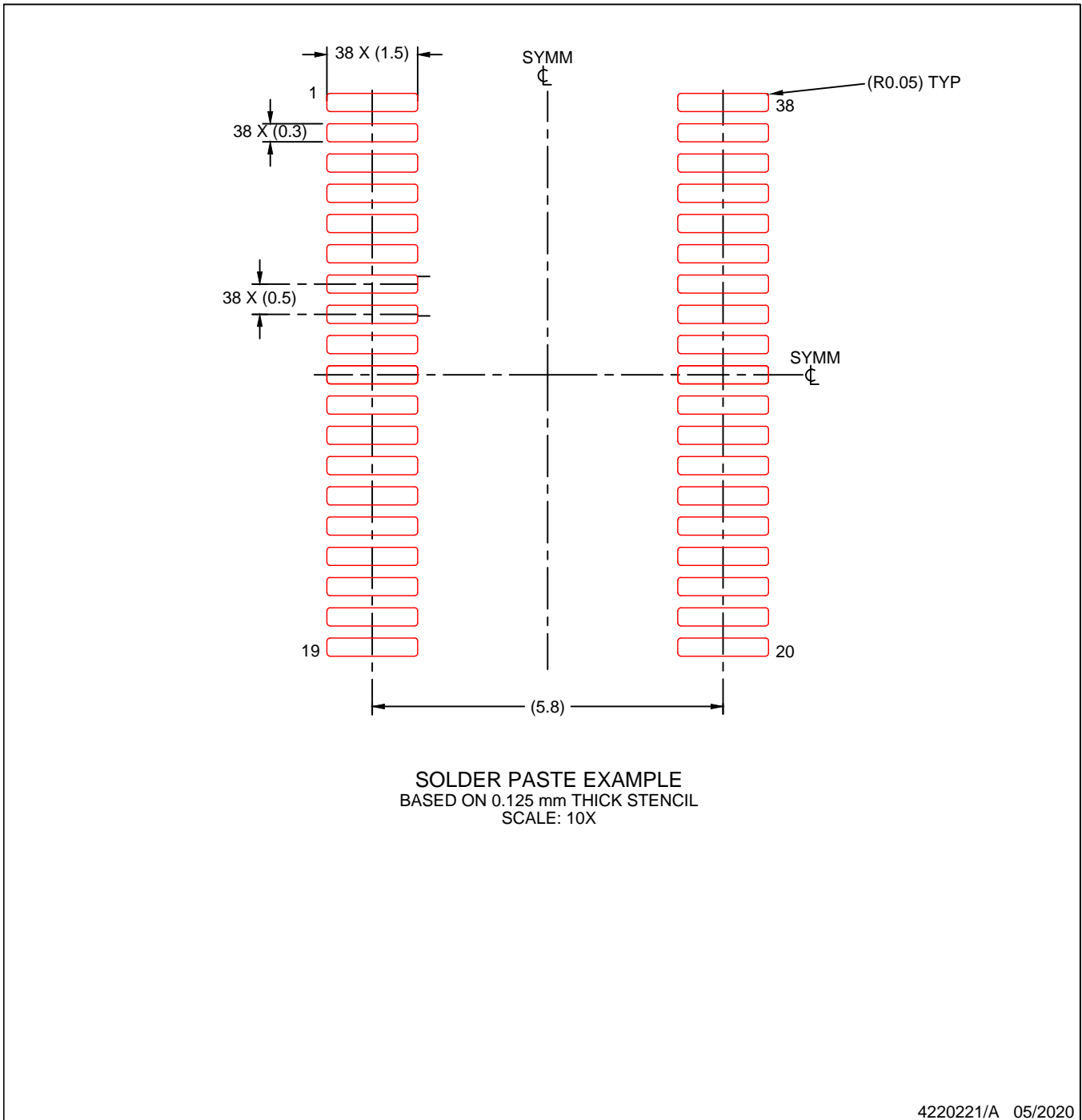
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBT0038A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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