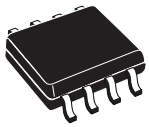
STS5DNF60L

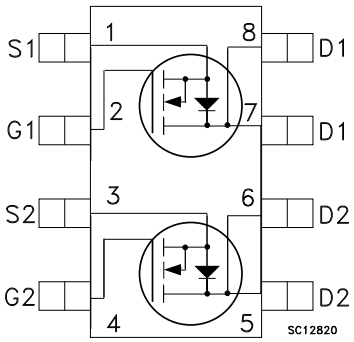
Automotive-grade dual N-channel 60 V, 0.035 Ω typ., 5 A STripFET™ II Power MOSFET in an SO-8 package

Datasheet - production data



SO-8

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS5DNF60L	60 V	0.045 Ω	5 A

- AEC-Q101 qualified
- Low threshold drive

Applications

- Switching applications

Description

This Power MOSFET has been developed using the STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packing
STS5DNF60L	5DF60L	SO-8	Tape and reel

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate- source voltage	± 15	V
I_D	Drain current (continuous) at T_{pcb} = 25 °C	5	A
I_D	Drain current (continuous) at T_{pcb}= 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}(2)	Total dissipation at T_{pcb} = 25 °C	2	W
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area
2. P_{TOT} = 1.6 W for single operation

Table 3. Thermal data

Simbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb (1)	62.5	°C/W

1. When mounted on 1 inch² FR-4 board, 2 Oz Cu, t ≤ 10 s, dual operation

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 T_C = 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 15 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2 A		0.035	0.045	Ω
		V_{GS} = 4.5 V, I_D = 2 A		0.045	0.055	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 25 V, I_D =2 A	-	25	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1030	-	pF
C_{oss}	Output capacitance			140		pF
C_{rss}	Reverse transfer capacitance			40		pF
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 4 A, V_{GS} = 4.5 V (see *Figure 13*)	-	15	-	nC
Q_{gs}	Gate-source charge			4		nC
Q_{gd}	Gate-drain charge			4		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	V_{DD} = 30 V, I_D = 2.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12* and *Figure 17*)		15		ns
t_r	Rise time		-	28	-	ns
$t_{d(off)}$	Turn-off delay time			45		ns
t_f	Fall time			10		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)				16	A
V_{SD} (2)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/µs V_{DD} = 20 V (see *Figure 14*)	-	85		ns
Q_{rr}	Reverse recovery charge			85		nC
I_{RRM}	Reverse recovery current			2		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

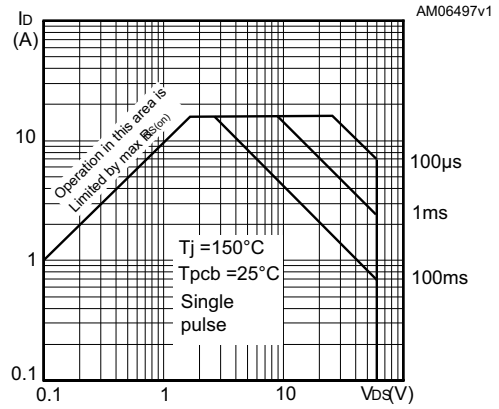


Figure 3. Thermal impedance

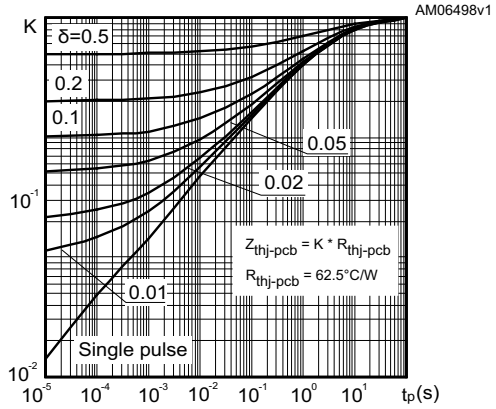


Figure 4. Output characterisics

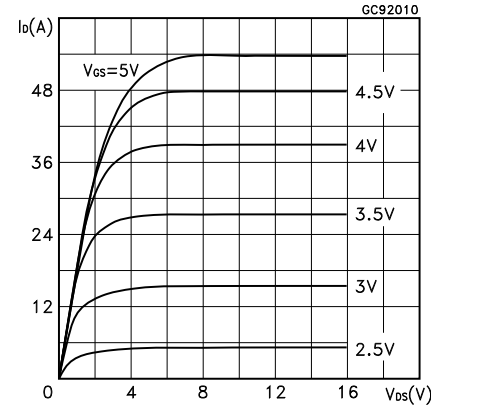


Figure 5. Transfer characteristics

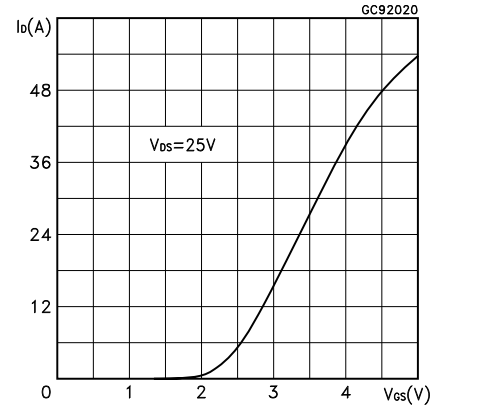


Figure 6. Source-drain diode forward characteristics

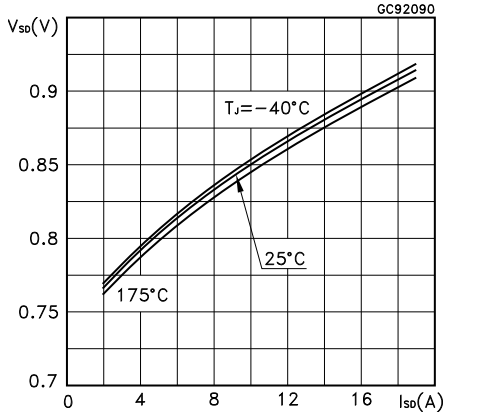


Figure 7. Static drain-source on resistance

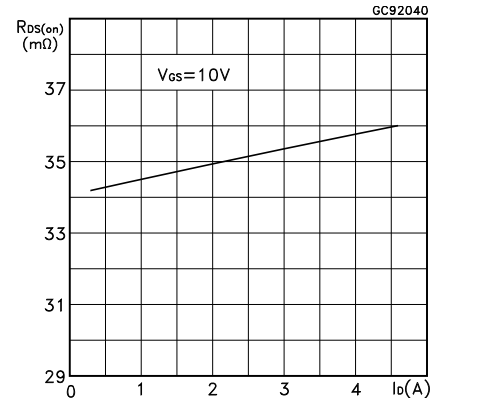


Figure 8. Gate charge vs gate-source voltage

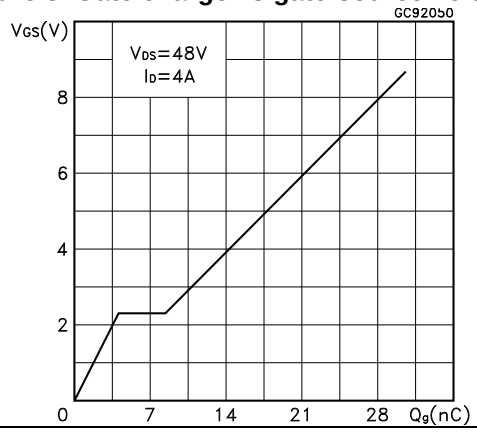


Figure 9. Capacitance variations

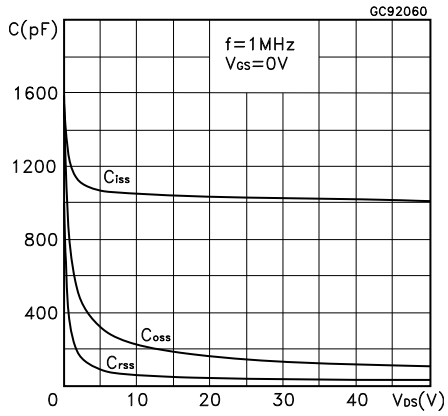


Figure 10. Normalized gate threshold voltage vs temperature

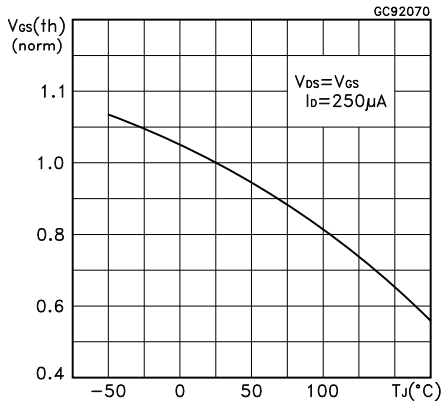
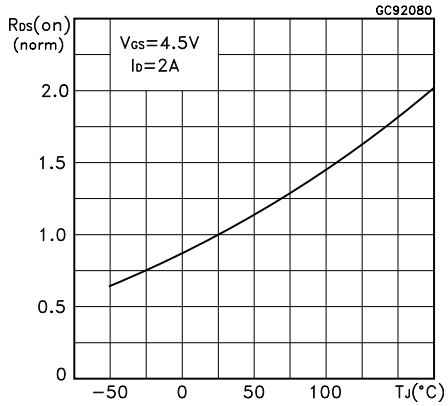


Figure 11. Normalized on resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

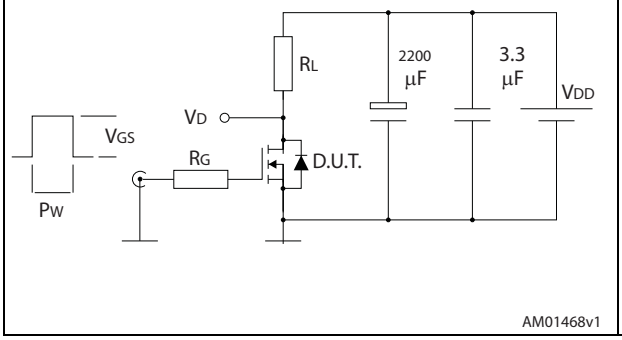


Figure 13. Gate charge test circuit

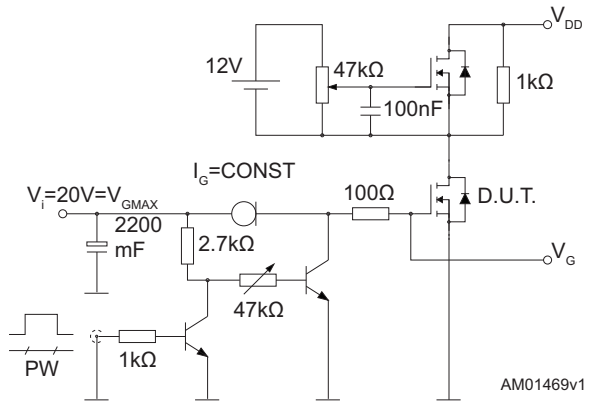


Figure 14. Test circuit for inductive load switching and diode recovery times

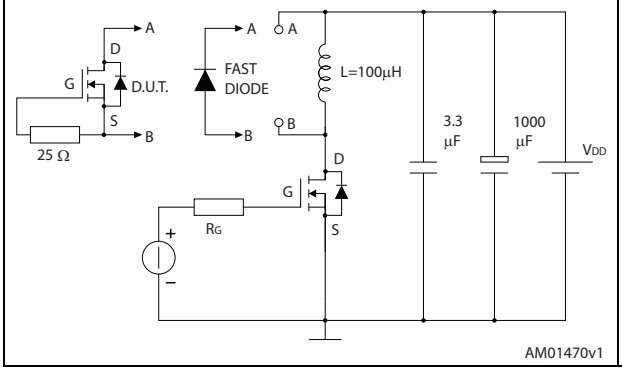


Figure 15. Unclamped Inductive load test circuit

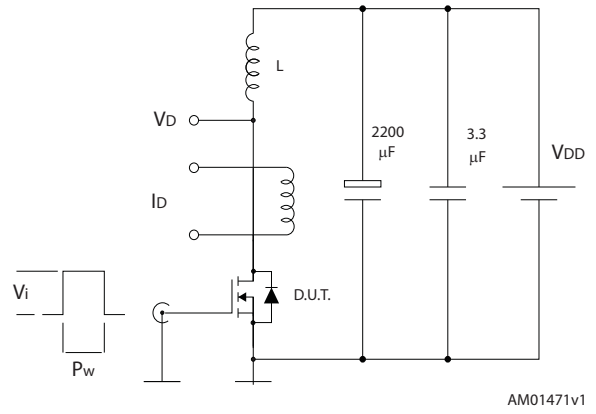


Figure 16. Unclamped inductive waveform

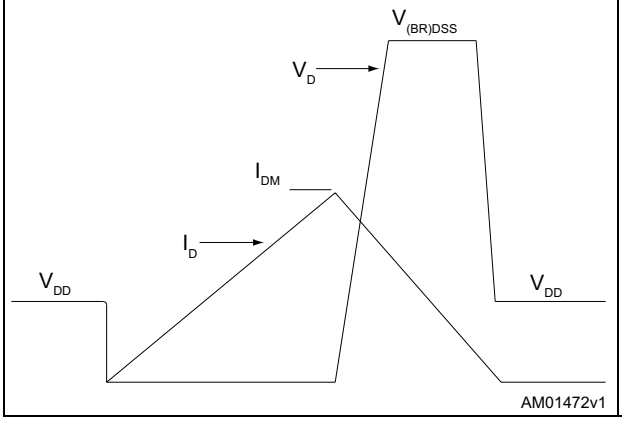
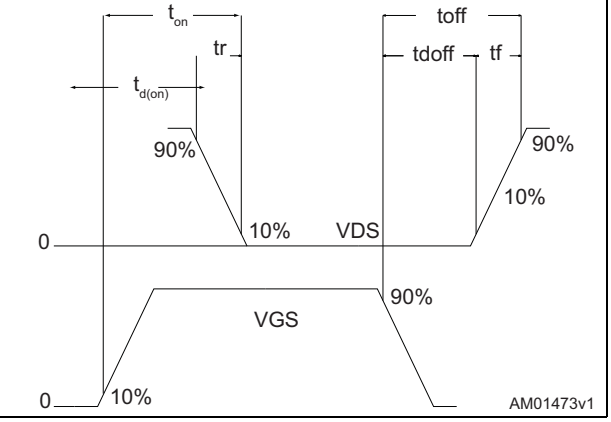


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 18. SO-8 package outline

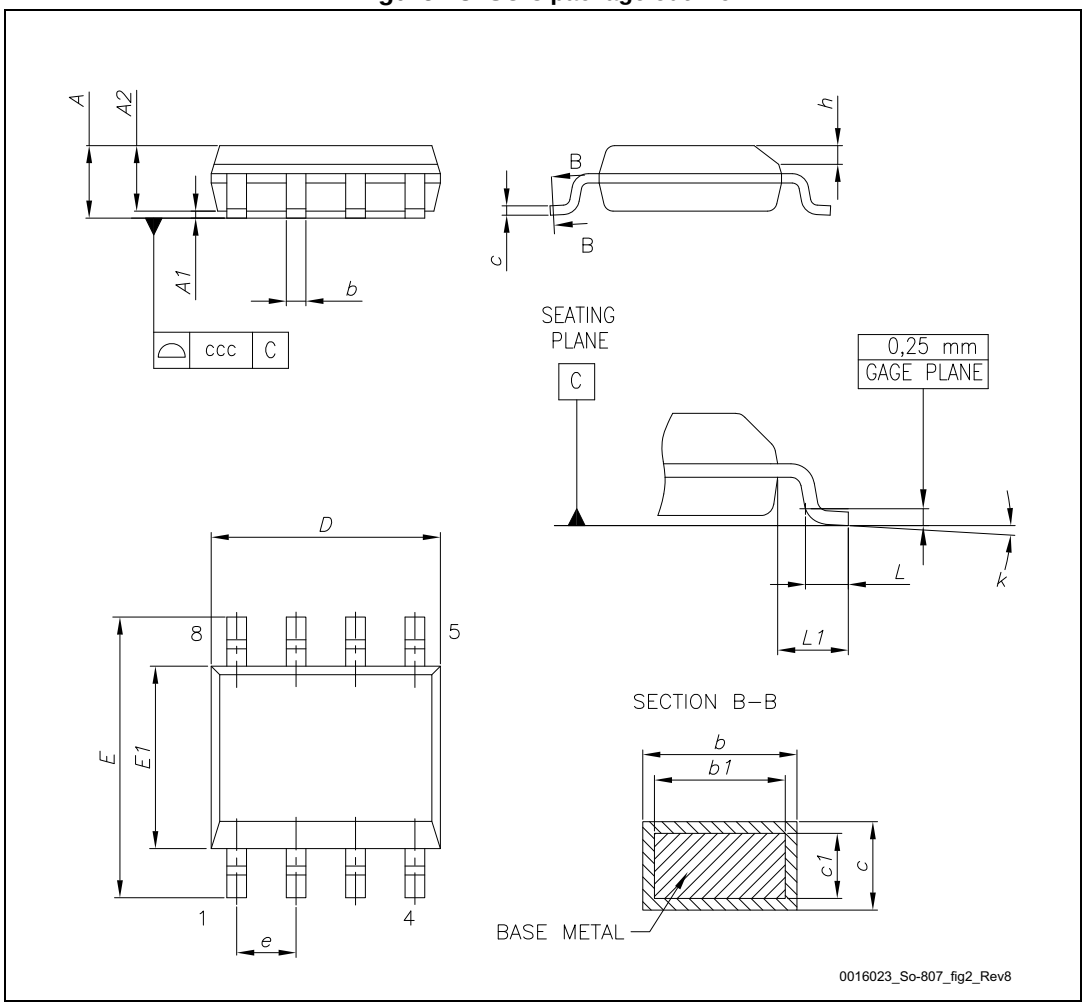
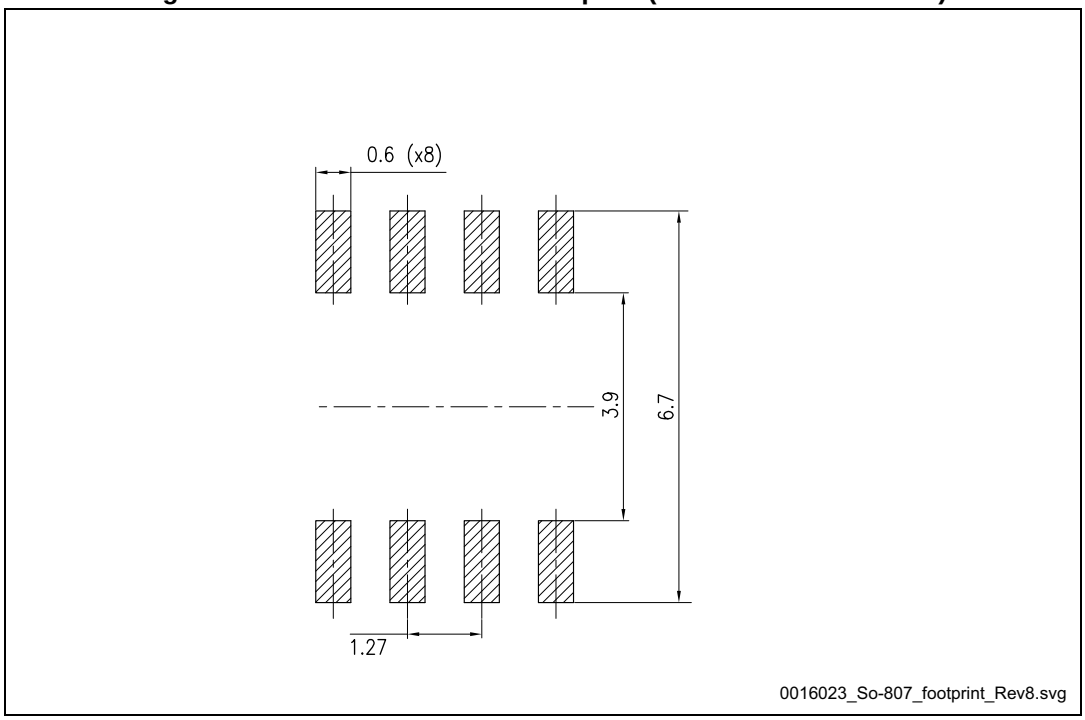


Table 8. SO-8 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
K	0°		8°
ccc			0.10

Figure 19. SO-8 recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 20. Tape and reel dimension

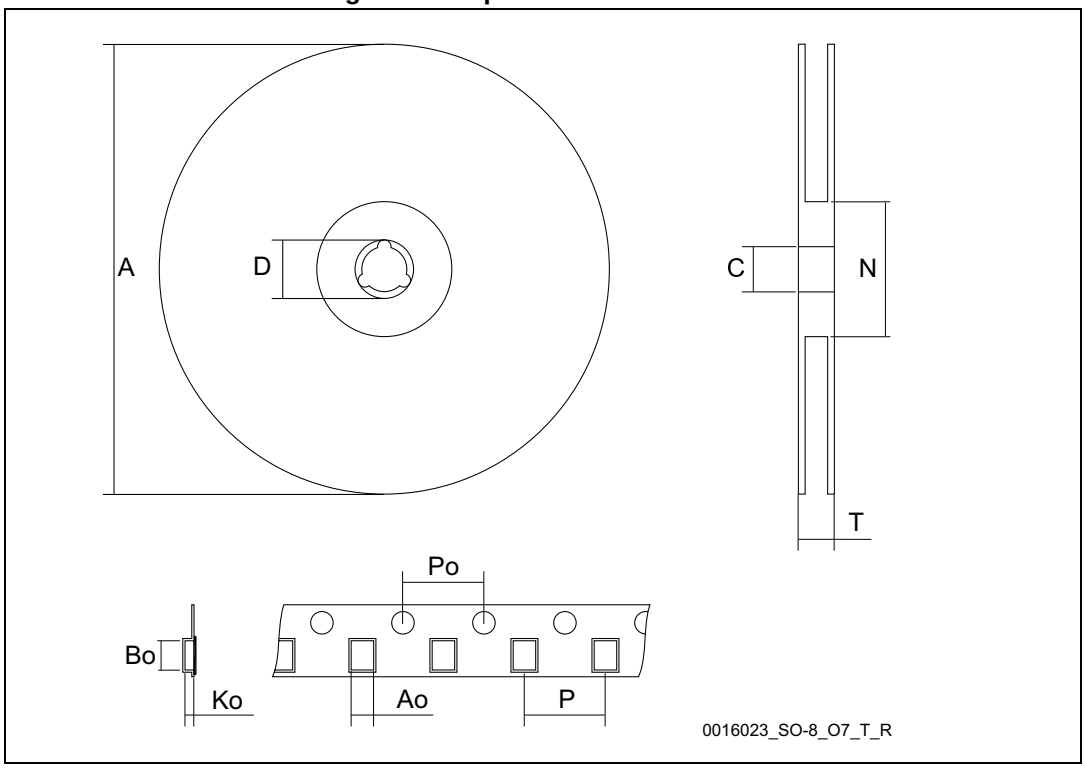


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

5 Revision history

Table 10. Revision history

Date	Revision	Changes
03-Mar-2008	1	First release
18-Mar-2010	2	*Figure 2: Safe operating area* and *Figure 3*: *Thermal impedance* have been changed.
17-Oct-2016	3	Updated title, features and description in cover page. Added AEC-Q101 qualified in the Features section. Updated *Package information* and *Packing information*. Minor text changes.

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