PD70210/PD70210A/PD70210AL

Datasheet

Front-End PD Interface Controller

March 2018

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in March 2018. The following is a summary of changes in revision 2.0 of this document.

- Document format was updated.
- Capacitor between VAUX and VPN_OUT was updated to 4.7 µF according to AN_209 Application Note. For more information, see Applications (see page 3).
- MSL3 rating was added to the storage temperature information. For more information, see Absolute Maximum Ratings (see page 12).

1.2 Revision 1.51

Revision 1.51 was published in October 2015. The following is a summary of changes in revision 1.51 of this document.

- The 80 mS delay was removed from the Vaux pin description.
- Missing UVLO_ON information was added.

1.3 Revision 1.50

Revision 1.50 was published in October 2014. In revision 1.50 of this document, flag description details were added.

1.4 Revision 1.40

Revision 1.40 was published in June 2014. In revision 1.40 of this document, WA_EN information was added.

1.5 Revision 1.38

Revision 1.38 was published in April 2014. In revision 1.38 of this document, thermal properties were added.

1.6 Revision 1.37

Revision 1.37 was published in January 2014. In revision 1.37 of this document, package information was corrected.

1.7 Revision 1.36

Revision 1.36 was published in January 2014. In revision 1.36 of this document, IC marking information was added.

1.8 Revision 1.34

Revision 1.34 was published in December 2013. The following is a summary of changes in revision 1.34 of this document.

- A new 38-pin, 5 × 7 QFN package option was added (PD70210AL).
- The package drawing was updated and an application diagram for the new package added.
- The flag table was updated.

1.9 Revision 1.2

Revision 1.2 was published in November 2013. In revision 1.2 of this document, the PD70210 application diagram was updated.

1.10 Revision 1.1

Revision 1.1 was published in October 2013. In revision 1.1 of this document, the Vaux description and cap GND symbol were fixed.

1.11 Revision 1.0

Revision 1.0 was published in June 2013. It was the first publication of this document.

2 Product Overview

The PD70210, PD70210A, and PD70210AL devices are advanced PD interface controllers (front-end IC) for powered devices in PoE applications. They support IEEE 802.3af, IEEE 802at, HDBaseT, and general 2-pair or 4-pair configurations.

The PD70210, PD70210A, and PD70210AL devices include an advanced classification block that supports 2, 3, 4, and 6 event classification. Using the SUPP_Sx pins, they also identify which of the four pairs of the cable actually receive power and generates appropriate flags. The IC features an internal bleeder for rapidly discharging the input capacitor of the DC–DC converter, so as to ensure fast re-detection and port power-up in case of sudden removal and re-insertion of the Ethernet cable into RJ-45.

2.1 Features

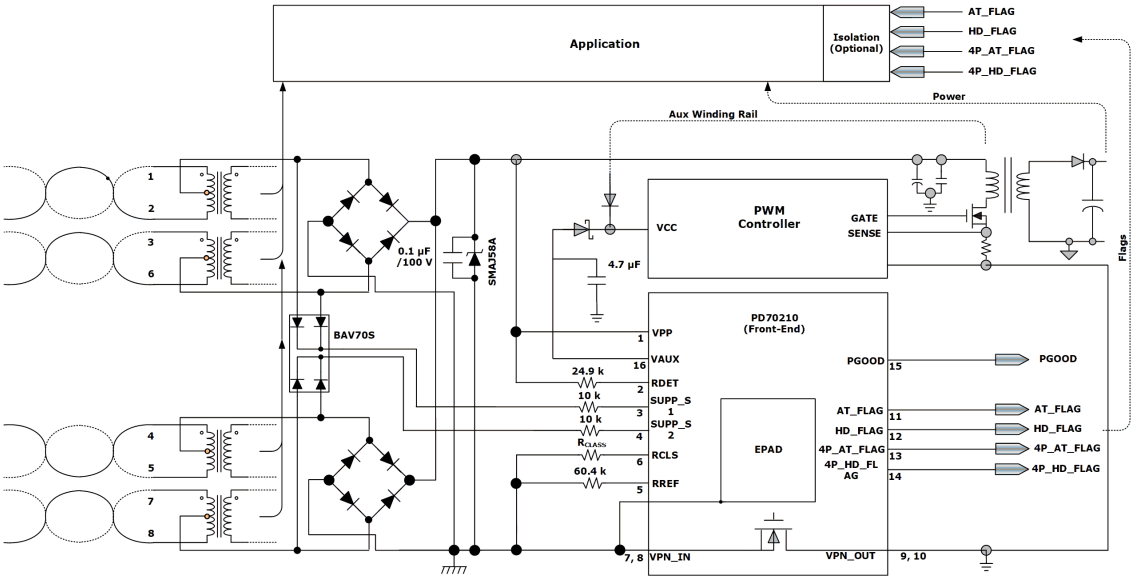
- Supports IEEE 802.3af/at, HDBaseT, and other 2-pair or 4-pair configurations.
- PD detection and programmable classification
- 2, 3, 4, and 6 event classification
- Integrated 0.3 Ω isolating (series-pass) FET
- In-rush current limiting
- Wall adapter support (PD70210A and PD70210AL only)
- Less than 5 µA offset current during detection
- Lead-free DFN-16/QFN-38 package

2.2 Applications

- Single HDBaseT or double, up to 95 W
- IEEE 802.3af and 802.3at
- Indoor and outdoor PoE

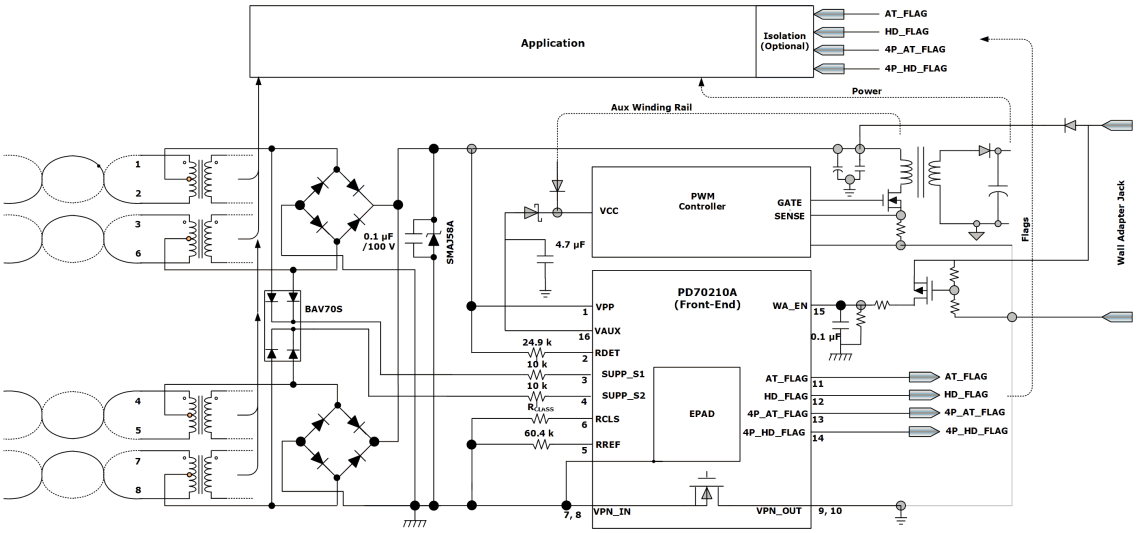
The following illustration shows a typical PD70210 application.

Figure 1 • PD70210 Typical Application



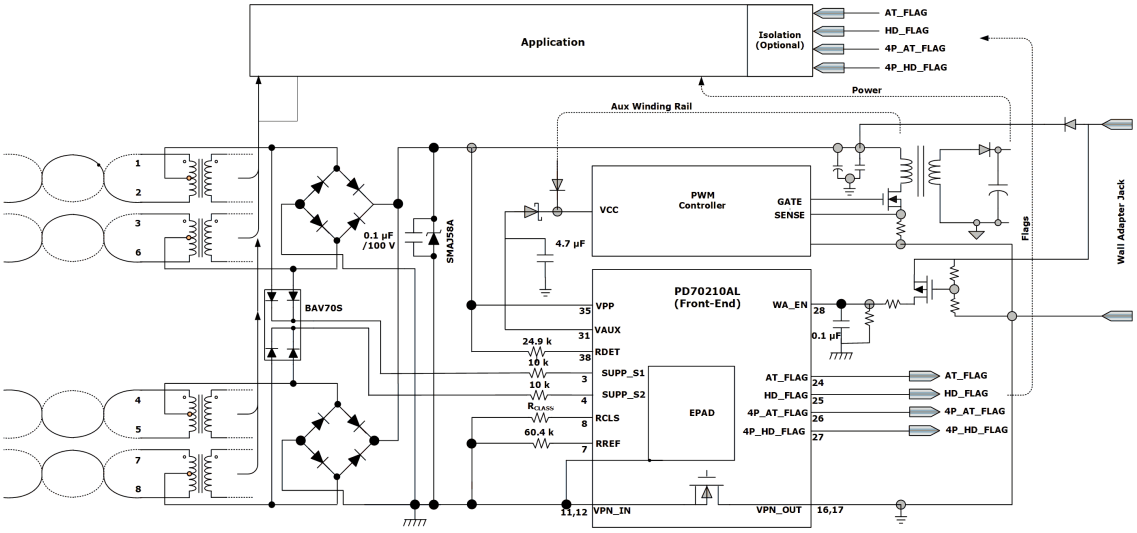
The following illustration shows a typical PD70210A application.

Figure 2 • PD70210A Typical Application



The following illustration shows a typical PD70210AL application.

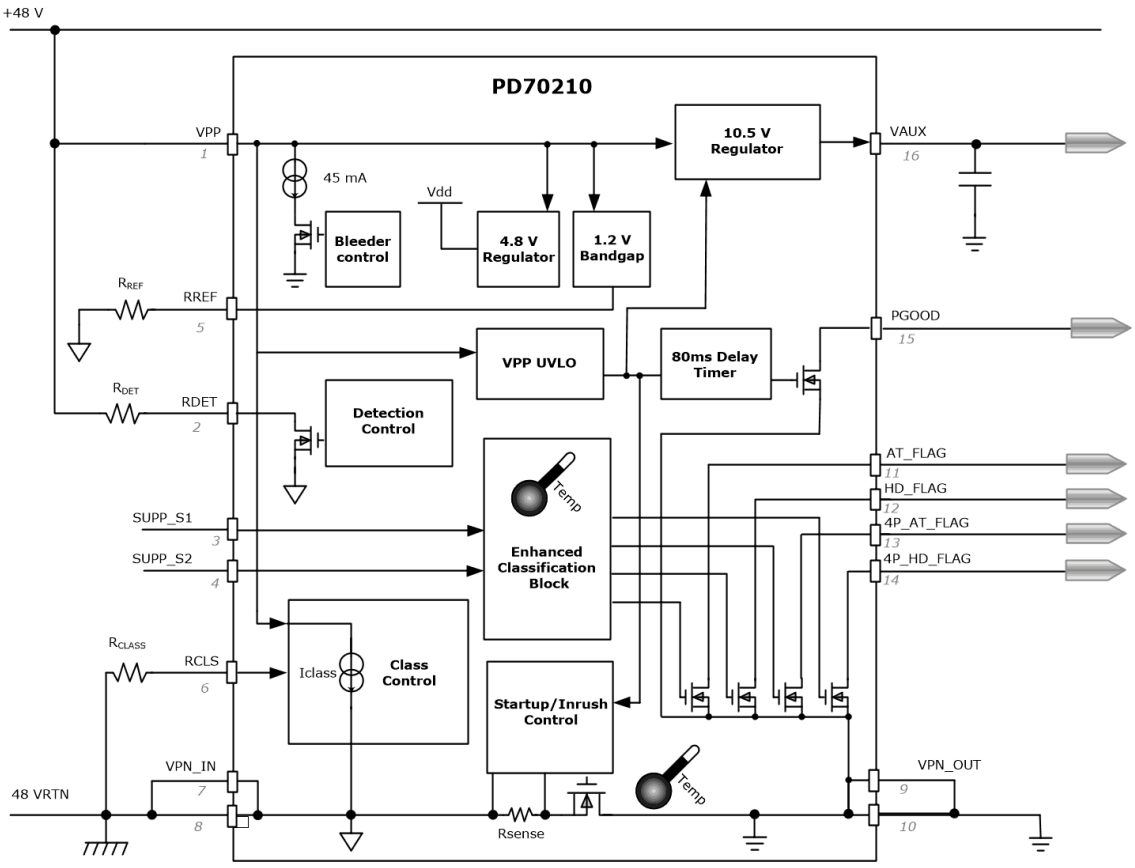
Figure 3 • PD70210AL Typical Application



3 Functional Descriptions

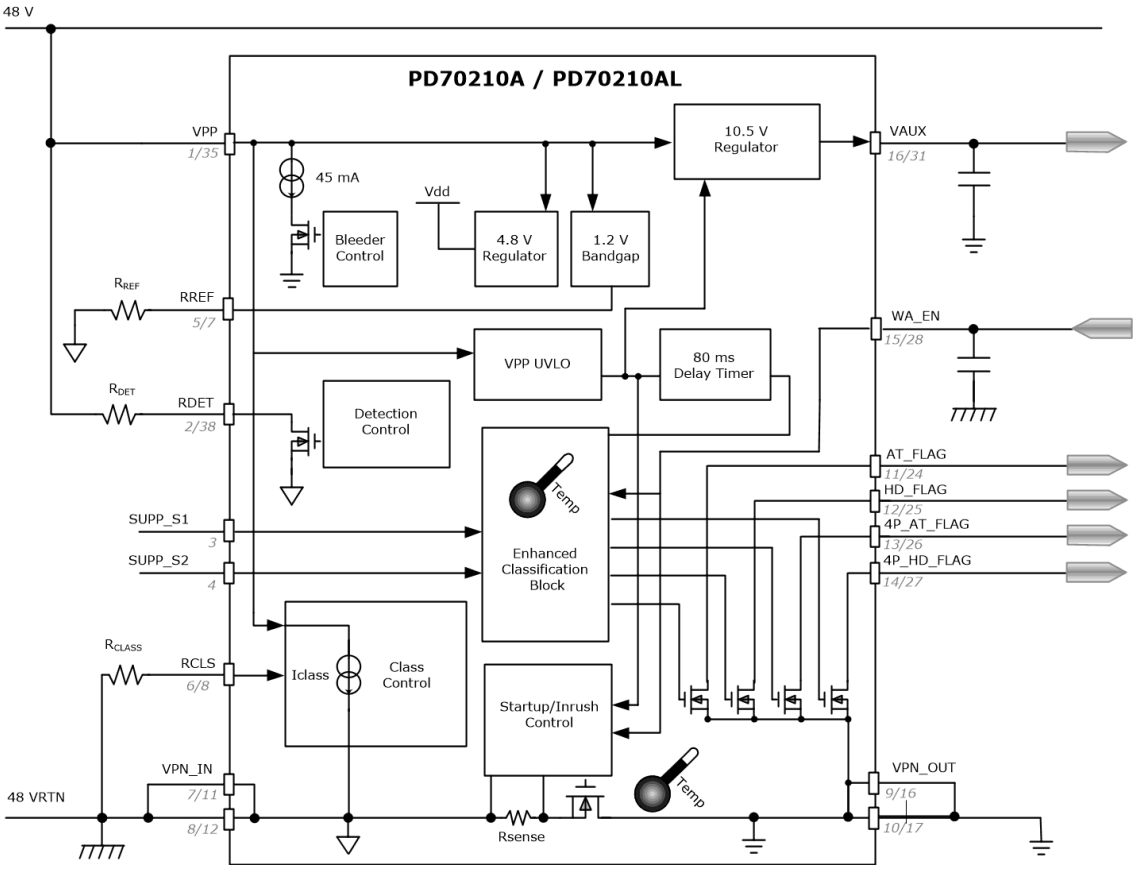
The following illustration shows the functional blocks of the PD70210 device.

Figure 4 • PD70210 Functional Block Diagram



The following illustration shows the functional blocks of the PD70210A/PD70210AL devices.

Figure 5 • PD70210A/PD70210AL Functional Block Diagram



3.1 Application Information

The following section describes the PD70210 application.

3.1.1 Peripheral Devices

- A 100 nF/100 V capacitor should be placed between the device's VPP and VPNI pins, and located as close as possible to the device.
- A 58 V TVS should be placed between the device's VPP and VPN_IN pins.
- A 10K Ω resistor should be placed on SUPP_S1 and SUPP_S2 lines between the diode bridge and PD70210/A device if 4-pair flags are going to be used.
- When WA_EN is used, an 100 nF/10 V capacitor should be placed between WA_EN and the VPN_IN pin, close to the PD70210/A device.
- When not used, WA_EN should be connected to the VPN_IN pin.
- A 4.7 µF/25 V capacitor should be placed between Vaux pin and VPN_OUT.

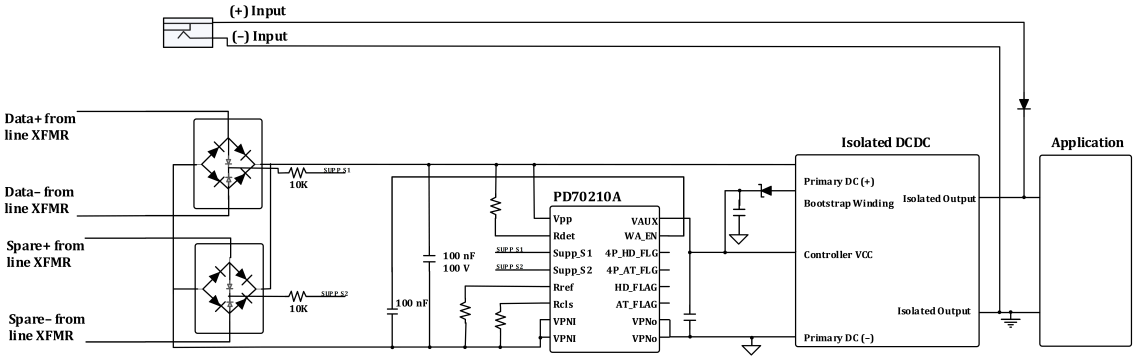
3.1.2 Operation with an External DC Source

PD applications utilizing the PD70210A IC may be operated with an external power source (DC wall adapter). There are two cases of providing power with an external source, presented in the following sections.

3.1.2.1 External Power Input Connected to Application Supply Rails

In this application, the external source is connected to the application's low-voltage supply rails. The external source voltage level is dependent on DC–DC output characteristics.

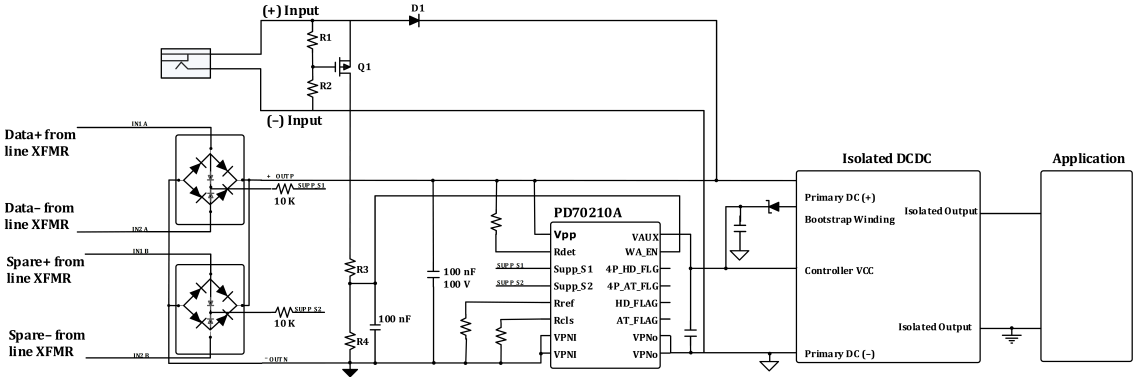
Figure 6 • External Power Input to Supply Rails



3.1.2.2 External Power Input Connected to PD70210A Output

In this application, the external source is connected to the PD device's output connection toward the application (VPP to VPN_{OUT}). The external source voltage level is dependent on DC–DC input requirements.

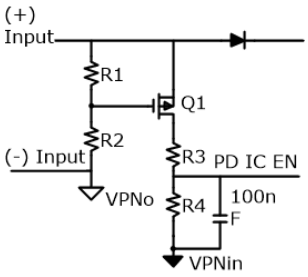
Figure 7 • External Power Input to PD70210A Output



When an external adapter is connected, the PD70210A WA_EN pin is used for disabling the isolation switch and PSE input power. The WA_EN resistors divider depends on the WA_EN threshold of the PD70210A.

The following illustration shows a detailed view of the resistors to be selected in an external adapter connection.

Figure 8 • External Power Input Resistors Dividers



R1 and R2 sets a rough threshold for Pfet Q1 enable to detect whether an external adapter exists or not. It should be set to be a lower threshold than PD70210A disable levels. R3 and R4 set the PD70210A disable threshold. So, in the case of a 36 V–57 V external adapter, the disable setting can be selected as follows:

Pfet enable threshold = 30 V.

R1 and R2 setting should be so that the value of Q1 VGS < 20 V at the maximum voltage condition of the external adapter.

When the external adapter voltage is above 30 V, Q1 will be above its VGS_{TH} value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

R1 is selected as 2K Ω.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

Using R1 = 2K Ω, Vext_adapter = 30 V, and VGS = maximum VGS_{TH} = 3.5 V, we get the R2 value.

R2 = 15K Ω

R3 and R4 are set to the range of few KΩ – 10s of KΩ using the following equation:

$$PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4}{(R3+R4)}$$

Using R3 = 15K Ω, Vext_adapter = 33.7 V, and PD70210A_WA_EN = 2.4 V as turn-off minimum threshold from the datasheet, solving the equation gives the valid resistor values for an adapter of 36 V and above.

R3 = 15K Ω

R4 = 1.15K Ω

3.2 Wall Adapter Mode (PD70210A/L)

PD70210A and PD70210AL support wall adapter functionality. That is, by setting the WA_EN pin high, it will give priority to the wall adapter jack to supply the load.

The WA_EN pin is used while connecting a wall-adapter voltage between VPP and VPN_OUT by means of an OR-ing diode. When WA_EN (the wall-adapter enable pin) is held low (referenced to VPN_IN), the front-end works as a normal PD. When WA_EN is raised high (referenced to VPN_IN), three internal operations are forced:

- The isolation FET is turned OFF.
- All output flags (AT_FLAG, HD_FLAG, 4P_AT_FLAG, and 4P_HD_FLAG) are activated (low state).
- Vaux output voltage is turned ON.

While activating the WA_EN pin, the wall-adapter will supply input voltage for the DC–DC converter. Having WA_EN at a high state disables detection and classification modes.

3.3 Flags

The following is the truth table for flags status.

Table 1 • Truth Table for Status of Flags

Number of Fingers "N" (N-Event Classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0 V	Hi Z	Hi Z	Hi Z
2	L	H	0 V	Hi Z	Hi Z	Hi Z
2	H	H	0 V	Hi Z	0 V	Hi Z
3	L	H	0 V	0 V	Hi Z	Hi Z
3	H	L	0 V	0 V	Hi Z	Hi Z
3	H	H	0 V	0 V	0 V	Hi Z
4	X	X	0 V	0 V	0 V	Hi Z
5	RESERVED FOR FUTURE					
6	X	X	0 V	0 V	0 V	0 V

Note: A flag's state is set only once at port turn on, while VPP-VPNin voltage crosses $UVLO_{ON}$. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly.

4 Electrical Specifications

Unless otherwise specified under conditions, the minimum and maximum ratings stated apply over the entire specified operating rating of the device. Typical values are either by design or by production testing at 25 °C ambient. Voltages are with respect to IC ground (VPN_IN).

Table 2 • Input Voltage

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{IN}	IC input current with I_{CLASS} off	VPP = 55 V	1	3	mA

Table 3 • Detection Phase

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DET}	Detection range		1.1		10.1	V
R_{DET_TH}	R_{DET} disconnect threshold		10.1		12.8	V
$R_{DS\_DET\_ON}$	On-resistance of internal FET during detection				50	Ω
$R_{DS\_DET\_OFF}$	Off-resistance of internal FET after detection		2			MΩ
I_{OFFSET_DET}	Input offset current	1.1 V ≤ VPP ≤ 10.1 V T_J ≤ 85 °C			5	µA
$V_{R\_DET\_ON}$	R_{DET} reconnection threshold when VPP goes low		2.8	3.0	4.85	V

Table 4 • Classification Phase

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CLS_ON}	Classification sink turn-on threshold		11.4		13.7	V
V_{CLS_OFF}	Classification sink turn-off threshold		20.9		23.9	V
$V_{HYS\_CLS\_ON}$	Hysteresis of V_{CLS_ON} threshold			1		V
V_{MARK_TH}	Mark detection threshold (VPP falling)		10.1		11.4	V
I_{MARK}	Current sink in mark event region		0.25		4	mA
I_{CLASS_CLIM}	Current limit of class current		50	68	80	mA
I_{CLASS}	Classification current sink	R_{CLASS} = not present (Class 0)			3	mA
		R_{CLASS} = 133 Ω (Class 1)	9.5	10.5	11.5	
		R_{CLASS} = 69.8 Ω (Class 2)	17.5	18.5	19.5	
		R_{CLASS} = 45.3 Ω (Class 3)	26.5	28.0	29.5	
		R_{CLASS} = 30.9 Ω (Class 4)	38.0	40.0	42.0	

Table 5 • Isolation FET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DSON}	On resistance	Total resistance between VPN_IN to VPN_OUT; I_{LOAD} < 600 mA, –40 °C < T_A < 85 °C		0.22	0.3	Ω
I_{CLIM_INRUSH}	Inrush current limit		105	240	325	mA
OCP	Overcurrent protection		2.2			A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LOAD}	Continuous operation load[1]				2	A

Note:

1. Actual maximum load is subject to the application environment conditions, such as ambient temperatures, air flow, mutual heating by other components, and so on.

Table 6 • Undervoltage Lockout

Symbol	Parameter	Min	Max	Unit
$UVLO_{ON}$	Threshold that marks start of inrush phase	36	42	V
$UVLO_{OFF}$	Threshold where pass-FET turns off as VPP collapses	30.5	34.5	V

Table 7 • DC–DC Input Cap Discharger

Symbol	Parameter	Conditions	Min	Max	Unit
I_{CAP_DIS}	Discharge current (PD70210)	12 V ≤ VPP ≤ 30 V	22.8	60	mA
		7 V ≤ VPP ≤ 12 V	10		mA
I_{CAP_DIS}	Discharge current (PD70210A)	7 V ≤ VPP ≤ 30 V	22.8	60	mA
$timer_{dis}$	Discharge timer	Time for which discharge circuit is activated	430		ms

Table 8 • References, Rails, and Logic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AUX}	Auxiliary voltage	0 mA < I_{AUX} < 4 mA	9.8	10.5	12.0	V
I_{AUX_CLIM}	Auxiliary current limit		10		32	mA
V_{REF}	Bias current reference voltage		1.17	1.2	1.23	V
V_{FLAG_LO}	Low-level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I_{FLAG} = 3 mA			0.4	V
V_{PGOOD_LO}	Power good, active low voltage	I_{PGOOD} = 3mA PD70210 only			0.4	V
t_{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80			ms
t_{PGOOD}	Delay timer between start of inrush and power good declared	PD70210 only	80			ms
I_{FLAG_max}	Flag current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5			mA
I_{PGOOD_max}	Power good current capability	PD70210 only	5			mA
V_{SUPP_HI}	SUPP_Sx high-voltage threshold	For SUPP_S1 and SUPP_S2	25		35	V

Table 9 • Wall Adapter Enable Pin

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input high logic	PD70210A, PD70210AL only	2.4		V
V_{IL}	Input low logic	PD70210A, PD70210AL only		0.8	V

4.1 Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN) unless otherwise specified.

Table 10 • Absolute Maximum Ratings

Parameter		Min	Max	Units
VPP, RDET		–0.3	74	V
PGOOD, AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG referenced to VPN_OUT		–0.3	20	V
SUPP_S1, SUPP_S2		0	V_{VPP} + 1.5	V
RREF, RCLS, WA_EN		–0.3	5	V
Junction temperature		–40	150	°C
Lead soldering temperature (40 s, reflow)			260	°C
Storage temperature, MSL3		–65	150	°C
ESD rating	HBM (PD70210)		±1.5	kV
	HBM (PD70210A/PD70210AL)		±1.25	kV
	MM		±100	V
	CDM		±500	V

4.2 Operating Conditions

Performance is generally guaranteed over this range as described in other electrical characteristics tables. Voltages are with respect to IC ground (VPN_IN).

Table 11 • Operating Conditions

	Min	Max	Units
VPP	0	57	V
Ambient temperature[1]	–40	85	°C
Detection range	1.1	10.1	V
Mark event range	4.9	10.1	V
Class event range	13.7	20.9	V

Note:

1. Corresponding maximum operating junction temperature is 125 °C.

4.3 Thermal Properties

The following table shows the thermal properties of the device.

Table 12 • Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	31	°C/W
θ_{JP}	3	°C/W
θ_{JC}	4	°C/W

Note: θ_{JX} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} is a function of the PCB construction. The stated number is for a four-layer board in accordance with JESD-51 (JEDEC).

5 Pin Descriptions

This section provides the pin information for the PD70210/PD70210A/PD7021AL devices.

The following illustrations show the device pin diagrams (top and bottom views).

Figure 9 • PD70210 Pinout

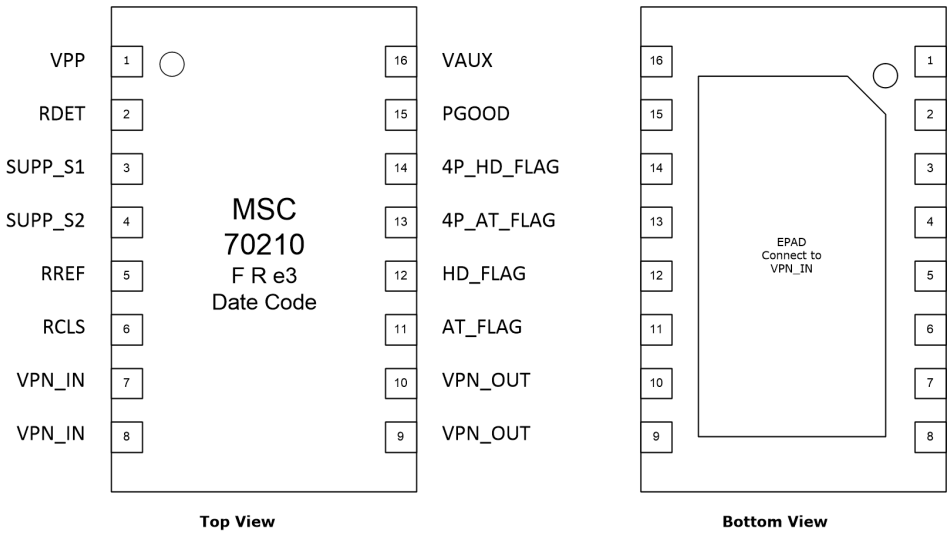


Figure 10 • PD70210A Pinout

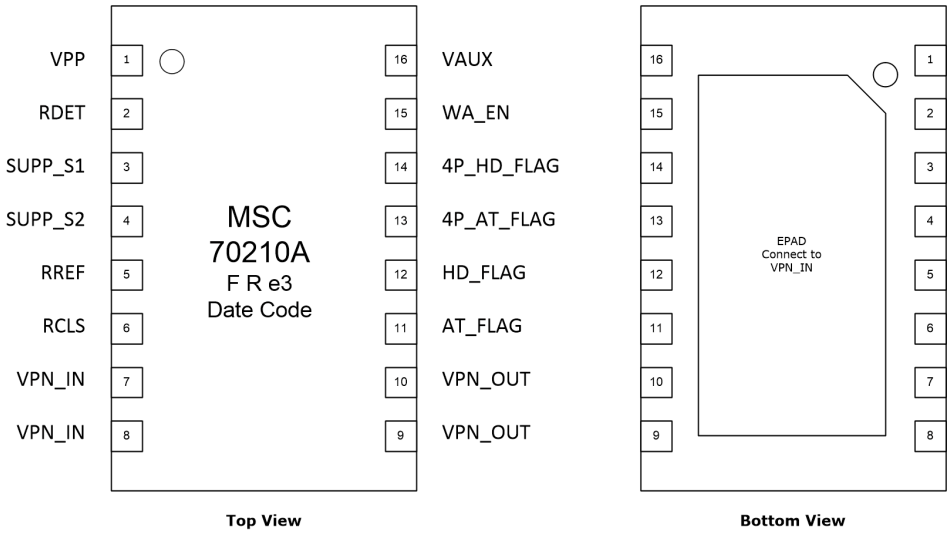
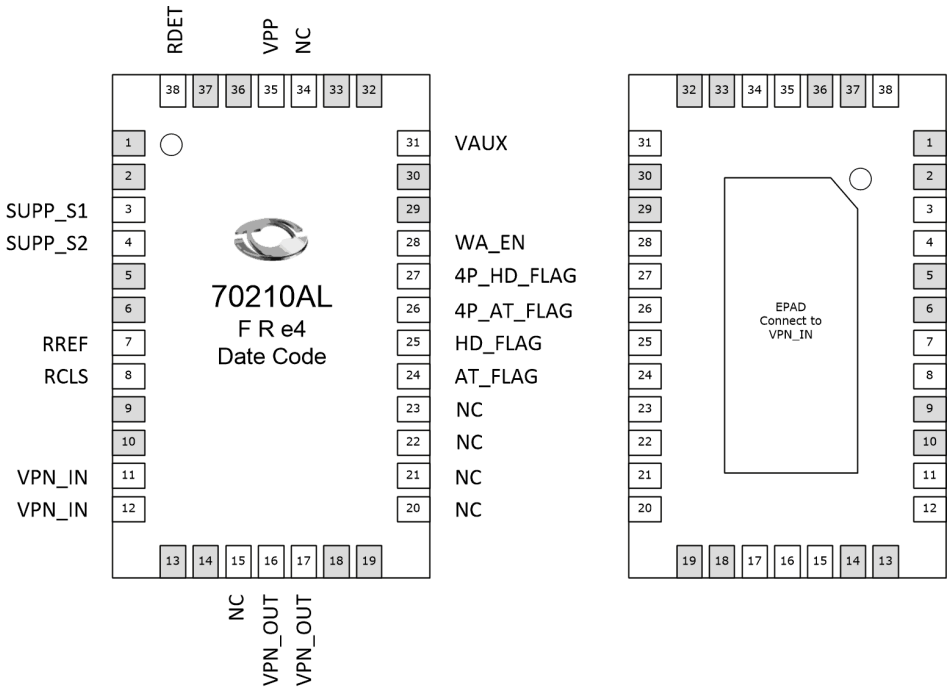


Figure 11 • PD70210AL Pinout



Note: Shaded pins do not exist.

The following table lists the pin descriptions for the PD70210/PD70210A devices.

Table 13 • PD70210/PD70210A Pin Descriptions

Pin Number	Pin Name (PD70210A)	Pin Name (PD70210)	Description
1	VPP	VPP	Upper rail of the incoming PSE voltage rail, from the positive terminal of the two OR-ed bridge rectifiers. The corresponding lower PoE rail is VPN_IN.
2	RDET	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25K Ω (or 24.9K) 1% resistor is connected between this pin and VPP.
3	SUPP_S1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S2 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4 pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
4	SUPP_S2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S1 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4 pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
5	RREF	RREF	Bias current resistor. A 60.4K 1% resistor is connected between RREF and IC ground (VPN_IN).

Pin Number	Pin Name (PD70210A)	Pin Name (PD70210)	Description
6	RCLS	RCLS	Sets the class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4, respectively. If R_{CLASS} is not present, the PD will draw up to 3 mA during classification, indicating Class 0 (default type 1) to the PSE. Signal is referenced to VPN_IN.
7, 8	VPN_IN	VPN_IN	Lower rail of the incoming PSE voltage rail, from the negative terminal of the two OR-ed bridge rectifiers. The corresponding upper PoE rail is VPP.
9, 10	VPN_OUT	VPN_OUT	In effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and power-up. It is connected to the power ground and PWM controller IC's ground plane of the DC–DC converter section.
11	AT_FLAG	AT_FLAG	Open drain output. This pin gets actively pulled low when a type 2 PD-PSE mutually identifies each other through classification. In PD70210A/L, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
12	HD_FLAG	HD_FLAG	Open drain output. This pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identifies each other through classification. In PD70210A/L, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
13	4P_AT_FLAG	4P_AT_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair version of a (non-standard) type 2 PD-PSE mutually identifies each other through classification. In PD70210A/L, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
14	4P_HD_FLAG	4P_HD_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identifies each other through classification. In PD70210A/L, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
15	WA_EN		While this input is low (referenced to VPN_IN), the chip works according to internal flow diagram. When this input is high, it enables the wall adapter feature. Place from 100 nF/10 V to 1 µF/10 V capacitor from WA_EN to VPN_IN pins, close to the device. When WA_EN is not used, connect it to VPN_IN. For more information, see External Power Input to Supply Rails (see page 7).
		PGOOD	Open drain output. Power good output signal from the front-end stage. This pin gets actively pulled low when power-on occurs. There is a minimum 80 ms delay from the moment VPort exceeds UVLO (~36 V) to this PGOOD signal being driven low as per the IEEE standard, to allow the PSE to increase its current limit after power-up is completed. Signal is referenced to VPN_OUT.
16	VAUX	VAUX	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (typically, 10.5 V). Signal is referenced to VPN_OUT and is activated once the front-end power-up sequence ends. DC–DC should not start up until Vaux is active.
	EPAD	EPAD	Connected on PCB plane to VPN_IN.

The following table lists the pin descriptions for the PD70210AL device.

Table 14 • PD70210AL Pin Descriptions

Pin Number	Pin Name	Description
1, 2	NA	
3	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S2 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4 pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
4	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S1 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4 pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10K resistor in the input of this pin.
5, 6	NA	
7	RREF	Bias current resistor. A 60.4K 1% resistor is connected between RREF and IC ground (VPN_IN).
8	RCLS	Sets the class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4, respectively. If R_{CLASS} is not present, the PD will draw up to 3 mA during classification, indicating Class 0 (default type 1) to the PSE. Signal is referenced to VPN_IN.
9, 10	NA	
11, 12	VPN_IN	Lower rail of the incoming PSE voltage rail, from the negative terminal of the two OR-ed bridge rectifiers. The corresponding upper PoE rail is VPP.
13, 14	NA	
15	NC	No connect.
16, 17	VPN_OUT	In effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and power-up. It is connected to the power ground and PWM controller IC's ground plane of the DC–DC converter section.
18, 19	NA	
20, 21, 22, 23	NC	No connect.
24	AT_FLAG	Open drain output. This pin gets actively pulled low when a type 2 PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
25	HD_FLAG	Open drain output. This pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
26	4P_AT_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair version of a (non-standard) type 2 PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
27	4P_HD_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
28	WA_EN	While this input is low (referenced to VPN_IN), the chip works according to internal flow diagram. When this input is high, it enables the wall adapter feature. Place from 100 nF/10 V to 1 µF/10 V capacitor from WA_EN to VPN_IN pins, close to the device. When WA_EN is not used, connect it to VPN_IN. For more information, see External Power Input to Supply Rails (see page 7).
29, 30	NA	

Pin Number	Pin Name	Description
31	VAUX	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (typically, 10.5 V). Signal is referenced to VPN_OUT and is activated once the front-end power-up sequence ends. DC–DC should not start up until Vaux is active.
32, 33	NA	
34	NC	No connect.
35	VPP	Upper rail of the incoming PSE voltage rail, from the positive terminal of the two OR-ed bridge rectifiers. The corresponding lower PoE rail is VPN_IN.
36, 37	NA	
38	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25K Ω (or 24.9K) 1% resistor is connected between this pin and VPP.
	EPAD	Connected on PCB plane to VPN_IN.

6 Package Information

This section provides information about the two available packages.

Note: Dimensions do not include protrusions; these shall not exceed 0.155 mm (0.006 in.) on any side. Lead dimension shall not include solder coverage. Dimensions are in millimeters, inches for reference only.

6.1 16-Pin Plastic DFN, 5 mm × 4 mm

This section shows the 16-pin plastic DFN, 5 mm × 4 mm package and package dimensions.

Figure 12 • DFN Package

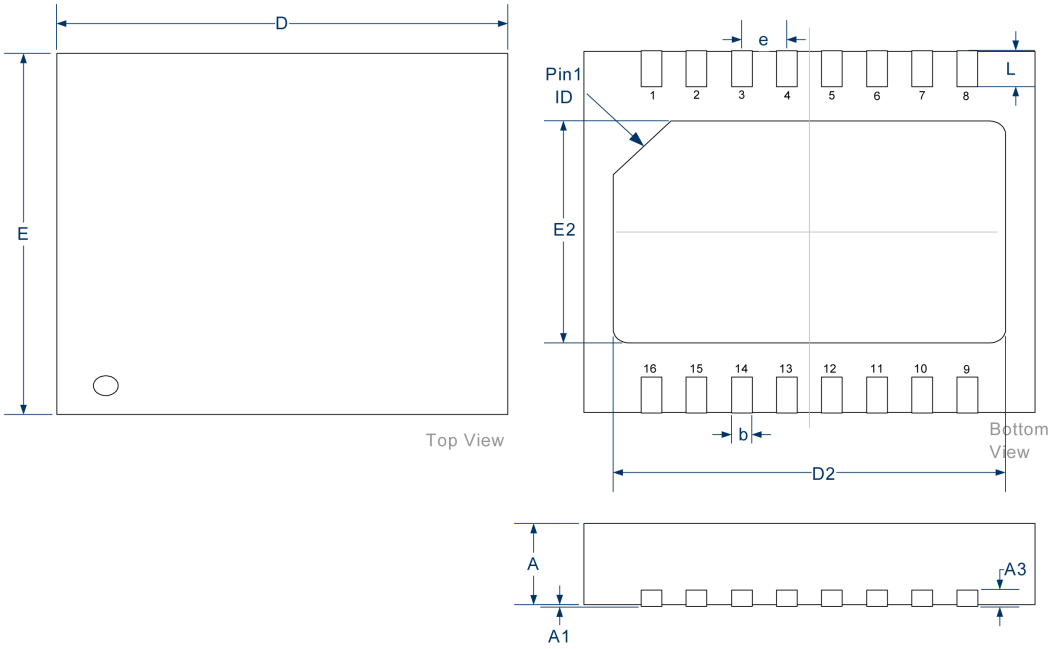


Table 15 • Package Dimensions: DFN

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
D	5.00 BSC		0.197 BSC	
E	4.00 BSC		0.157 BSC	
D2	4.20	4.45	0.165	0.175
E2	2.30	2.55	0.091	0.100
e	0.50 BSC		0.0197 BSC	
K	0.20 MIN		0.008 MIN	
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012

6.2 38-Pin Plastic QFN, 5 mm × 7 mm

This section shows the 38-pin plastic DFN, 5 mm × 7 mm package and package dimensions.

Figure 13 • QFN Package

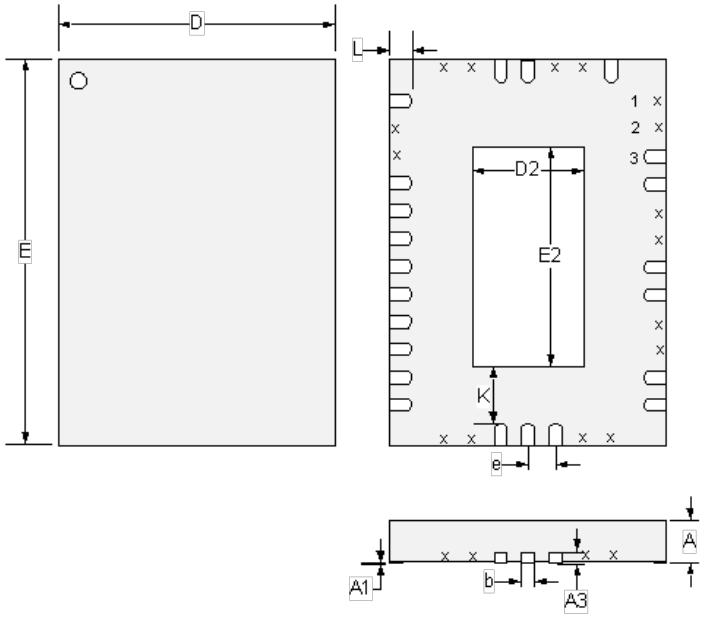


Table 16 • Package Dimensions: QFN

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.196 BSC	
E	7.00 BSC		0.275 BSC	
D2	1.85	2.10	0.073	0.083
E2	3.85	4.10	0.152	0.161
e	0.50 BSC		0.020 BSC	
K	1.016		0.040	
L	0.30	0.50	0.012	0.020

6.3 Thermal Protection

PD70210, PD70210A, and PD70210AL are protected from excessive internal temperatures that may occur during various operating procedures. Two temperature sensors are located on the chip, monitoring the temperatures of the isolating switch (pass-FET) and classification current sink.

Each of the over-temperature sensors activates a protection mechanism that will disconnect the isolation (pass) FET or the classification circuit. This protects the device from being permanently damaged and from long-term degradation.

7 Ordering Information

The following table lists the detailed part ordering information for the PD70210 device. All part numbers are RoHS-compliant, Pb-free, and have an ambient temperature range of –40 °C to 85 °C. All parts also have 2-pair/4-pair HDBaseT support.

Table 17 • Ordering Information

Part Number	Packaging Type	Package	Part Marking	Wall Adapter Support	Clearance Between HV Pins
PD70210ILD	Bulk	DFN 5 mm × 4 mm, 0.5 mm pitch 16 pins	MSC 70210 FR e3[1] YYWWAZZ[2]		0.2 mm
PD70210ILD-TR	Tape and reel				
PD70210AILD	Bulk	DFN 5 mm × 4 mm, 0.5 mm pitch 16 pins	MSC 70210A FR e3[1] YYWWAZZ[2]	Available	0.2 mm
PD70210AILD-TR	Tape and reel				
PD70210ALILQ	Bulk	QFN 5 mm × 7 mm, 0.5 mm pitch 38 pins	Microsemi Logo 70210AL FR e4[1] YYWWAZZ[2]	Available	1 mm
PD70210ALILQ-TR	Tape and reel				

Notes:

1. FR e3: F = FAB Code; R = Product Revision Code; and e3,e4 = 2nd Level Interconnect.
2. YY = Year; WW = Week; A = Assembly Location; ZZ = Assembly Lot Sequence Code.

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