Dual Bidirectional I²C-bus and SMBus Voltage-Level Translator

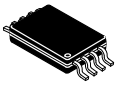
PCA9306

The PCA9306 is a dual bidirectional I²C–bus and SMBus voltage–level translator with an enable (EN) input.

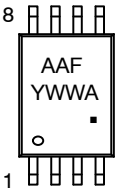
Features

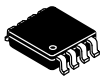
- 2–bit Bidirectional Translator for SDA and SCL Lines in Mixed–Mode I²C–Bus Applications
- Standard–Mode, Fast–Mode, and Fast–Mode Plus I²C–Bus and SMBus Compatible
- Less Than 1.5 ns Maximum Propagation Delay to Accommodate Standard–Mode and Fast–Mode I²C–Bus Devices and Multiple Masters
- Allows Voltage Level Translation Between:
  - 1.0 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.2 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.8 V $V_{ref(1)}$ and 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 2.5 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
  - 3.3 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
- Provides Bidirectional Voltage Translation With No Direction Pin
- Low 3.5 Ω ON–State Connection Between Input and Output Ports Provides Less Signal Distortion
- Open–Drain I²C–Bus I/O Ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V Tolerant I²C–Bus I/O Ports to Support Mixed–Mode Signal Operation
- High–Impedance SCL1, SDA1, SCL2 and SDA2 Pins for EN = LOW
- Lock–Up Free Operation
- Flow Through Pinout for Ease of Printed–Circuit Board Trace Routing
- Packages Offered:
  - TSSOP–8, US8, UQFN8, UDFN8
- ESD Performance: 4000 V Human Body Model, 400 V Machine Model
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These are Pb–Free Devices

MARKING DIAGRAMS



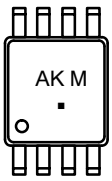
TSSOP–8
DT SUFFIX
CASE 948AL





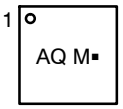
US8
US SUFFIX
CASE 493

Commercial

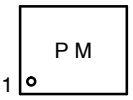


NLV Prefix

UQFN8
MU SUFFIX
CASE 523AN



UDFN8
1.45 x 1.0
CASE 517BZ



AAF, AK, AQ, P	= Specific Device Code
A	= Assembly Location
L	= Lot Code
Y	= Year Code
W, WW	= Week Code
M	= Date Code
▪	= Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Function Description

The PCA9306 is a dual bidirectional I^2C−bus and SMBus voltage−level translator with an enable (EN) input, and is operational from 1.0 V to 3.6 V ($V_{ref(1)}$) and 1.8 V to 5.5 V ($V_{bias(ref)(2)}$).

The PCA9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON−state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high−impedance state exists between ports.

The PCA9306 is not a bus buffer that provides both level translation and physical capacitance isolation to either side of the bus when both sides are connected. The PCA9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PCA9306 can be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C−bus system, pull−up resistors are required to provide the logic HIGH levels on the translator's bus. The PCA9306 has a standard open−collector configuration of the I^2C−bus. The size of these pull−up resistors depends on the system, but each side of the translator must have a pull−up resistor. The device is designed to work with Standard−mode, Fast−mode and Fast mode Plus I^2C−bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2 MHz.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON−state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port, when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull−up supply voltage ($V_{pu(D)}$) by the pull−up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD−resistant devices.

FUNCTIONAL DIAGRAM

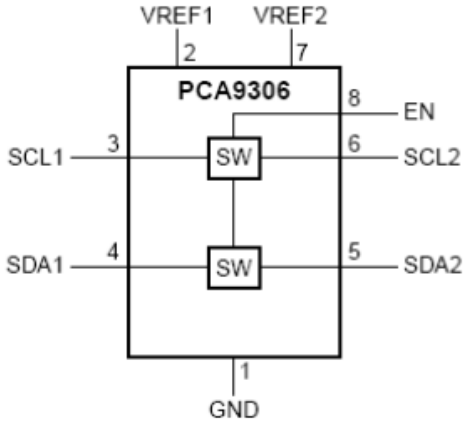


Figure 1. Logic Diagram

PIN ASSIGNMENTS

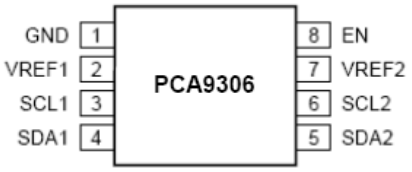


Figure 2. TSSOP−8 / US8 Pinouts

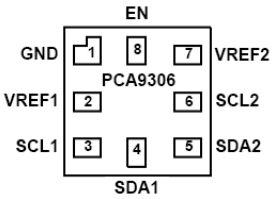


Figure 3. UQFN8 Pinout (Top Thru View)

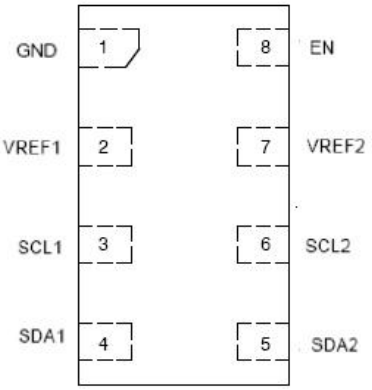


Figure 4. UDFN8 Pinout (Top Thru View)

Table 1. PIN DESCRIPTION

Pin	Description
GND	Ground
VREF1	Low−voltage side reference supply voltage for SCL1 and SDA1
SCL1	Serial clock, low−voltage side; connect to VREF1 through a pull−up resistor
SDA1	Serial data, low−voltage side; connect to VREF1 through a pull−up resistor
SDA2	Serial data, high−voltage side; connect to VREF2 through a pull−up resistor
SCL2	Serial clock, high−voltage side; connect to VREF2 through a pull−up resistor
VREF2	High−voltage side reference supply voltage for SCL2 and SDA2
EN	Switch enable input; connect to VREF2 and pull−up through a high resistor

Table 2. FUNCTION TABLE

Input EN (Note 1)	**Function**
Low	Disconnect
High	SCL1 = SCL2; SDA1 = SDA2

1. EN is controlled by the $V_{bias(ref)(2)}$ logic levels and should be at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{ref(1)}$	Reference Voltage (Note 2)	−0.5 to +7.0	V
$V_{bias(ref)(2)}$	Reference Bias Voltage (Note 3)	−0.5 to +7.0	V
V_{IN}	Input Voltage	−0.5 to +7.0	V
$V_{I/O}$	Input / Output Pin Voltage	−0.5 to +7.0	V
I_{CH}	DC Channel Current	128	mA
I_{IK}	DC Input Diode Current V_{IN} < GND	−50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	T_L = 260	°C
T_J	Junction Temperature Under Bias	T_J = 150	°C
θ_{JA}	Thermal Resistance (Note 2)	θ_{JA} = 150	°C/W
P_D	Power Dissipation in Still Air at 85°C	P_D = 833	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Mode (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 4000 > 400 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125 °C (Note 6)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
3. Tested to EIA / JESD22−A114−A.
4. Tested to EIA / JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA / JESD78.

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
$V_{ref(1)}$	Reference Voltage (1) (Note 7)	VREF1	0	5.5	V
$V_{bias(ref)(2)}$	Reference Bias Voltage (2) (Note 7)	VREF2	0	5.5	V
$V_{I/O}$	Input / Output Pin Voltage SCL1, SDA1, SCL2, SDA2		0	5.5	V
$V_{I(EN)}$	Control Pin Input Voltage EN		0	5.5	V
$I_{sw(pass)}$	Pass Switch Current		0	64	mA
T_A	Operating Free−Air Temperature		−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. $V_{(ref)(1)} \leq V_{bias(ref)(2)}$ −1 V for best results in level shifting applications.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	T_A = −55°C to +125°C			Unit
			Min	Typ (Note 8)	Max	
V_{IK}	Input Clamping Voltage	I_I = −18 mA; $V_{I(EN)}$ = 0 V			−1.2	V
I_{IH}	High−Level Input Current	V_I = 5 V; $V_{I(EN)}$ = 0 V			5	μA
$C_{i(EN)}$	EN Pin Input Capacitance	V_I = 3 V or 0 V		7.1		pF
$C_{i/O(off)}$	OFF−State I/O Pin Capacitance SCLn, SDAn	V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		4	6	pF
$C_{i/O(on)}$	ON−State I/O Pin Capacitance SCLn, SDAn	V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		9.3	12.5	pF
R_{ON}	ON−State Resistance[2][3] SCLn, SDAn	V_I = 0 V; I_O = 64 mA $V_{I(EN)}$ = 4.5 V $V_{I(EN)}$ = 3 V $V_{I(EN)}$ = 2.3 V $V_{I(EN)}$ = 1.5 V		 2.4 3.0 3.8 9.0	 5.0 6.0 8.0 20	Ω
		V_I = 2.4 V; I_O = 15 mA $V_{I(EN)}$ = 4.5 V $V_{I(EN)}$ = 3 V		 4.8 46	 7.5 80	
		V_I = 1.7 V; I_O = 15 mA $V_{I(EN)}$ = 2.3 V		 40	 80	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

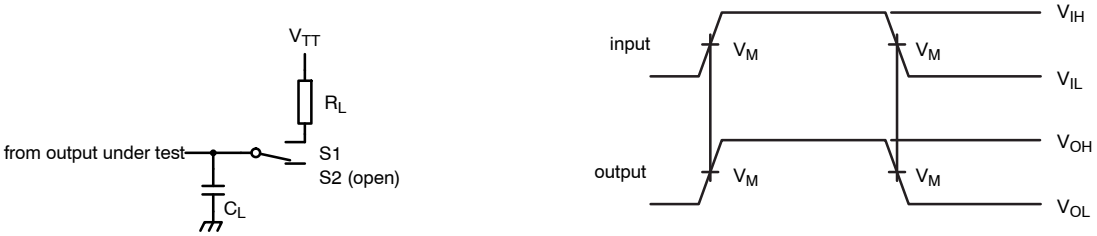
8. All typical values are at T_A = 25°C.
9. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON−state resistance is determined by the lowest voltage of the two terminals.
10. Guaranteed by design.

Table 6. AC ELECTRICAL CHARACTERISTICS (Translating Down) − Values Guaranteed by Design

Symbol	Parameter	Test Condition	Load Condition	T_A = −55°C to +125°C		Unit
				Min	Max	
SEE FIGURE 4 LOAD SWITCH AT S2 POSITION						
t_{PLH}	Low−to−High Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V	C_L = 15 pF	0	0.6	ns
			C_L = 30 pF	0	1.2	
			C_L = 50 pF	0	2.0	
t_{PHL}	High−to−Low Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1		C_L = 15 pF	0	0.75	
			C_L = 30 pF	0	1.5	
			C_L = 50 pF	0	2.0	
t_{PLH}	Low−to−High Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	$V_{I(EN)}$ = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V	C_L = 15 pF	0	0.6	ns
			C_L = 30 pF	0	1.2	
			C_L = 50 pF	0	2.0	
t_{PHL}	High−to−Low Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1		C_L = 15 pF	0	0.75	
			C_L = 30 pF	0	1.5	
			C_L = 50 pF	0	2.5	

Table 7. AC ELECTRICAL CHARACTERISTICS (Translating Up) − Values Guaranteed by Design

Symbol	Parameter	Test Condition	Load Condition	T_A = −55°C to +125°C Min	T_A = −55°C to +125°C Max	Unit
SEE FIGURE 4 LOAD SWITCH AT S1 POSITION						
t_{PLH}	Low−to−High Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_{TT} = 3.3 V; V_M = 1.15 V	R_L = 300 Ω, C_L = 15 pF	0	0.5	ns
			R_L = 300 Ω, C_L = 30 pF	0	1.0	
			R_L = 300 Ω, C_L = 50 pF	0	1.75	
t_{PHL}	High−to−Low Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2		R_L = 300 Ω, C_L = 15 pF	0	0.8	
			R_L = 300 Ω, C_L = 30 pF	0	1.65	
			R_L = 300 Ω, C_L = 50 pF	0	2.75	
t_{PLH}	Low−to−High Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_{TT} = 2.5 V; V_M = 0.75 V	R_L = 300 Ω, C_L = 15 pF	0	0.5	ns
			R_L = 300 Ω, C_L = 30 pF	0	1.0	
			R_L = 300 Ω, C_L = 50 pF	0	1.75	
t_{PHL}	High−to−Low Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2		R_L = 300 Ω, C_L = 15 pF	0	1.0	
			R_L = 300 Ω, C_L = 30 pF	0	2.0	
			R_L = 300 Ω, C_L = 50 pF	0	3.3	



A. Load Circuit

B. Timing Diagram

S1 = translating up; S2 = translating down.
C_L includes probe and jig capacitance.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2 ns; t_f ≤ 2 ns.
The outputs are measured one at a time, with one transition per measurement.

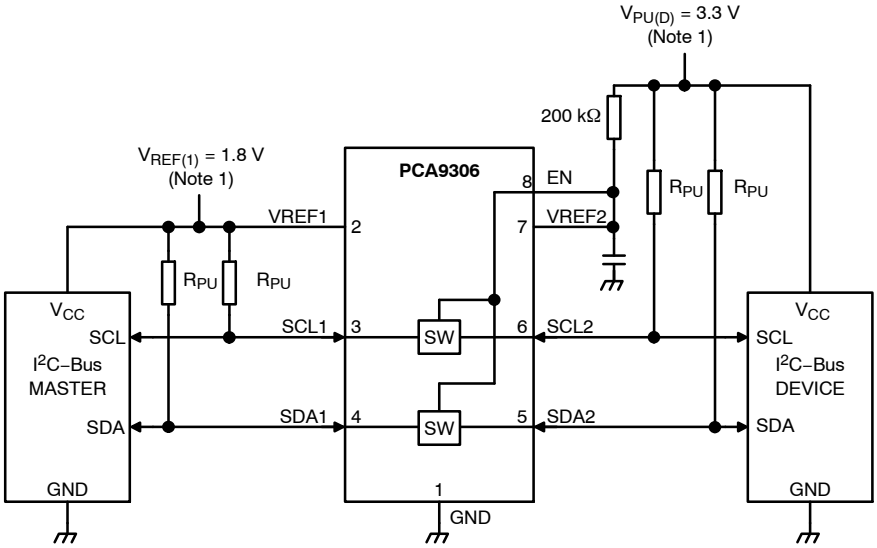
Figure 5. Load Circuit for Outputs

ORDERING INFORMATION

Device	Package	Shipping†
PCA9306DTR2G	TSSOP−8 (Pb−Free)	4000 / Tape & Reel
PCA9306AMUTCG	UQFN8 (Pb−Free)	3000 / Tape & Reel
NLVPCA9306AMUTCG*		
PCA9306FMUTAG	UDFN8 (Pb−Free)	3000 / Tape & Reel
PCA9306FMUTCG	UDFN8 (Pb−Free)	3000 / Tape & Reel
PCA9306USG	US8 (Pb−Free)	3000 / Tape & Reel
NLV9306USG*		

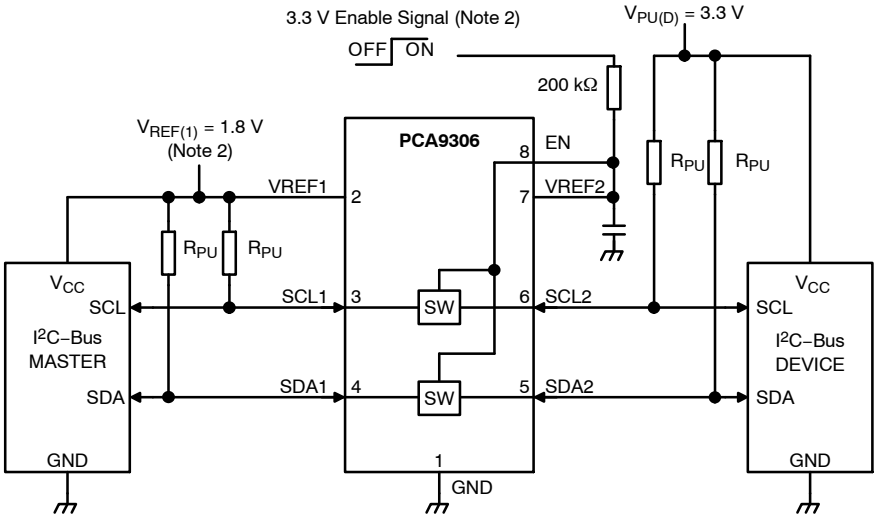
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

APPLICATION INFORMATION



1. The applied voltages at $V_{ref(1)}$ and $V_{pu(D)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Figure 6. Typical Application (Switch Always Enabled)



2. In the Enabled mode, the applied enable voltage and the applied voltage at $V_{ref(1)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Figure 7. Typical Application (Switch Enable Control)

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side $V_{pu(D)}$ through a pull−up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I^2C–bus master output can be totem−pole or open−drain (pull−up resistors may be required) and the I^2C–bus device output can be totem−pole or open−drain (pull−up resistors are required to pull the SCL2 and SDA2 outputs to $V_{pu(D)}$). However, if either output is totem−pole, data must be unidirectional or the outputs must be 3−stateable and be controlled by some direction−control mechanism to prevent HIGH−to−LOW contentions in either direction. If both outputs are open−drain, no direction control is needed.

The reference supply voltage ($V_{ref(1)}$) is connected to the processor core power supply voltage. When VREF2 is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V $V_{pu(D)}$ power supply, and $V_{ref(1)}$ is set between 1.0 V and ($V_{pu(D)}$ − 1 V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to $V_{pu(D)}$.

Table 8. APPLICATION OPERATING CONDITIONS Refer to Figure 6.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{bias(ref)(2)}$	Reference Bias Voltage (2)		$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{I(EN)}$	EN Pin Input Voltage		$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{ref(1)}$	Reference Voltage (1)		0	1.5	4.4	V
$I_{sw(pass)}$	Pass Switch Current			14		mA
I_{ref}	Reference Current	Transistor		5		μA
T_{amb}	Ambient Temperature	Operating in free−air	−55		+125	°C

11. All typical values are at T_{amb} = 25 °C.

Sizing Pull−up Resistor

The pull−up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pull−up resistor value is calculated as:

$$R_{PU} = \frac{V_{PU(D)} - 0.35\ V}{0.015\ A} \qquad \text{(eq. 1)}$$

The following table summarizes resistor reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor values shown in the +10% column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306 device at 0.175 V, although the 15 mA only applies to current flowing through the PCA9306 device.

Table 9. PULLUP RESISTOR VALUES Calculated for V_{OL} = 0.35 V; assumes output driver V_{OL} = 0.175 V at stated current.

	Pullup Resistor Value (Ω)					
	15 mA		10 mA		3 mA	
$V_{pu(D)}$	Nominal	+10% (Note 12)	Nominal	+10%[1]	Nominal	+10% (Note 12)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

12. +10% to compensate for V_{CC} range and resistor tolerance.

Maximum Frequency Calculation

The maximum frequency is totally dependent upon the specifics of the application and the device can operate > 33 MHz. Basically, the PCA9306 behaves like a wire with the additional characteristics of transistor device physics and should be capable of performing at higher frequencies if used correctly.

Here are some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306 close to the processor.
- The trace length should be less than half the time of flight to reduce ringing and reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher the drive strength (up to 15 mA), the higher the frequency the device can use.

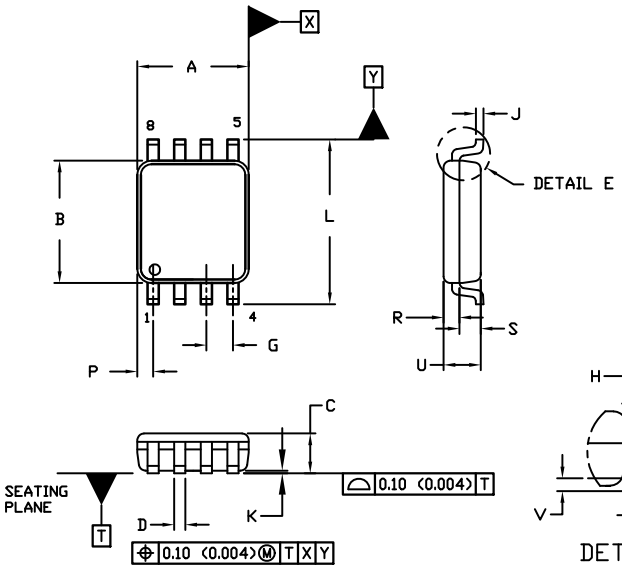
In a 3.3 V to 1.8 V direction level shift, if the 3.3 V side is being driven by a totem pole type driver no pull−up resistor is needed on the 3.3 V side. The capacitance and line length of concern is on the 1.8 V side since it is driven through the ON resistance of the PCA9306. If the line length on the 1.8 V side is long enough there can be a reflection at the chip/terminating end of the wire when the transition time is shorter than the time of flight of the wire because the PCA9306 looks like a high−impedance compared to the wire. If the wire is not too long and the lumped capacitance is not excessive the signal will only be slightly degraded by the series resistance added by passing through the PCA9306. If the lumped capacitance is large the rise time will deteriorate, the fall time is much less affected and if the rise time is slowed down too much the duty cycle of the clock will be degraded and at some point the clock will no longer be useful. So the principle design consideration is to minimize the wire length and the capacitance on the 1.8 V side for the clock path. A pull−up resistor on the 1.8 V side can also be used to trade a slower fall time for a faster rise time and can also reduce the overshoot in some cases.

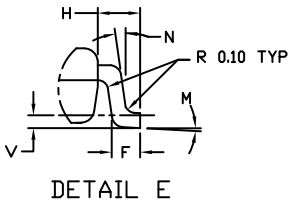
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 4 :1

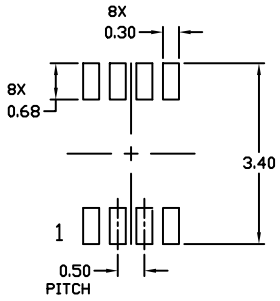
US8
CASE 493
ISSUE F

DATE 01 SEP 2021





DETAIL E



RECOMMENDED *
MOUNTING FOOTPRINT

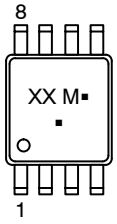
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0.0203 MM (0.003–0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON04475D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**US8**	**PAGE 1 OF 1**

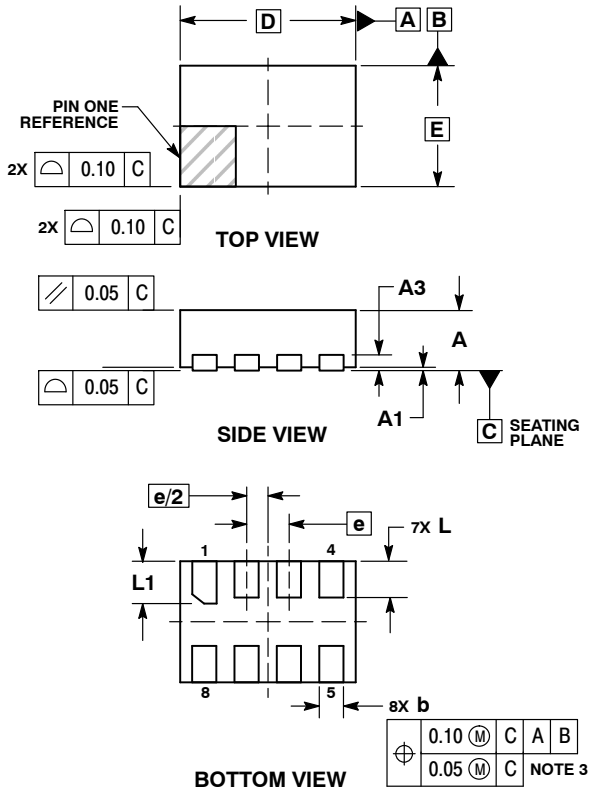
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

UDFN8, 1.45x1, 0.35P
CASE 517BZ−01
ISSUE O

SCALE 4:1

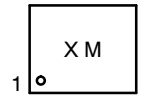
DATE 18 MAY 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

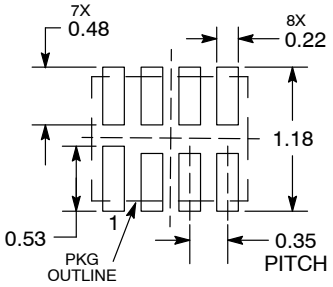
GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON56796E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**UDFN8, 1.45X1, 0.35P**	**PAGE 1 OF 1**

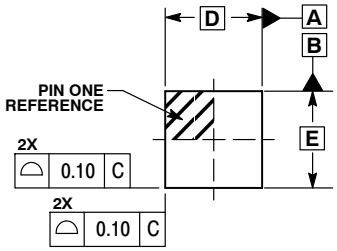
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

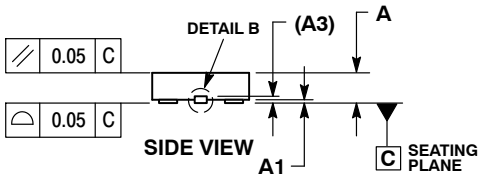
UQFN8, 1.6x1.6, 0.5P
CASE 523AN−01
ISSUE O

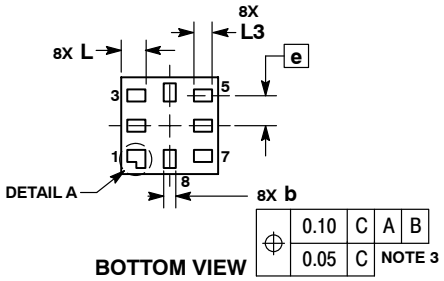
DATE 26 NOV 2008

SCALE 4:1

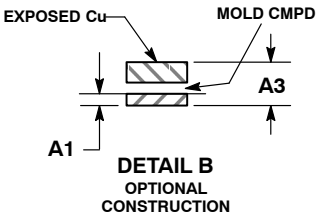


TOP VIEW

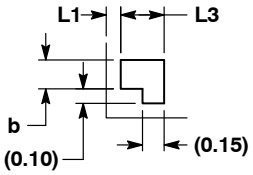




BOTTOM VIEW



DETAIL B
OPTIONAL CONSTRUCTION

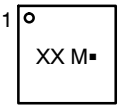


DETAIL A
OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	−−−	0.15
L3	0.25	0.35

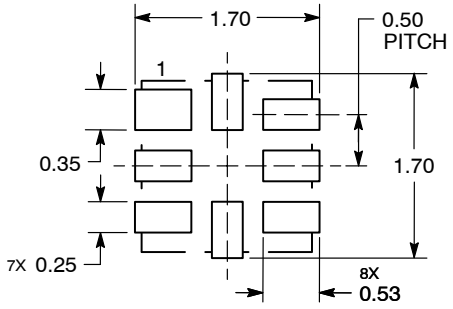
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*

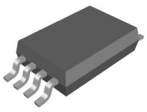


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

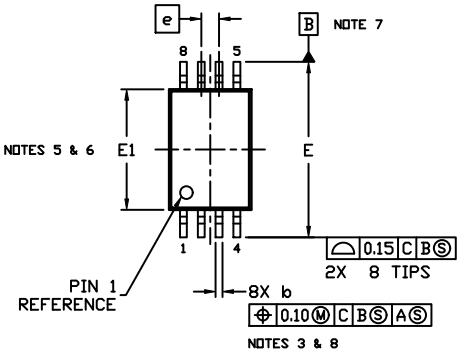
DOCUMENT NUMBER:	**98AON36348E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**8 PIN UQFN, 1.6X1.6, 0.5P**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

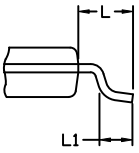


TSSOP8, 4.4x3.0, 0.65P
CASE 948AL
ISSUE A

DATE 20 MAY 2022



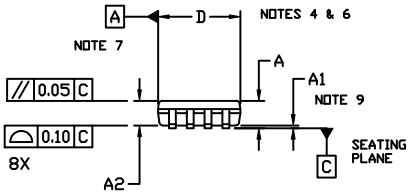
TOP VIEW



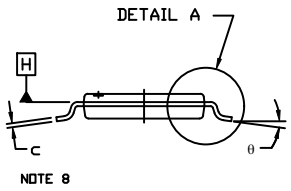
DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



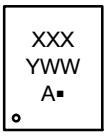
SIDE VIEW



END VIEW

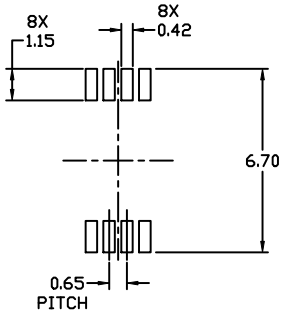
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
Y = Year
WW = Work Week
A = Assembly Location
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON34428E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP8, 4.4X3.0, 0.65P**	**PAGE 1 OF 1**

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