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FODM452, FODM453

5-Pin Mini Flat Package High Speed Transistor Optocoupler

Features

- Compact 5-pin mini flat package
- High speed-1 MBit/s
- Superior CMR-15kV/μs at $V_{CM} = 1500V$ (FODM453)
- Performance guaranteed over temperature (0–70°C)
- U.L. recognized (File # E90700)
- VDE0884 recognized (File # 136480)
 - Ordering option V, e.g., FODM452V
- 260°C reflow capability for Pb-free assembly

Applications

- Line receivers
- Pulse transformer replacement
- Output interface to CMOS-LSTTL-TTL
- Wide bandwidth analog coupling

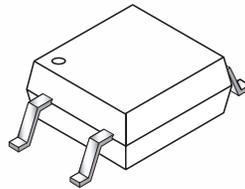
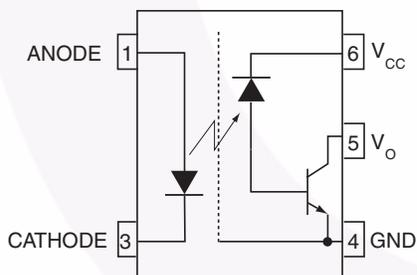
Description

The FODM452 and FODM453 optocouplers consist of an AlGaAs LED optically coupled to a high speed photo-detector transistor. The devices are housed in a compact 5-pin mini flat package for optimum mounting density. The FODM453 features a high CMR rating for optimum common mode transient immunity.

Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/FO/FODM611.html
- www.fairchildsemi.com/pf/FO/FODM8061.html
- www.fairchildsemi.com/pf/FO/FODM8071.html

Functional Schematic



Truth Table

LED	Output
Off	High
On	Low

Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V_O	Output Voltage
6	V_{CC}	Output Supply Voltage

Safety and Insulation Ratings for Mini-Flat Package (SO5 Pin)

As per IEC60747-5-2 (Pending Certification). This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For rated main voltage < 150Vrms		I-IV		
	For rated main voltage < 300Vrms		I-III		
	Climatic Classification		40/85/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC	1060			
V_{PR}	Input to Output Test Voltage, Method a, $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test with $t_m = 60$ sec, Partial Discharge < 5 pC	848			
V_{IORM}	Max Working Insulation Voltage	565			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	4000			V_{peak}
	External Creepage	5.0			mm
	External Clearance	5.0			mm
	Insulation thickness	0.5			mm
T_{Case}	Safety Limit Values, Maximum Values allowed in the event of a failure, Case Temperature	150			°C
R_{IO}	Insulation Resistance at T_S , $V_{IO} = 500V$	10^9			Ω

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +85	$^\circ\text{C}$
EMITTER			
I_F (avg)	DC/Average Forward Input Current	25	mA
I_F (pk)	Peak Forward Input Current (50% duty cycle, 1ms P.W.)	50	mA
I_F (trans)	Peak Transient Input Current ($\leq 1\mu\text{s}$ P.W., 300pps)	1.0	A
V_R	Reverse Input Voltage	5	V
P_D	Input Power Dissipation (No derating required over specified operating temp range)	45	mW
DETECTOR			
I_O (avg)	Average Output Current	8	mA
I_O (pk)	Peak Output Current	16	mA
V_{CC}	Supply Voltage	-0.5 to 30	V
V_O	Output Voltage	-0.5 to 20	V
P_D	Output Power Dissipation (No derating required over specified operating temp range)	100	mW

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max.	Unit
EMITTER						
V _F	Input Forward Voltage	I _F = 16mA, T _A = 25°C		1.60	1.7	V
		I _F = 16mA			1.8	
B _{VR}	Input Reverse Breakdown Voltage	I _R = 10μA	5.0			V
ΔV _F /ΔT _A	Temperature Coefficient of Forward Voltage	I _F = 16mA		-1.8		mV/°C
DETECTOR						
I _{OH}	Logic High Output Current	I _F = 0mA, V _O = V _{CC} = 5.5V, T _A = 25°C		.001	0.5	μA
		I _F = 0 mA, V _O = V _{CC} = 15V, T _A = 25°C		.001	1	
		I _F = 0mA, V _O = V _{CC} = 15V			50	
I _{CCL}	Logic Low Supply Current	I _F = 16mA, V _O = Open, V _{CC} = 15V		100	200	μA
I _{CCH}	Logic high supply current	I _F = 0 mA, V _O = Open, V _{CC} = 15V, T _A = 25°C		0.05	1	μA
		I _F = 0mA, V _O = Open, V _{CC} = 15V			2	

Transfer Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.*	Max	Unit	
COUPLED							
CTR	Current Transfer Ratio ⁽¹⁾	I _F = 16mA, V _{CC} = 4.5V	T _A = 25°C V _{OL} =0.4V	20		50	%
			V _{OL} =0.5V	15			
V _{OL}	Logic LOW Output Voltage	I _F = 16mA, I _O = 3mA, V _{CC} = 4.5V, T _A = 25°C			0.4	V	
		I _F = 16mA, I _O = 2.4mA, V _{CC} = 4.5 V			0.5		

Switching Characteristics (V_{CC} = 5V)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.*	Max.	Unit
T _{PHL}	Propagation Delay Time to Logic LOW	R _L = 1.9kΩ, I _F = 16mA, T _A = 25°C ⁽²⁾ (Fig. 9)			0.40	0.8	μs
		R _L = 1.9kΩ, I _F = 16mA ⁽²⁾ (Fig. 9)				1.0	
T _{PLH}	Propagation Delay Time to Logic HIGH	R _L = 1.9kΩ, I _F = 16mA, T _A = 25°C ⁽²⁾ (Fig. 9)			0.35	0.8	μs
		R _L = 1.9kΩ, I _F = 16mA ⁽²⁾ (Fig. 9)				1.0	
CM _H	Common Mode Transient Immunity at Logic HIGH	I _F = 0mA, V _{CM} = 10V _{P-P} , R _L = 1.9kΩ, T _A = 25°C ⁽³⁾ (Fig. 10)	FODM452	5	15		KV/μs
		I _F = 0mA, V _{CM} = 1500V _{P-P} , R _L = 1.9kΩ, T _A = 25°C ⁽³⁾ (Fig. 10)	FODM453	15	40		KV/μs
CM _L	Common Mode Transient Immunity at Logic LOW	I _F = 16mA, V _{CM} = 10V _{P-P} , R _L = 1.9kΩ, T _A = 25°C ⁽³⁾ (Fig. 10)	FODM452	5	15		KV/μs
		I _F = 16mA, V _{CM} = 1500V _{P-P} , R _L = 1.9kΩ, T _A = 25°C ⁽³⁾ (Fig. 10)	FODM453	15	40		KV/μs
BW	Bandwidth	R _L = 100Ω			3		MHz

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Typ.*	Max.	Unit
V _{ISO}	Withstand Insulation Test Voltage	RH ≤ 50%, T _A = 25°C, t = 1 min. ⁽⁴⁾	3750			V _{RMS}
C _{I-O}	Capacitance (Input to Output)	f = 1MHz ⁽⁴⁾		0.2		pF

*All Typicals at T_A = 25°C

Notes:

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
2. The 1.9k Ω load represents 1 TTL unit load of 1.6mA and 5.6k Ω pull-up resistor.
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0V$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8V$).
4. Device is considered a two terminal device: Pins 1, and 3 are shorted together and Pins 4, 5, and 6 are shorted together.

Typical Performance Curves

Fig. 1 Input Forward Current vs Forward Voltage

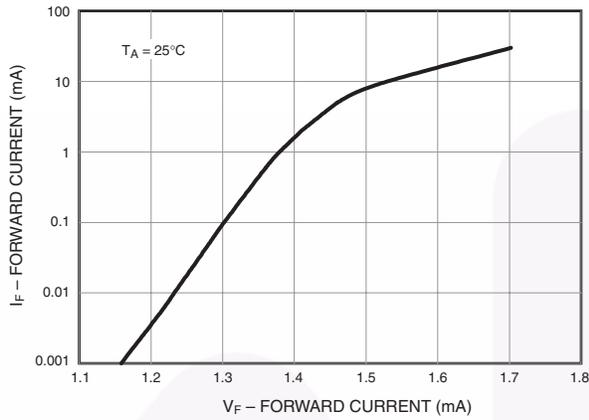


Fig. 2 Normalized Current Transfer Ratio vs. Input Current

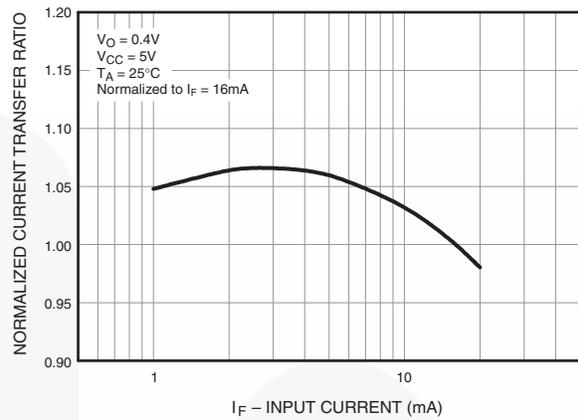


Fig. 3 Normalized Current Transfer Ratio vs. Ambient Temperature

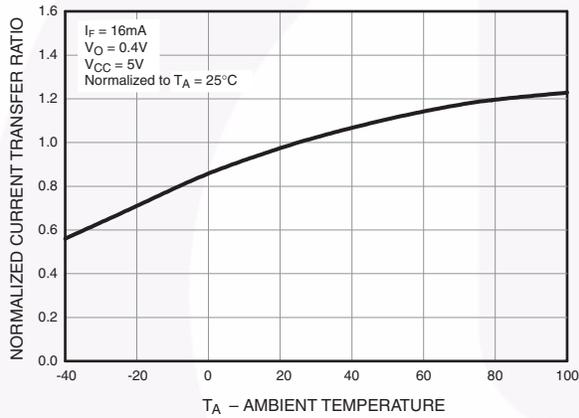


Fig. 4 Logic High Output Current vs. Ambient Temperature

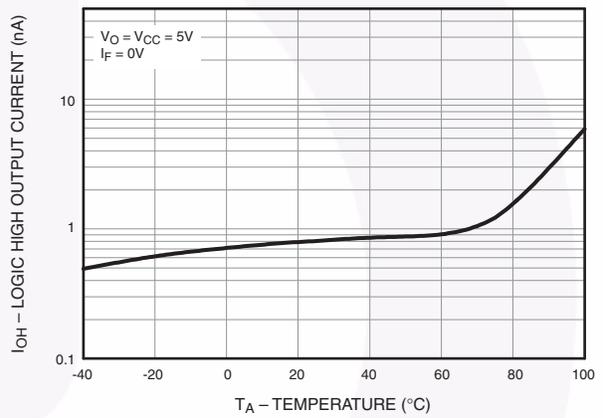


Fig. 5 DC and Pulsed Transfer Characteristics

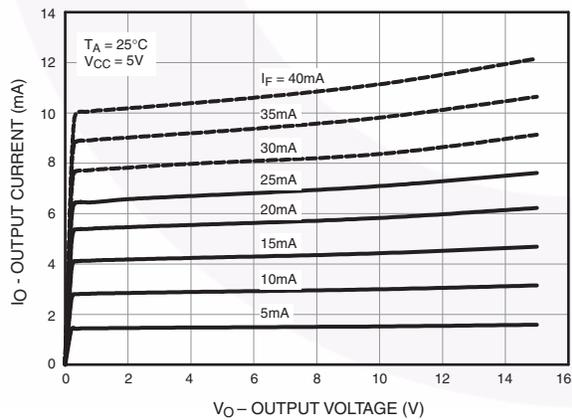
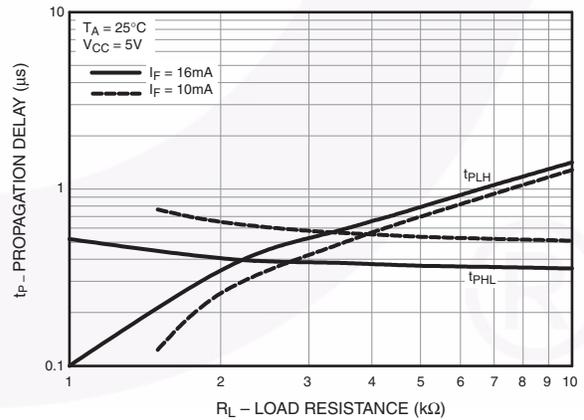


Fig. 6 Propagation Delay vs. Load Resistance



Typical Performance Curves (Continued)

Fig. 7 Propagation Delay vs. Ambient Temperature

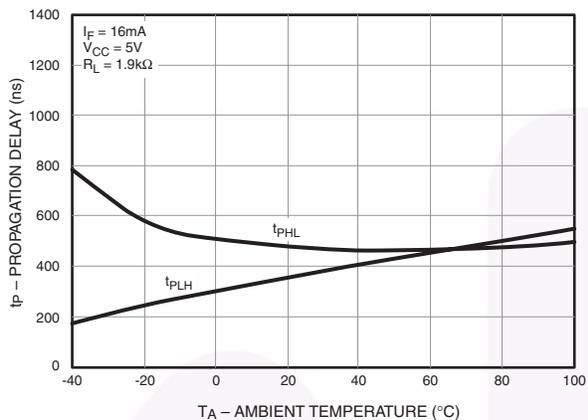
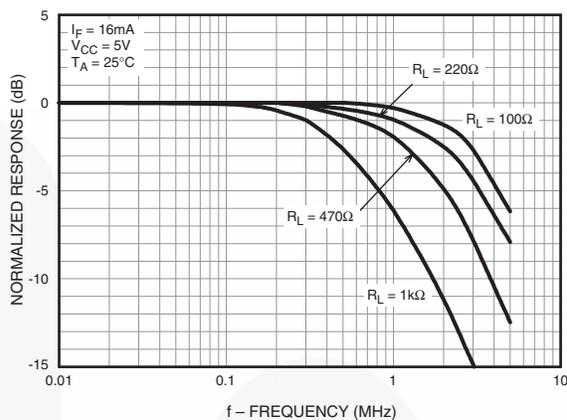


Fig. 8 Frequency Response



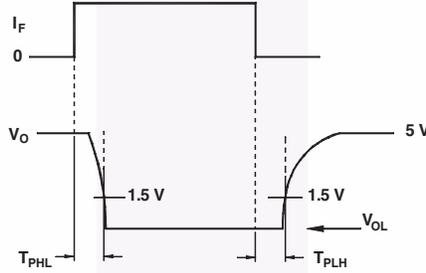
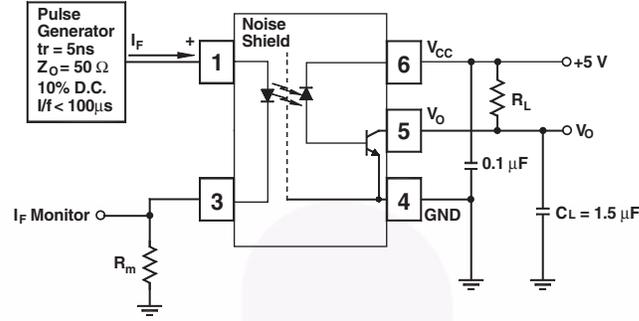
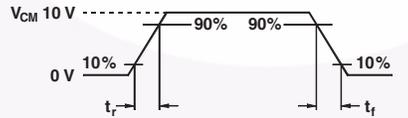
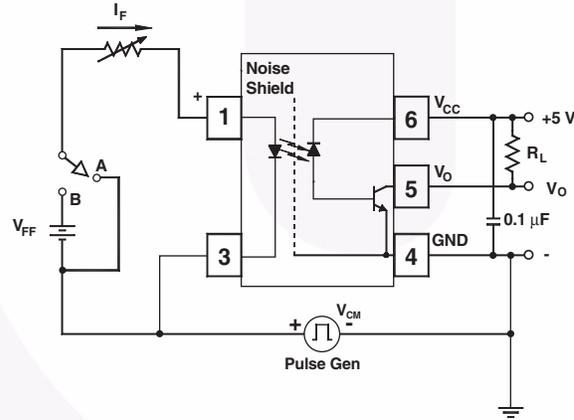


Fig. 9 Switching Time Test Circuit

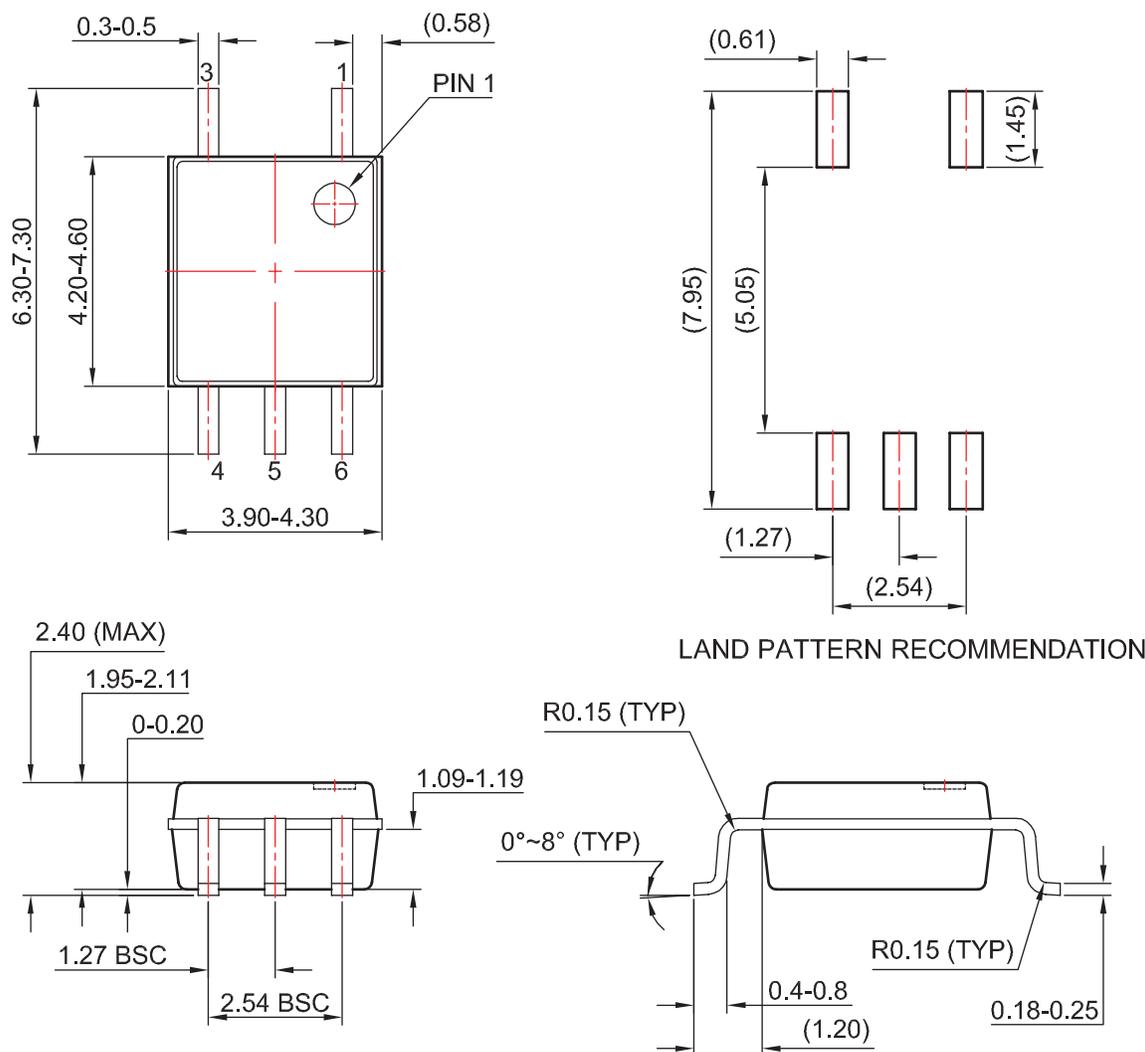


V_O — 5 V
Switch at A : $I_F = 0$ mA

V_O — V_{OL}
Switch at A : $I_F = 16$ mA

Fig. 10 Common Mode Immunity Test Circuit

Package Dimensions



Notes:

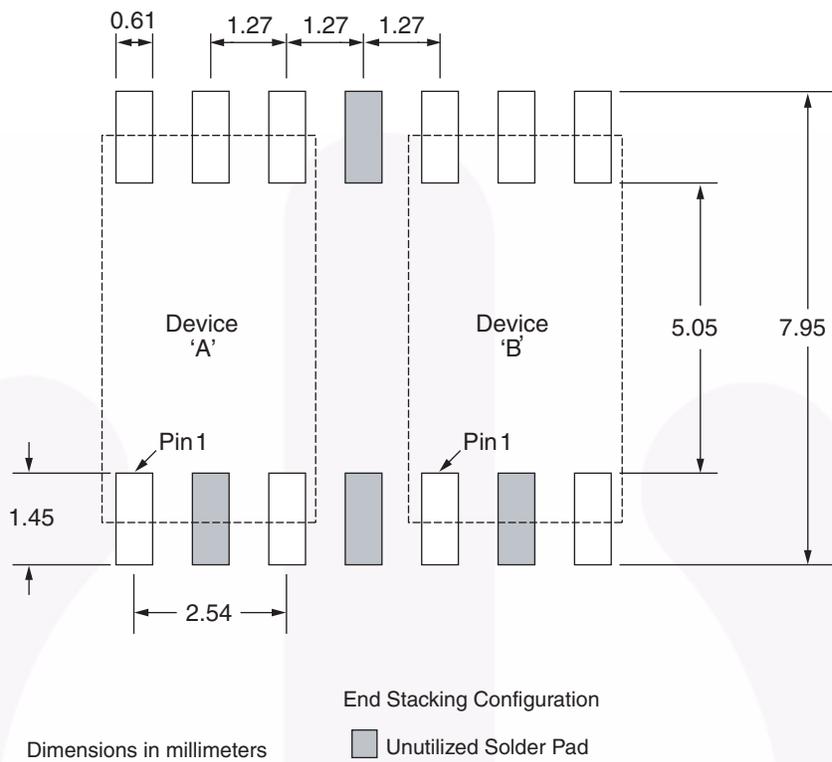
1. No standard applies to this package.
2. All dimensions are in millimeters.
3. Dimensions are exclusive of burrs, mold flash, and tie bar extrusion.
4. Drawings filename and revision: MKT-MFP05A.

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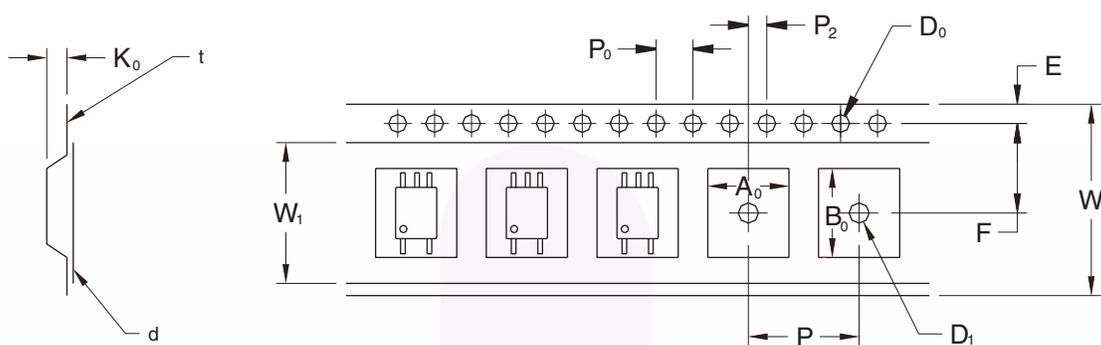
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<http://www.fairchildsemi.com/packaging/>

Footprint Drawing for PCB Layout



Tape and Reel Dimensions

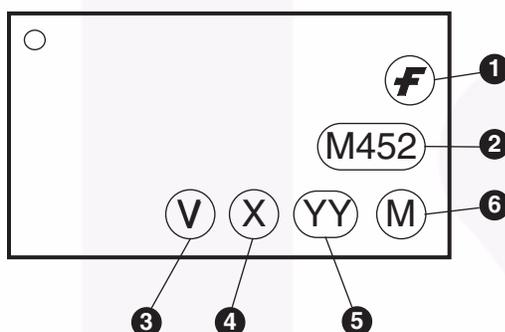


		2.54 Pitch
Description	Symbol	Dimensions (mm)
Tape Width	W	12.00 +0.30/-0.10
Tape Thickness	t	0.30 ±0.05
Sprocket Hole Pitch	P ₀	4.00 ±0.10
Sprocket Hole Diameter	D ₀	1.50 +0.10/-0.0
Sprocket Hole Location	E	1.75 ±0.10
Pocket Location	F	5.50 ±0.10
	P ₂	2.00 ±0.10
Pocket Pitch	P	8.00 ±0.10
Pocket Dimension	A ₀	4.40 ±0.10
	B ₀	7.30 ±0.10
	K ₀	2.30 ±0.10
Pocket Hole Diameter	D ₁	1.50 Min.
Cover Tape Width	W ₁	9.20
Cover Tape Thickness	d	0.065 ±0.010
Max. Component Rotation or Tilt		10° Max.
Devices Per Reel		2500
Reel Diameter		330mm (13")

Ordering Information

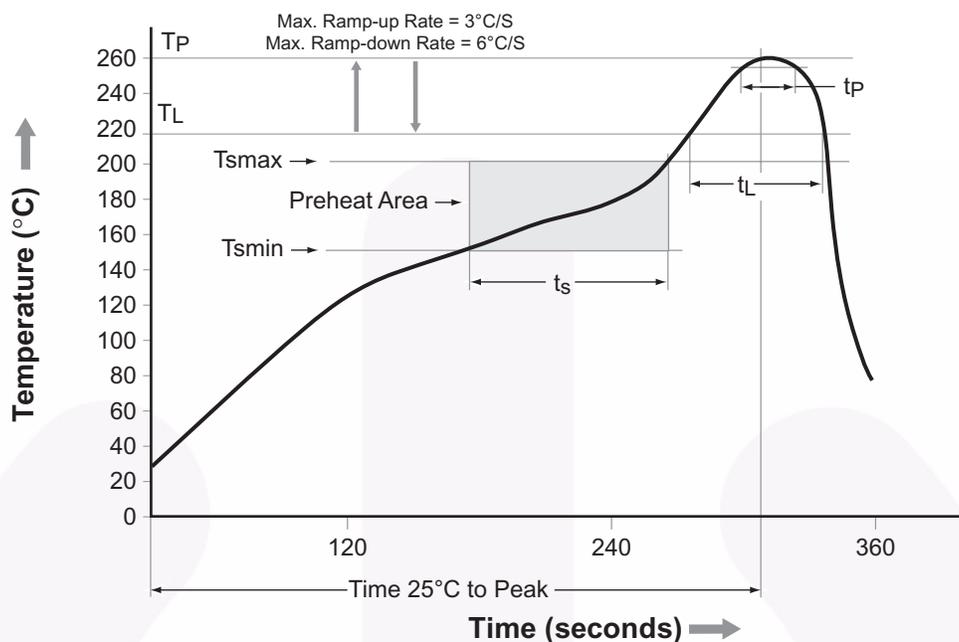
Option	Order Entry Identifier (example)	Description
R2	FODM452R2	Tape and Reel (2500 per reel)
V	FODM452V	IEC60747-5-2
R2V	FODM452R2V	IEC60747-5-2, Tape and Reel (2500 per reel)

Marking Information



Definitions	
1	Fairchild logo
2	Device number
3	IEC60747-5-2 mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	One digit year code, e.g., '7'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60–120 seconds
Ramp-up Rate (tL to tP)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.



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SuperSOT™-6
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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