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# FDMS86540

## N-Channel PowerTrench<sup>®</sup> MOSFET

60 V, 129 A, 3.4 mΩ

### Features

- Max  $r_{DS(on)}$  = 3.4 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 20\text{ A}$
- Max  $r_{DS(on)}$  = 4.1 mΩ at  $V_{GS} = 8\text{ V}$ ,  $I_D = 18.5\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

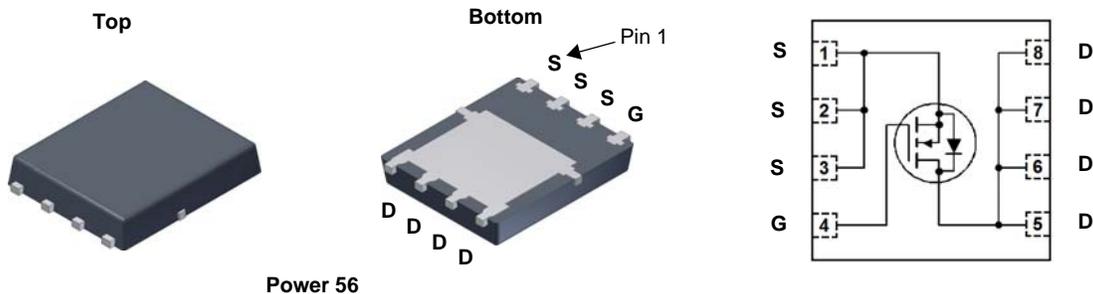


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- Primary Switch in isolated DC-DC
- Synchronous Rectifier
- Load Switch



Power 56

### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	129
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	82
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	20
	-Pulsed	(Note 4)	642
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	228
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	96
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86540	FDMS86540	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		28		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-11		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		2.7	3.4	m $\Omega$
		$V_{GS} = 8\text{ V}, I_D = 18.5\text{ A}$		3.1	4.1	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$		3.8	4.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		73		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		4837	6435	pF
$C_{oss}$	Output Capacitance			1413	1880	pF
$C_{rss}$	Reverse Transfer Capacitance			50	90	pF
$R_g$	Gate Resistance			1.0		$\Omega$

### Switching Characteristics

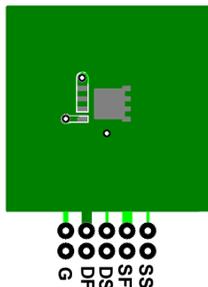
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		28	45	ns
$t_r$	Rise Time			16	29	ns
$t_{d(off)}$	Turn-Off Delay Time			32	52	ns
$t_f$	Fall Time			7.2	15	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$	$V_{DD} = 30\text{ V},$ $I_D = 20\text{ A}$	65	90	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 8\text{ V}$		53	75	nC
$Q_{gs}$	Gate to Source Charge			23		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			12		nC

### Drain-Source Diode Characteristics

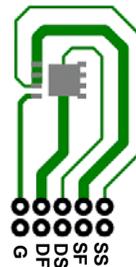
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.70	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ (Note 2)		0.79	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		55	88	ns
$Q_{rr}$	Reverse Recovery Charge			41	66	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		44	70	ns
$Q_{rr}$	Reverse Recovery Charge			76	122	nC

#### Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a)  $50\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width  $< 300\text{ }\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 39\text{ A}$ ,  $V_{DD} = 54\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 57\text{ A}$ .

4. Pulse  $I_d$  please refer to SOA curve for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

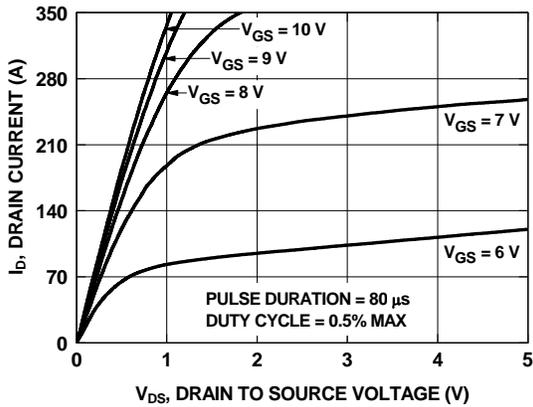


Figure 1. On-Region Characteristics

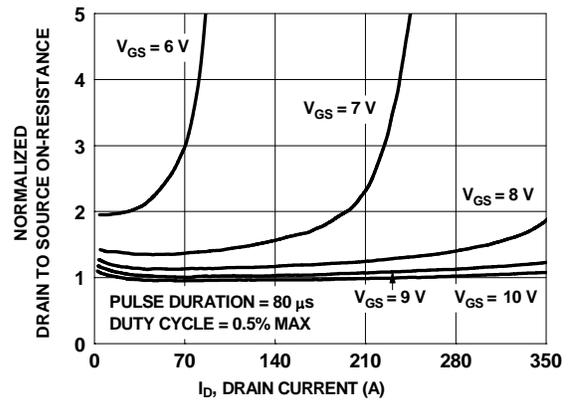


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

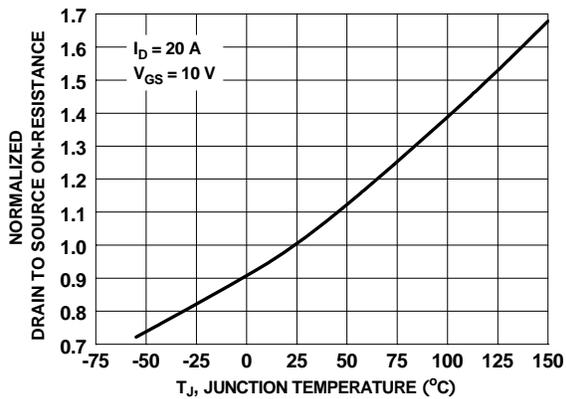


Figure 3. Normalized On-Resistance vs. Junction Temperature

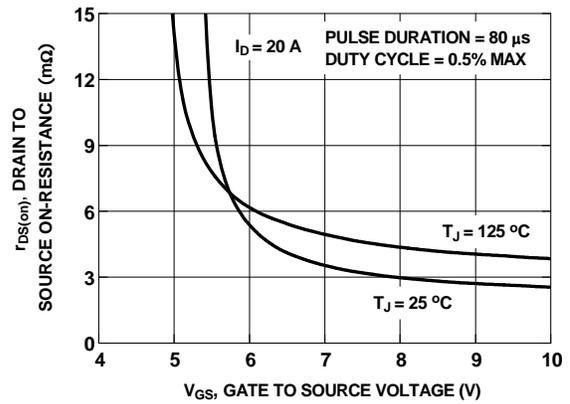


Figure 4. On-Resistance vs. Gate to Source Voltage

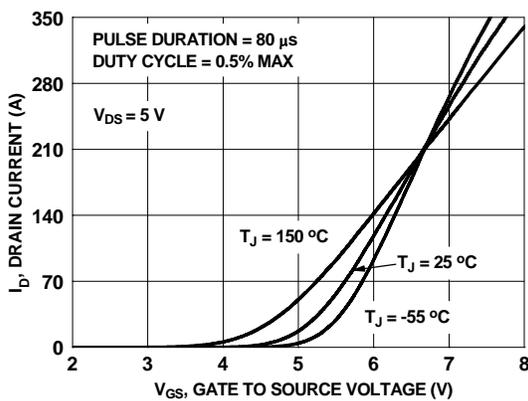


Figure 5. Transfer Characteristics

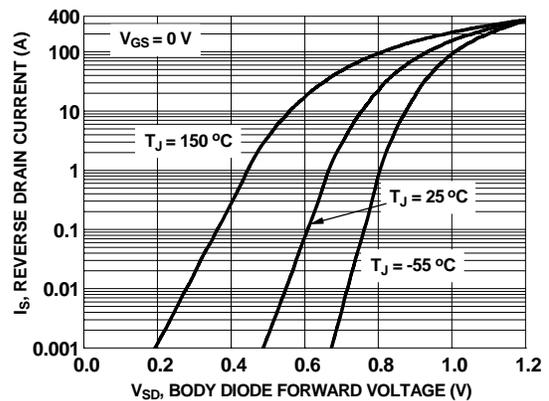
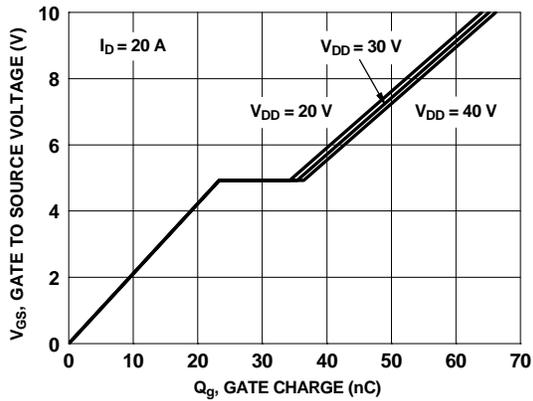
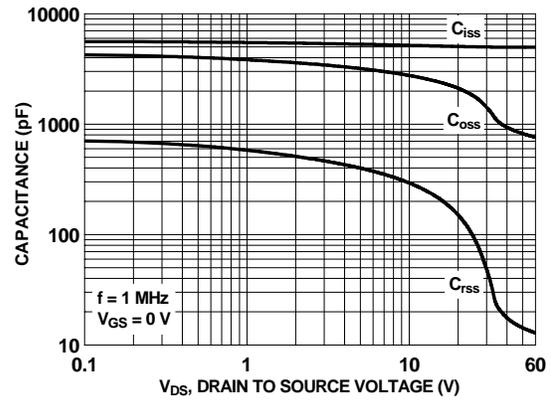


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

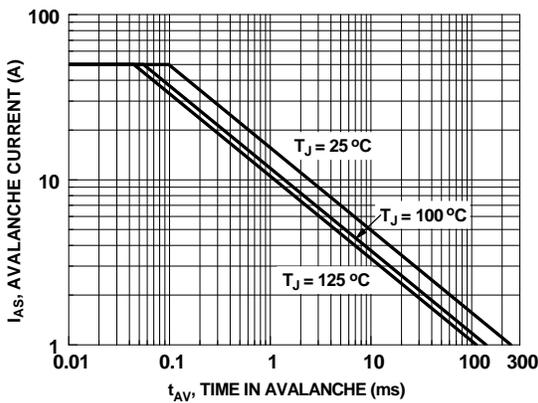
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



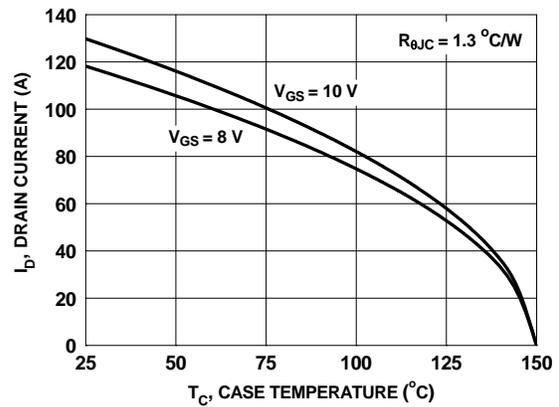
**Figure 7. Gate Charge Characteristics**



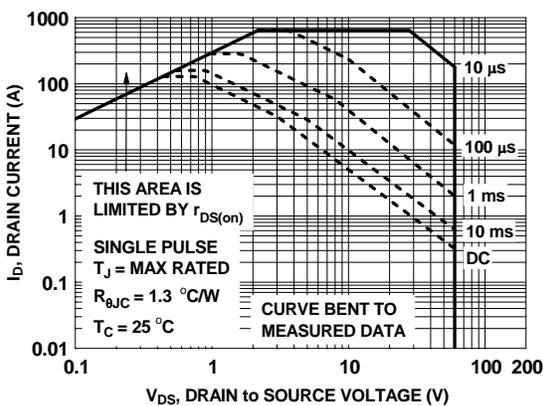
**Figure 8. Capacitance vs. Drain to Source Voltage**



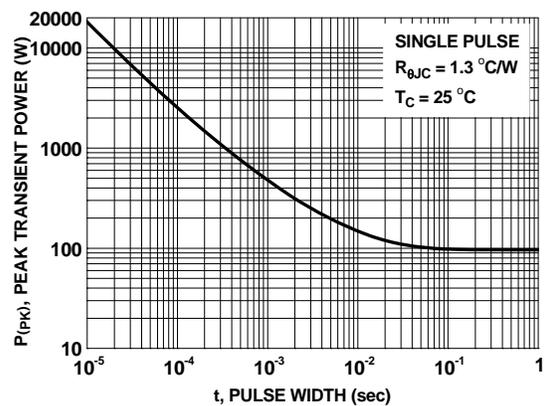
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

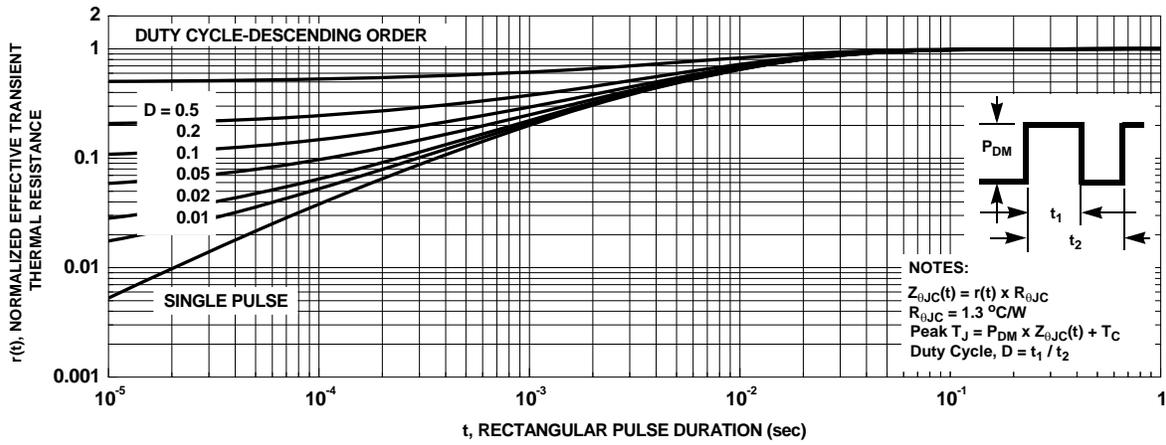


**Figure 11. Forward Bias Safe Operating Area**



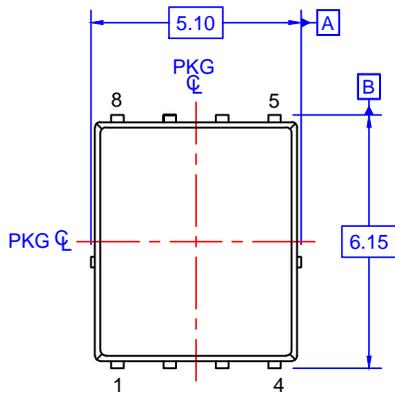
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

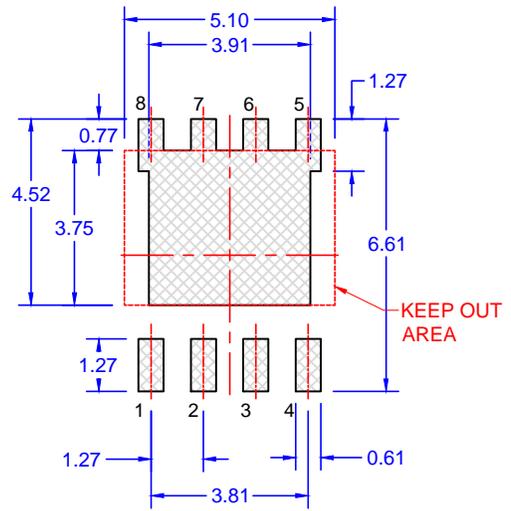
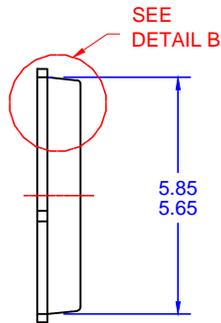


**Figure 13. Junction-to-Case Transient Thermal Response Curve**

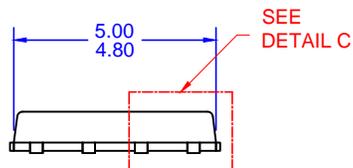
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CASE 483AE  
ISSUE A



TOP VIEW

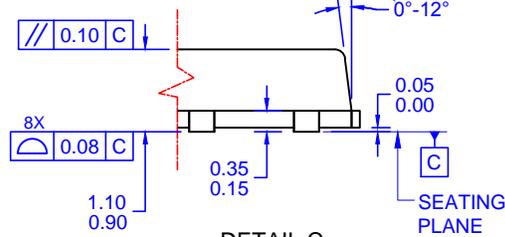


LAND PATTERN RECOMMENDATION

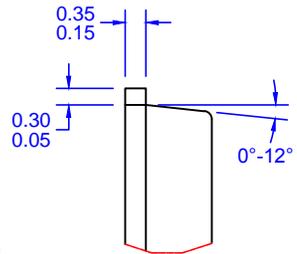


SIDE VIEW

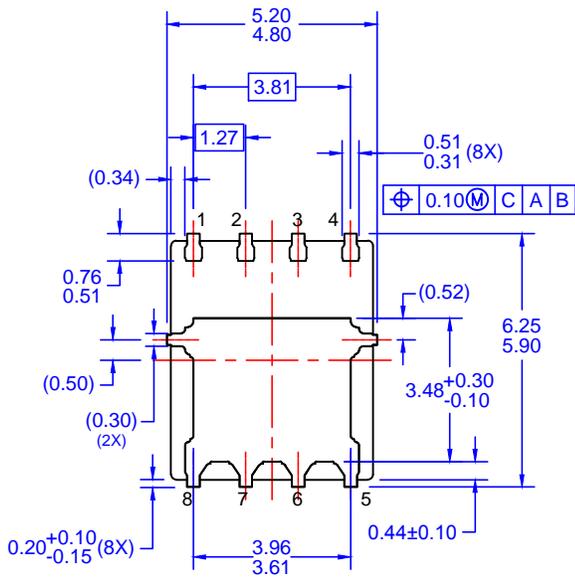
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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