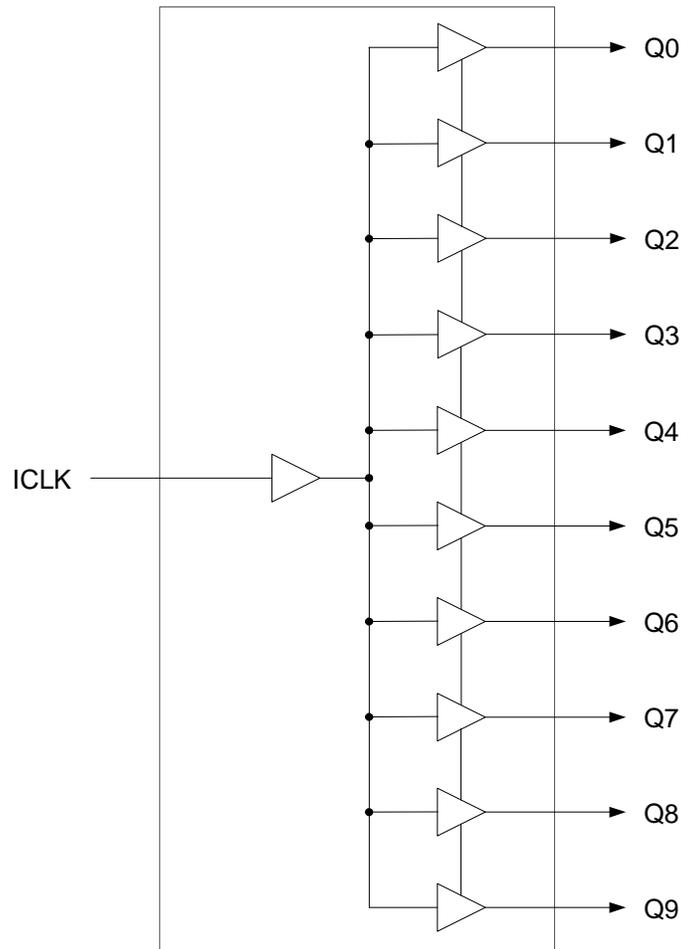## Description

The 74FCT3807S is a low skew, single input to ten output, clock buffer. The 74FCT3807S has best in class additive phase Jitter of sub 50 fsec.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.
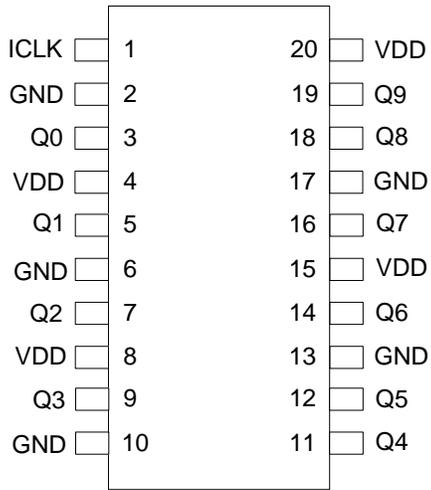
Features

- Low additive phase jitter RMS: 50fs
- Low skew outputs (50ps)
- Packaged in 20-pin TSSOP, SSOP, QSOP and VFQFPN packages, Pb (lead) free
- Operating voltages of 1.8V to 3.3V
- Input/Output clock frequency up to 200 MHz
- Advanced, low power CMOS process
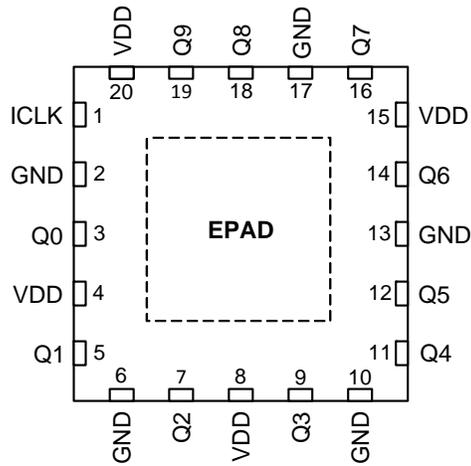- Extended temperature range (-40°C to +105°C)

Block Diagram

Pin Assignments

20-pin TSSOP/SSOP/QSOP

20-pin VFQFPN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input.
2	GND	Power	Connect to ground.
3	Q0	Output	Clock output 0.
4	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
5	Q1	Output	Clock output 1.
6	GND	Power	Connect to ground.
7	Q2	Output	Clock Output 2.
8	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
9	Q3	Output	Clock Output 3.
10	GND	Power	Connect to ground.
11	Q4	Output	Clock Output 4.
12	Q5	Output	Clock Output 5.
13	GND	Power	Connect to ground.
14	Q6	Output	Clock Output 6.
15	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
16	Q7	Output	Clock Output 7.
17	GND	Power	Connect to ground.
18	Q8	Output	Clock Output 8.
19	Q9	Output	Clock Output 9.
20	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD pins and GND pins, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 74FCT3807S is capable of, careful attention must be paid to board layout. Essentially, all ten outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 74FCT3807S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Outputs	-0.5 V to VDD+0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40° to +105°C
Storage Temperature	-65° to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics
(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -10 mA	1.3			V
Output Low Voltage	V_{OL}	I_{OL} = 10 mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	1.8			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		45		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.2			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		55		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

AC Electrical Characteristics
(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, C_L=5 pF		1.4	1.9	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, C_L=5 pF		1.4	1.9	ns
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, C_L=5 pF		1.0	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, C_L=5 pF		1.0	1.5	ns
Propagation Delay		Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, C_L=5 pF		0.6	1.0	ns
Propagation Delay		Note 1	1.5	2.5	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2		50	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

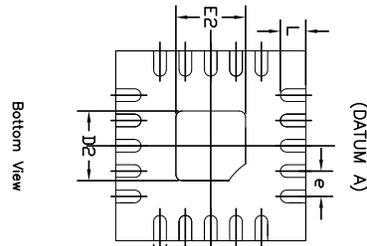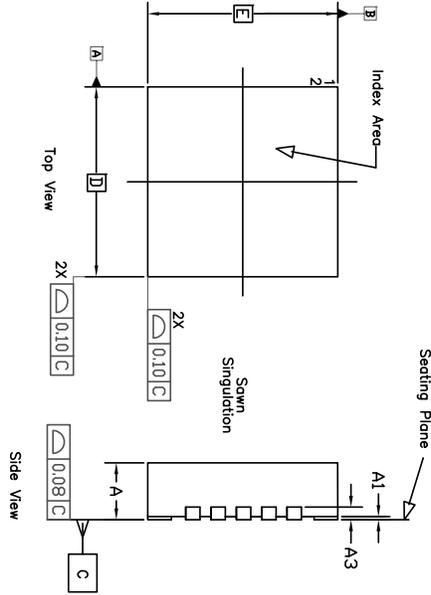## Test Load and Circuit

Marking Diagrams

20-pin TSSOP/SSOP/QSOP

20-pin VFQFPN
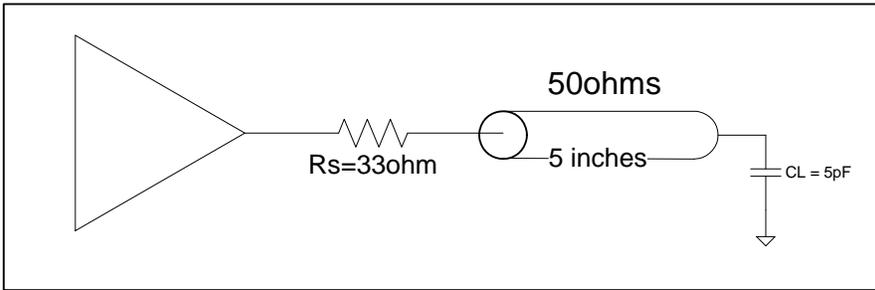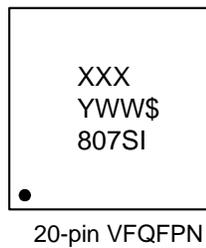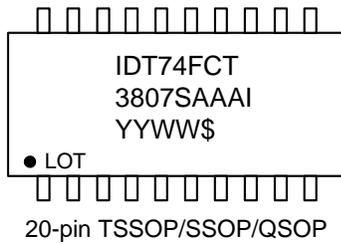
Notes:

1. "LOT" denotes the lot number.

2. "XXX" denotes the lot number.

3. "YYWW" or "YWW" are the last digits of the year and week that the part was assembled.

4. "$" denotes mark code.

5. "I" denotes extended temperature range device.

6. "AAA" denotes package code.

Package Outline and Package Dimensions (20-pin VFQFPN)

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
   COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

Top View

Side View

Bottom View

Index Area

Seating Plane

Sawn Singulation

(DATUM A)

(DATUM B)

COMMON DIMENSION

Symbol	DIMENSION		
	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	0.20 Ref		
b	0.17	0.20	0.25
e	0.40 BASIC		
N	20		
ND	5		
NE	5		
D	3.00 BASIC		
E	3.00 BASIC		
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
L	0.30	0.40	0.50

EPAD OPTION

Symbol	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
E2	0.95	1.10	1.25	1.55	1.65	1.75
D2	0.95	1.10	1.25	1.55	1.65	1.75

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/14/08	RC
01	ADD EPAD OPTION	11/28/12	RC
02	COMBINE POD & LAND PATTERN	12/5/13	J.HUA
03	Change Dimension aaa	7/14/14	J.HUA

TOLERANCES UNLESS SPECIFIED
DECIMAL
X± ANGULAR ±1°
XX±
XXX±

APPROVALS	DATE
DRAWN R.L.C	11/14/08
CHECKED	

www.IDT.com ®
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE ND/NDG 20 PACKAGE OUTLINE QFN 3.0 x 3.0 mm BODY, 0.40 PITCH

SIZE C

DRAWING No. PSC-4179

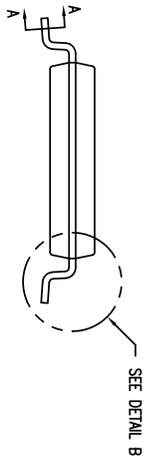REV 03

SHEET 1 OF 2

DO NOT SCALE DRAWING

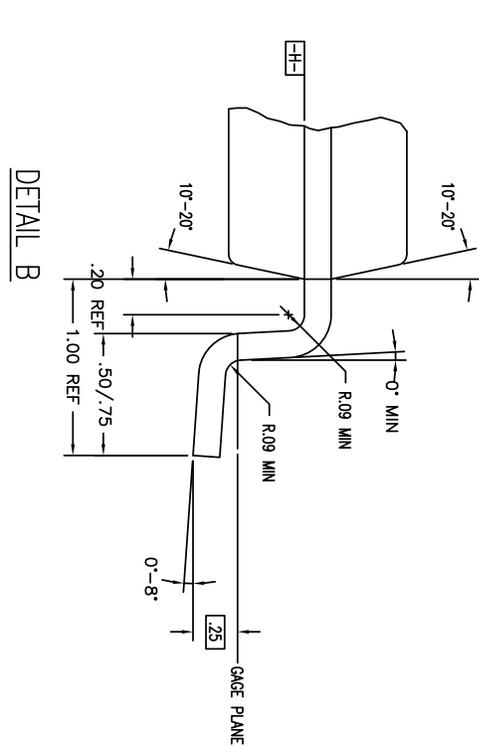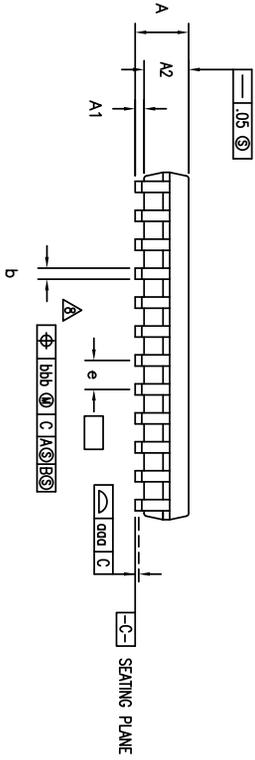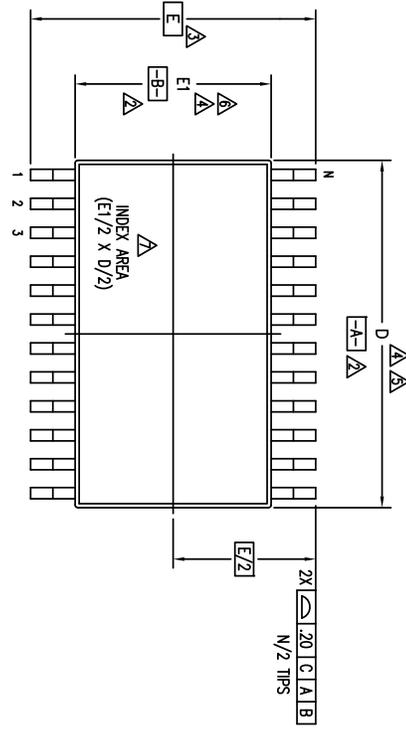# Package Outline and Package Dimensions, cont. (20-pin VFQFPN)
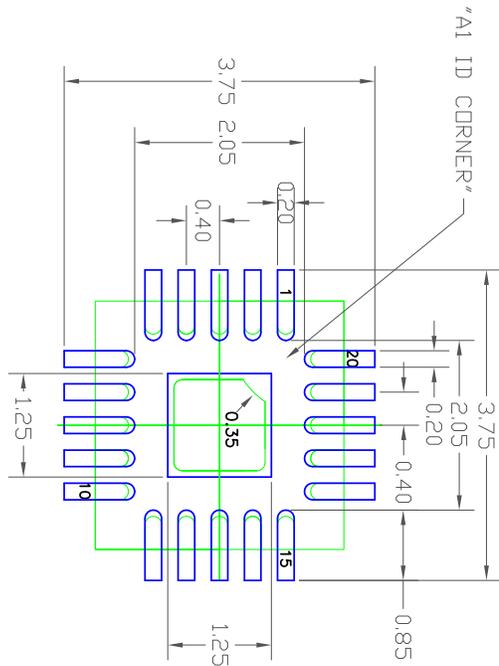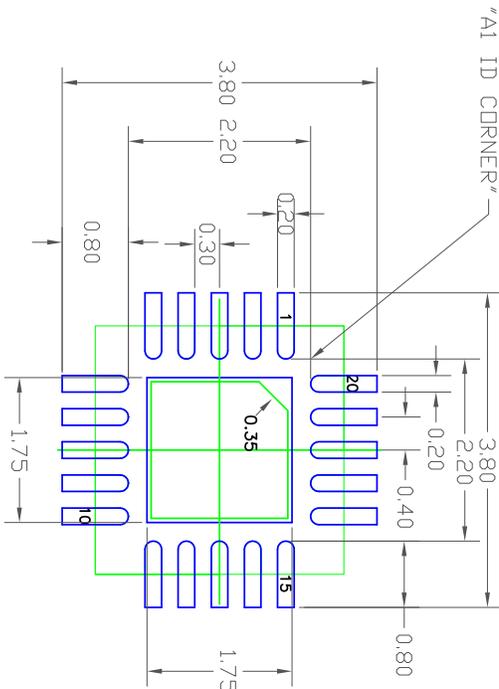
EPAD 1.1 mm SQ

RECOMMENDED LAND PATTERN DIMENSION

EPAD 1.65 mm SQ

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
   FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Outline and Package Dimensions (20-pin TSSOP)

SECTION A–A

.09/.20

b1
b
REF

.09/.16

WITH PLATING
BASE METAL

DETAIL B

SEE DETAIL B

SEATING PLANE

INDEX AREA
(E1/2 X D/2)

N/2 TIPS

10°–20'
10°–20'
.20 REF
1.00 REF
.50/.75
R.09 MIN
R.09 MIN
0° MIN
0°–8'
.25
GAGE PLANE

TOLERANCES
UNLESS SPECIFIED
DECIMAL   ANGULAR
XX±   ±
XXX±
XXXX±

APPROVALS	DATE
DRAWN JY	01/15/96
CHECKED	

www.IDT.com
2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727–6116
FAX: (408) 492–8674

TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C

DRAWING No.
PSC–4056

REV 06

SHEET 1 OF

DO NOT SCALE DRAWING

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

△2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

△3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

△4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

△5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

△6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

△7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

△8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

△9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10. ALL DIMENSIONS ARE IN MILLIMETERS

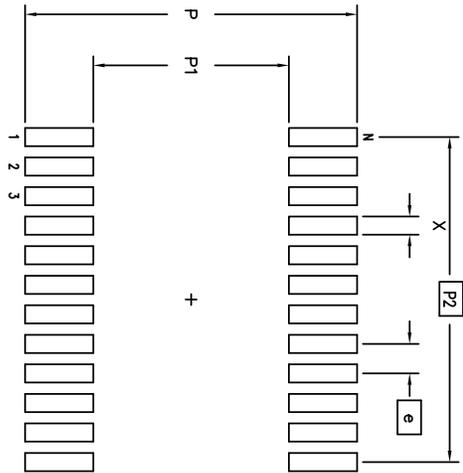11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

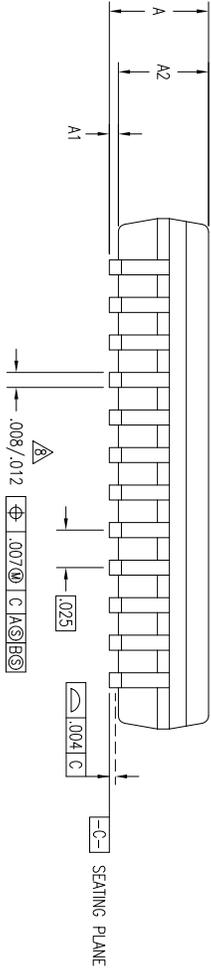| PG/PGG20						
JEDEC VARIATION				AC		
		MIN	NOM	MAX	N	
A	-	-	1.20			
A1	.05	-	.15			
A2	.80	1.00	1.05			
b	-	-	-			
D	6.40	6.50	6.60	4.5		
E	6.40 BSC			3		
E1	4.30	4.40	4.50	4.6		
e	.65 BSC					
L	-	-	-			
L1	.19	-	.30			
N	20					

LAND PATTERN DIMENSIONS

	MIN	MAX
	7.20	7.40
	4.20	4.40
	5.85 BSC	
	.30	.50
	.65 BSC	
	20	

Package Outline and Package Dimensions (20-pin QSOP)

SECTION A-A

.007/.010

.008/.012 REF

.008/.011

.007/.009

WITH PLATING

BASE METAL

A

A2

A1

.008/.012

.007 M C A(S)B(S)

.025

.004 C

-C- SEATING PLANE

E

.010 M C A(S)B(S)

-B-

E1

.120 MAX

.080 MAX

1 2 3

N

INDEX AREA

-A-

D

A

A

.010
.016 X 45°

DETAIL B

-H-

5°/15°

5°/15°

.041 REF

.016/.035

0° MIN

R.003 MIN

R.003/.013

0°-8°

.010

GAGE PLANE

SEE DETAIL B

REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVI
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	T. VU
	03	CHANGE TO QSOP	12/15/99	S.SUE
	04	ADD "GREEN" PCG NOMENCLATURE	10/08/04	TU VU
	05	CHANGE RADIUS DIM	11/15/11	CK LEE

TOLERANCES UNLESS SPECIFIED

DECIMAL
XX±
XXX±
XXXX±

ANGULAR ±

APPROVALS | DATE
DRAWN
CHECKED

www.IDT.com

2975 Stender Way
Santa Clara, CA 950
PHONE: (408) 727-61
FAX: (408) 492-8674

TITLE
PC/PCG PACKAGE OUTLINE
.150" BODY WIDTH QSOP
.025" PITCH

SIZE C

DRAWING No.
PSC-4040

DO NOT SCALE DRAWING

SHEET 1 OF

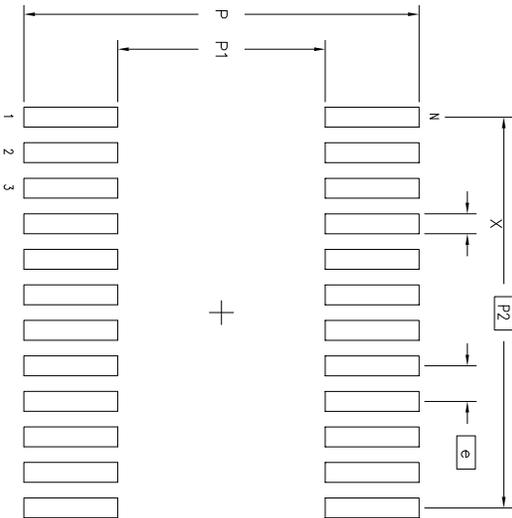# Package Outline and Package Dimensions, cont. **(20-pin QSOP)**

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2. DATUMS ⎿-A-⏌ AND ⎿-B-⏌ TO BE DETERMINED AT DATUM PLANE ⎿-H-⏌

3. DIMENSION E TO BE DETERMINED AT SEATING PLANE ⎿-C-⏌

4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE ⎿-H-⏌

5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS, INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE

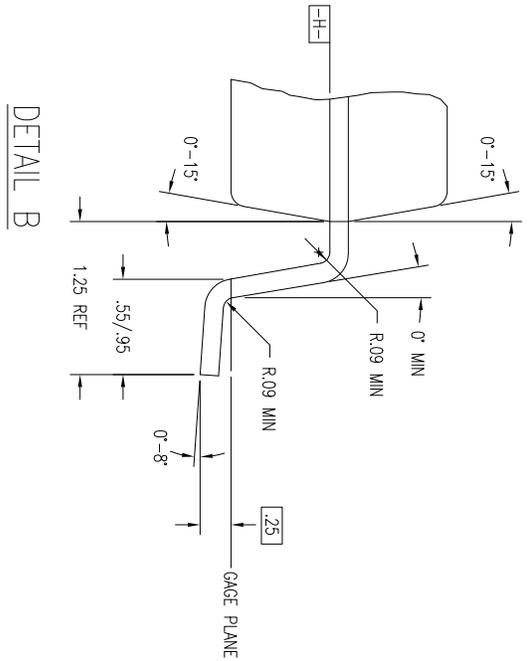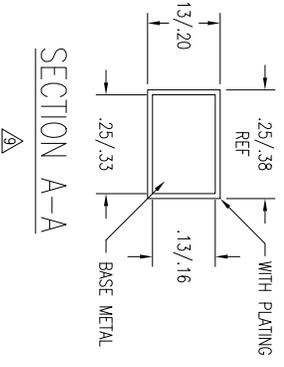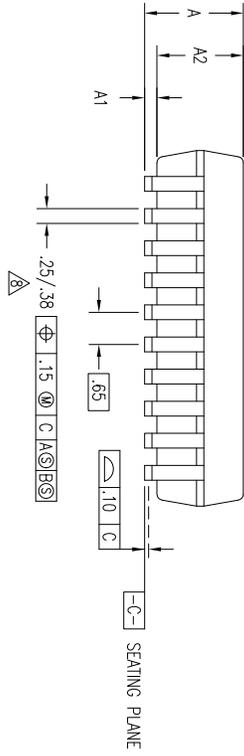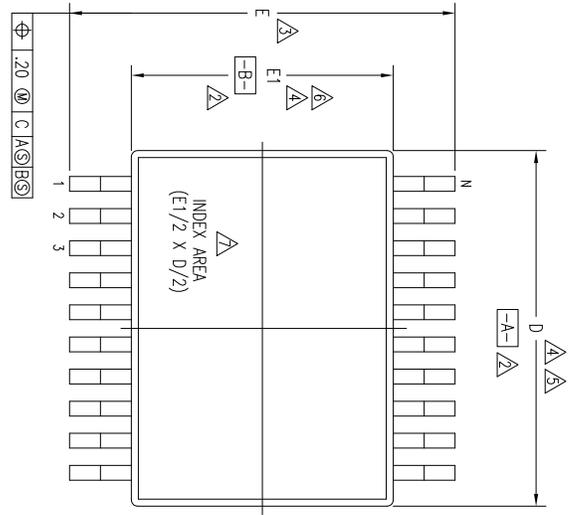7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9. THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10. ALL DIMENSIONS ARE IN INCHES

11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

JEDEC VARIATION AD							
	MIN	NOM	MAX	N	D	E	
D	.061	.064	.068				
	.004	.006	.010				
	.055	.058	.061	11			
	.337	.342	.344	4,5			
	.230	.236	.244	3			
	.150	.155	.157	4,6			
	20						

LAND PATTERN DIMENSIONS

	MIN	MAX
	.274	.282
	.142	.150
	.225 BSC	
	.010	.018
	.025 BSC	
	20	

P
P1
1 2 3
N
X
P2
e

Package Outline and Package Dimensions (20-pin SSOP)

SECTION A-A

.13/.20

.25/.38 REF

.25/.33

.13/.16

WITH PLATING

BASE METAL

A
A2
A1
.25/.38
.65
⊕ .15 Ⓜ C A Ⓢ B Ⓢ
⬠ .10 C
-C-
SEATING PLANE

E
⊕ .20 Ⓜ C A Ⓢ B Ⓢ
-B-
E1
1 2 3
N
INDEX AREA
(E1/2 X D/2)
-A-
D

DETAIL B

-H-
0°-15°
0°-15°
1.25 REF
.55/.95
R.09 MIN
0° MIN
0°-8°
R.09 MIN
.25
GAGE PLANE

SEE DETAIL B

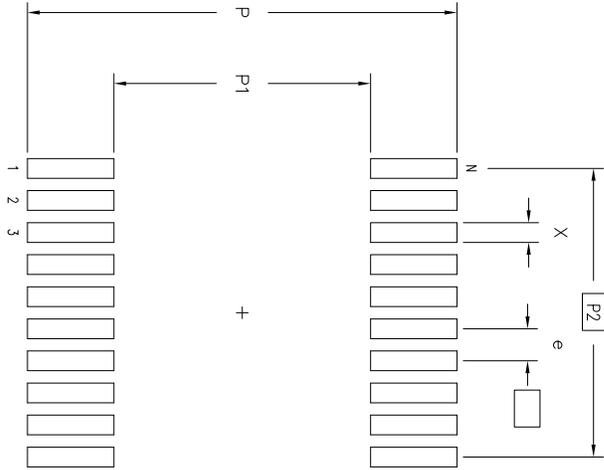|				
06	ADDED PACKAGE CODE	12/12/12	RC	
05	ADD "GREEN" PYG NOMENCLATURE	10/12/04	TU VU	
04	ADDED TOPMARK TO TITLE	5/23/01	T. VU	
03	ADD 14 & 16 LD	08/25/98	T. VU	
02	REDRAW TO JEDEC FORMAT	03/15/95	T. VU	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .20 mm PER SIDE

6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .20 mm PER SIDE

7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .13 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10. ALL DIMENSIONS ARE IN MILLIMETERS

11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-150, VARIATION AB, AC, AE, AG & AH

PY/PYG20				
JEDEC VARIATION AE			N D	E
	MIN	NOM	MAX	
	1.73	1.86	1.99	
	.05	.13	.21	
	1.68	1.73	1.78	
	7.07	7.20	7.33	4,5
	7.65	7.80	7.90	3
	5.20	5.30	5.38	4,6
			20	20

02	REDRAW TO JEDEC FORMAT	03/15
03	ADD 14 & 16 LD	08/25
04	ADDED TOPMARK TO TITLE	5/23
05	ADD "GREEN" PYG NOMENCLATURE	10/12
06	ADDED PACKAGE CODE	12/12

TOLERANCES UNLESS SPECIFIED
DECIMAL   ANGULAR
XX±   ±
XXX±
XXXX±

APPROVALS	DATE
DRAWN	
CHECKED	

www.IDT.com

6024 SILV...
SAN...
PHON...
FAX:

TITLE PY/PYG PACKAGE OUTLINE (PY OR PV TOPMARK CO... 5.3 mm BODY WIDTH SS...

SIZE C   DRAWING No. PSC-40...

![Renesas]

Package Outline and Package Dimensions, cont. (20-pin SSOP)

LAND PATTERN DIMENSIONS

MIN	MAX
8.60	8.80
5.10	5.30
5.85 BSC	
.30	.40
.65 BSC	
20	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
74FCT3807SNDGI	see page 6	Tubes	20-pin VFQFPN	-40° to +105°C
74FCT3807SNDGI8		Tape and Reel	20-pin VFQFPN	-40° to +105°C
74FCT3807SPGGI		Tubes	20-pin TSSOP	-40° to +105°C
74FCT3807SPGGI8		Tape and Reel	20-pin TSSOP	-40° to +105°C
74FCT3807SQGI		Tubes	20-pin QSOP	-40° to +105°C
74FCT3807SQGI8		Tape and Reel	20-pin QSOP	-40° to +105°C
74FCT3807SPYGI		Tubes	20-pin SSOP	-40° to +105°C
74FCT3807SPYGI8		Tape and Reel	20-pin SSOP	-40° to +105°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/18/15	B. Chandhoke	Initial release.

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