# MOSFET

OptiMOS^{TM} Power-MOSFET, 40 V

Features

- Optimized for high performance SMPS, e.g. sync. rec.
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability with enlarged source interconnection

TSDSON-8 FL
(enlarged source interconnection)
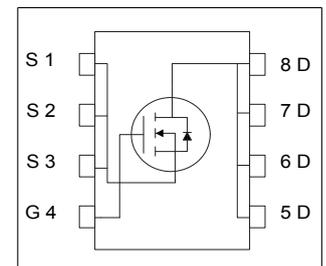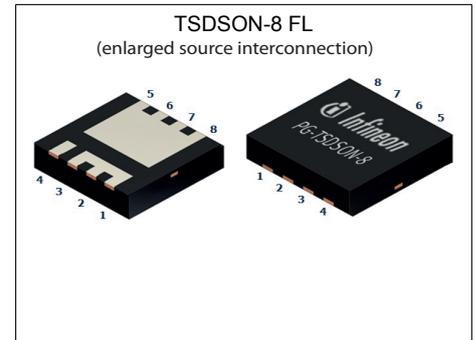
Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	3.4	mΩ
I_D	40	A
Q_{OSS}	22	nC
Q_G(0V..10V)	25	nC

Type / Ordering Code	Package	Marking	Related Links
BSZ034N04LS	PG-TSDSON-8 FL	034N04L	-

[1] J-STD20 and JESD22

Final Data Sheet

Rev. 2.1, 2016-06-09

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - - -	- - - - -	40 40 40 40 19	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=60 K/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	160	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	70	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	52 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 K/W[1]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.4	2.4	K/W	-
Device on PCB, 6 cm^2 cooling area[1]	R_{thJA}	-	-	60	K/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.7 3.4	3.4 4.6	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=4.5 V, I_D=20 A
Gate resistance[1]	R_G	-	0.8	1.6	Ω	-
Transconductance	g_{fs}	46	93	-	S	$\|V_{DS}\|$>2$\|I_D\|R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	1800	2520	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	500	700	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	40	80	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$,ext=1.6 Ω
Rise time	t_r	-	4	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$,ext=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$,ext=1.6 Ω
Fall time	t_f	-	3	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$,ext=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4.3	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	2.8	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	4.0	5.6	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	5.5	-	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	25	35	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	13	18	nC	V_{DD}=20 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	10	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[1]	Q_{oss}	-	22	31	nC	V_{DD}=20 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test
[2] See ″Gate charge waveforms″ for parameter definition

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	40	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	160	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.82	1	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	23	46	ns	V_R=20 V, I_F=20A, di_F/dt=400 A/µs
Reverse recovery charge	Q_{rr}	-	52	-	nC	V_R=20 V, I_F=20A, di_F/dt=400 A/µs

[1] Defined by design. Not subject to production test

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4 Electrical characteristics diagrams

Diagram 1: Power dissipation

$P_{tot}=f(T_C)$

Diagram 2: Drain current

$I_D=f(T_C)$; $V_{GS}\geq10$ V

Diagram 3: Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$
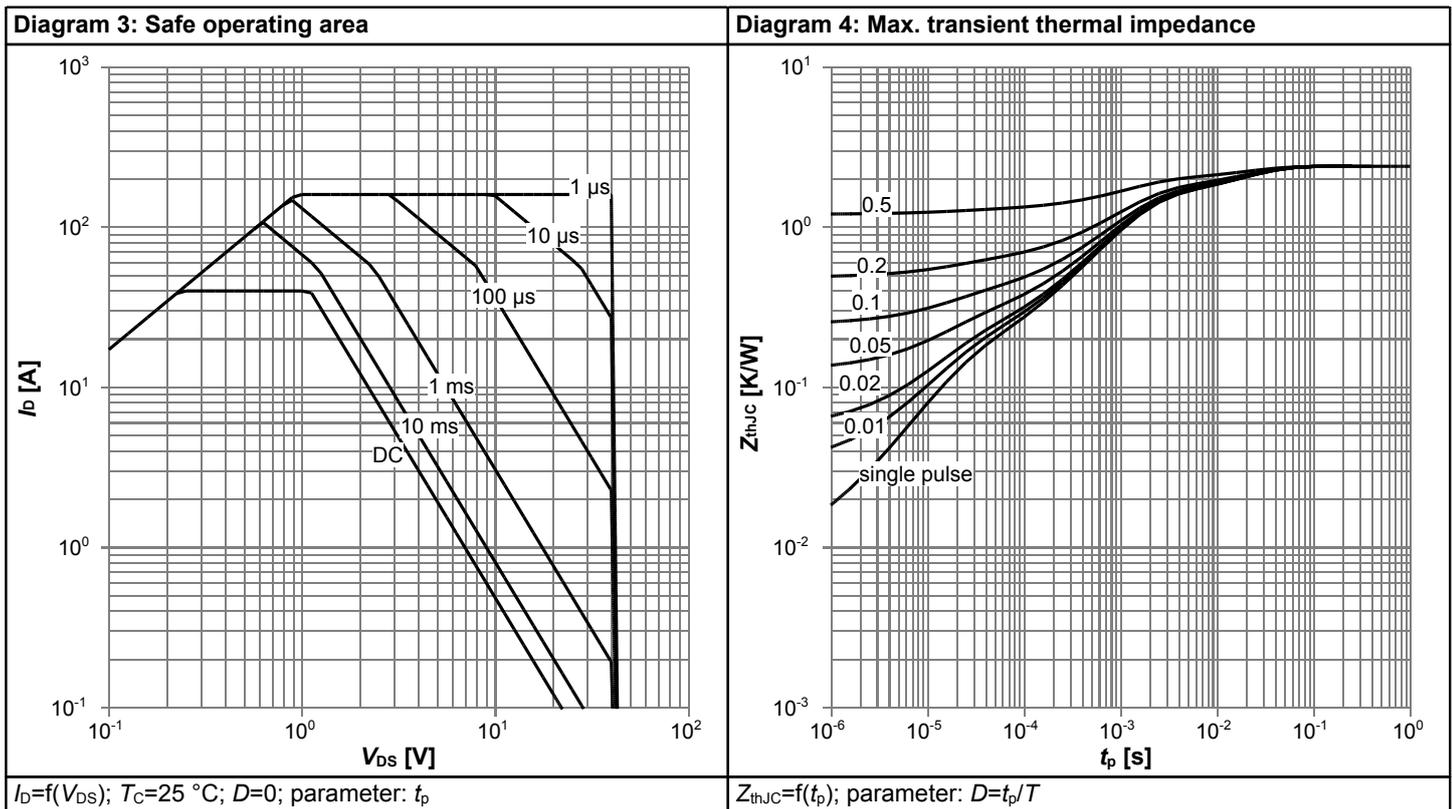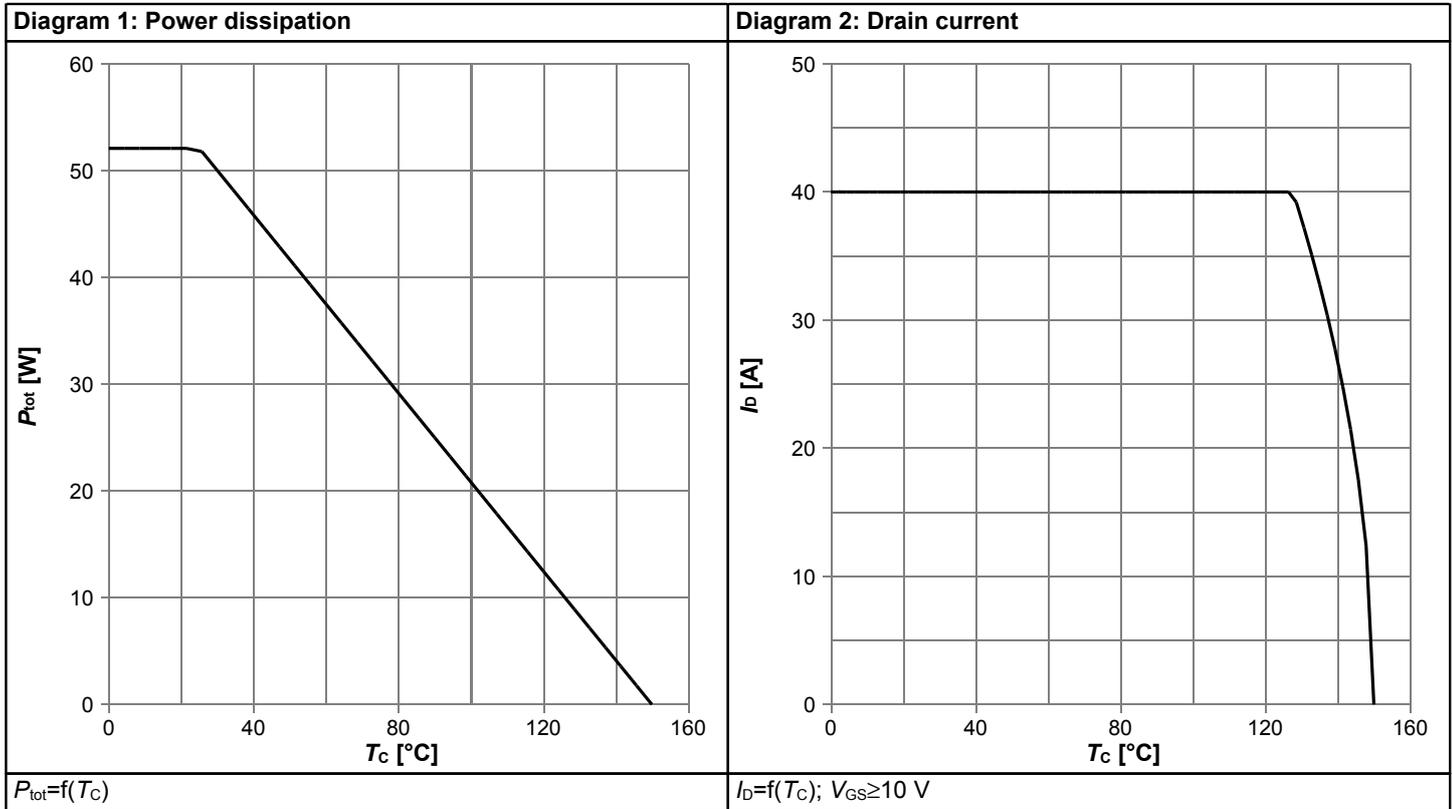
Diagram 5: Typ. output characteristics
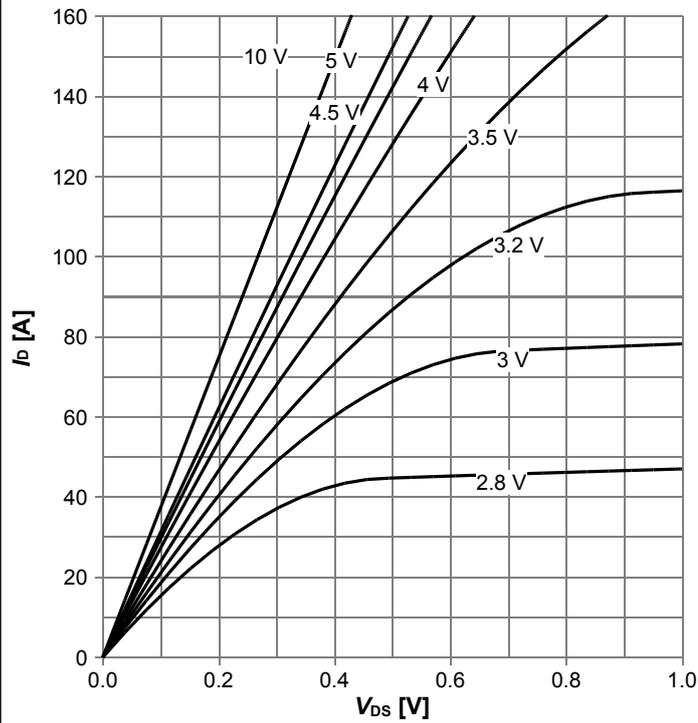
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance
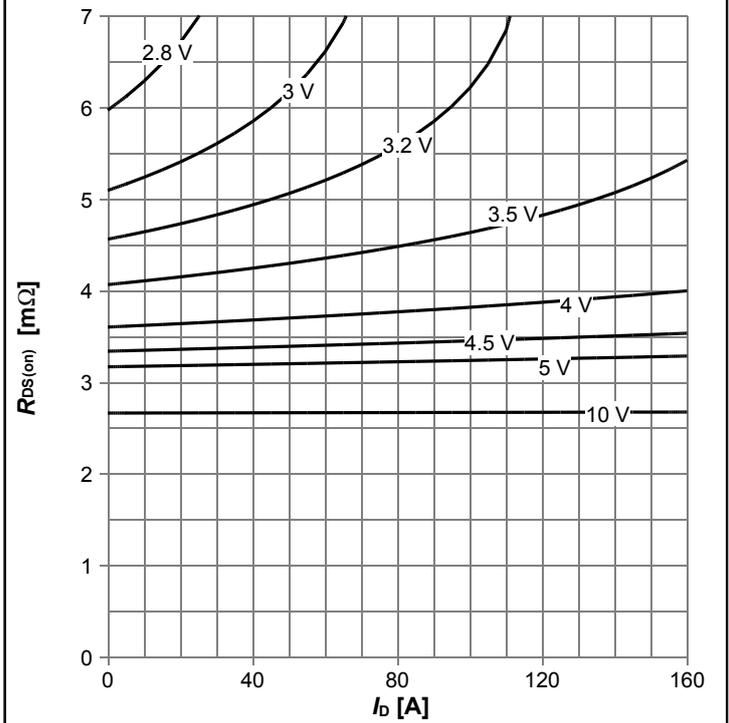
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics
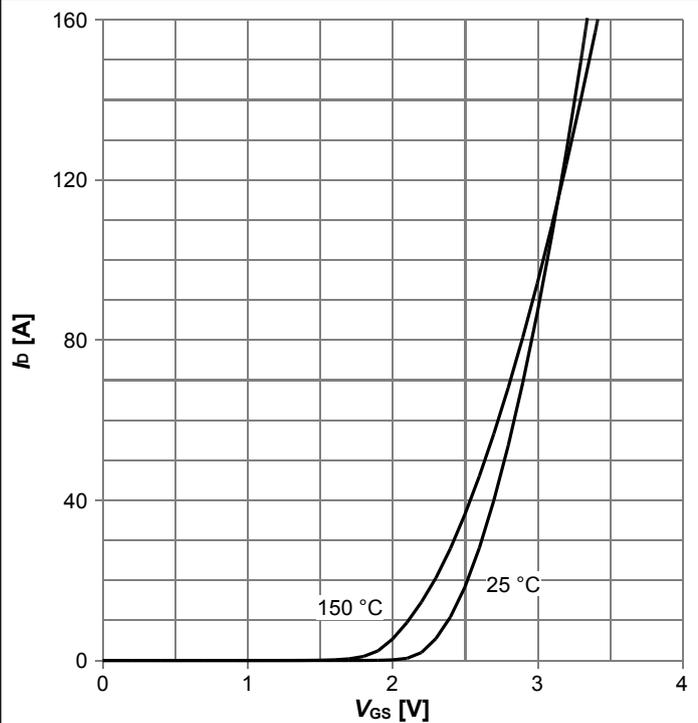
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance
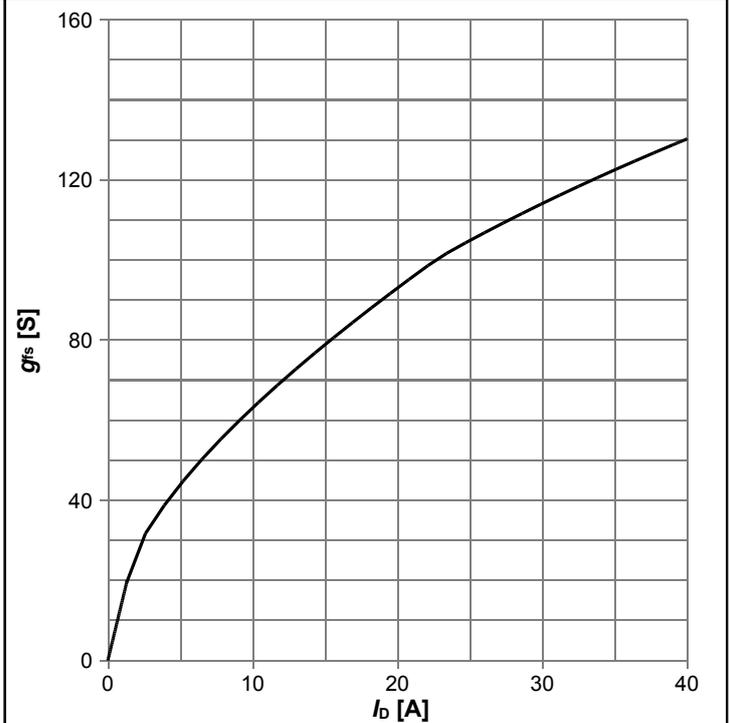
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance
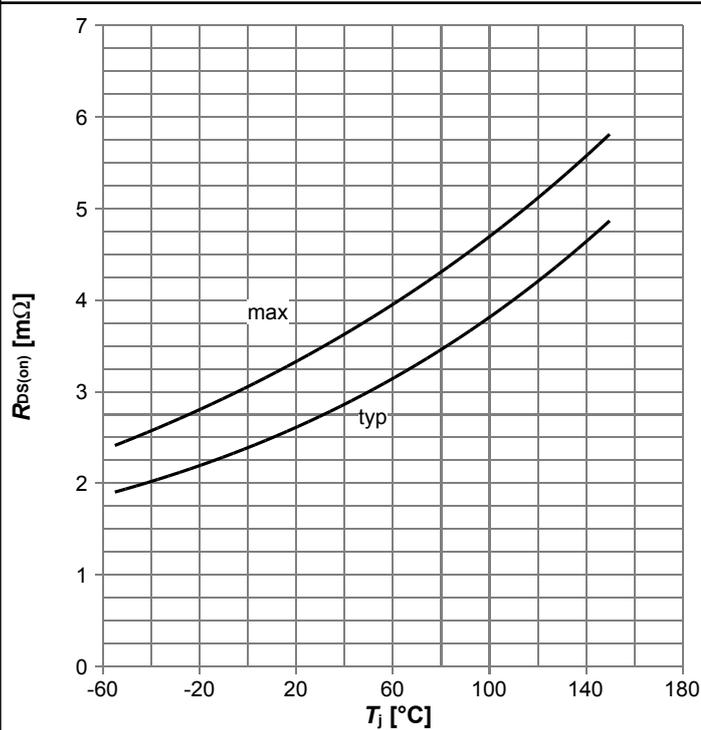
$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage
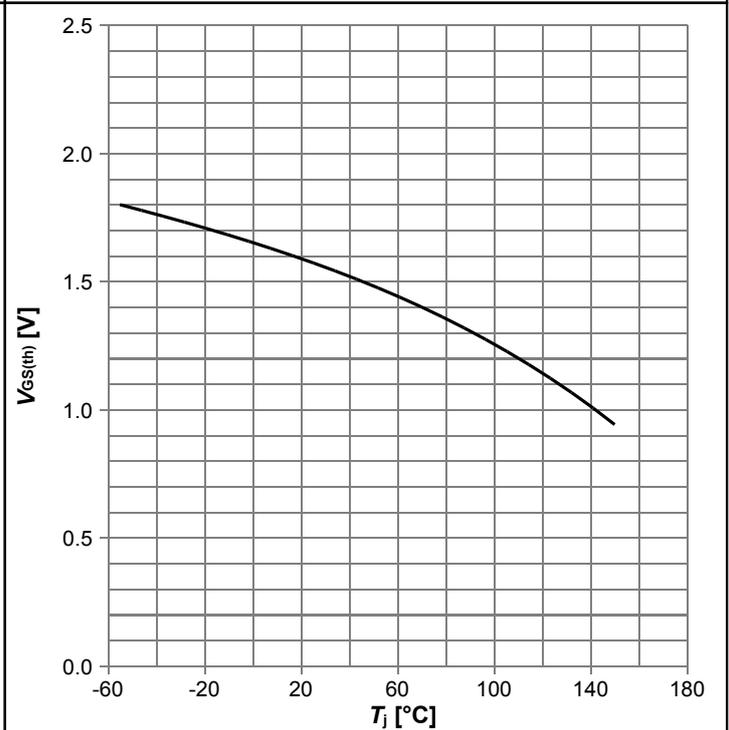
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances
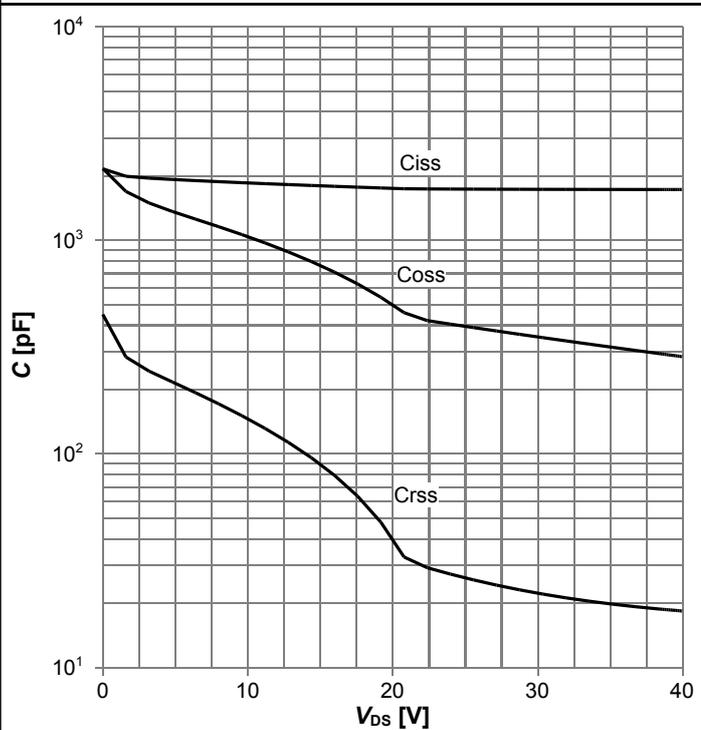
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode
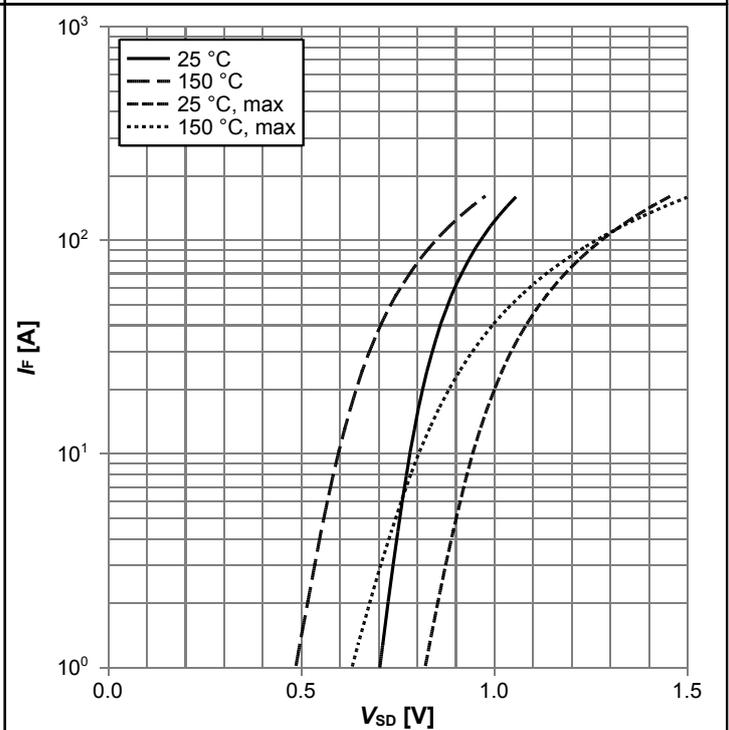
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics
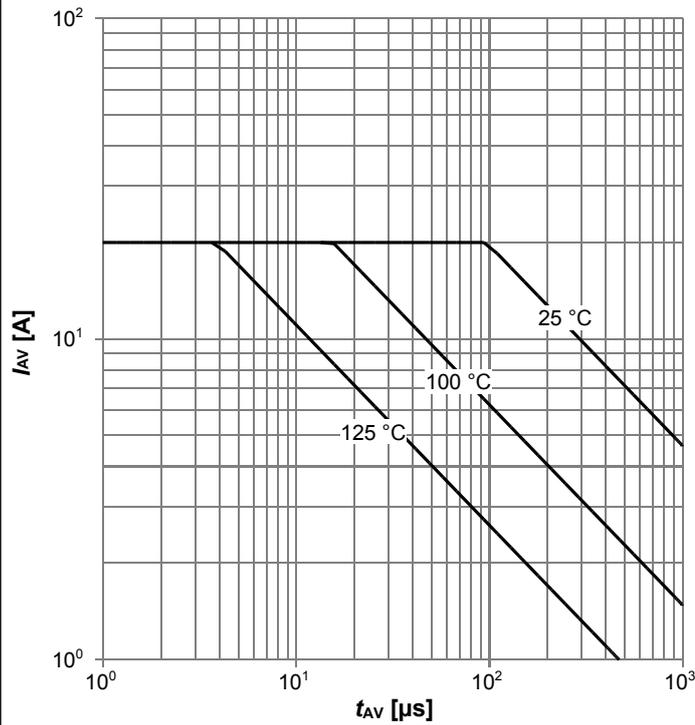
$I_{AS}=f(t_{AV})$; $R_{GS}=25\,\Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge
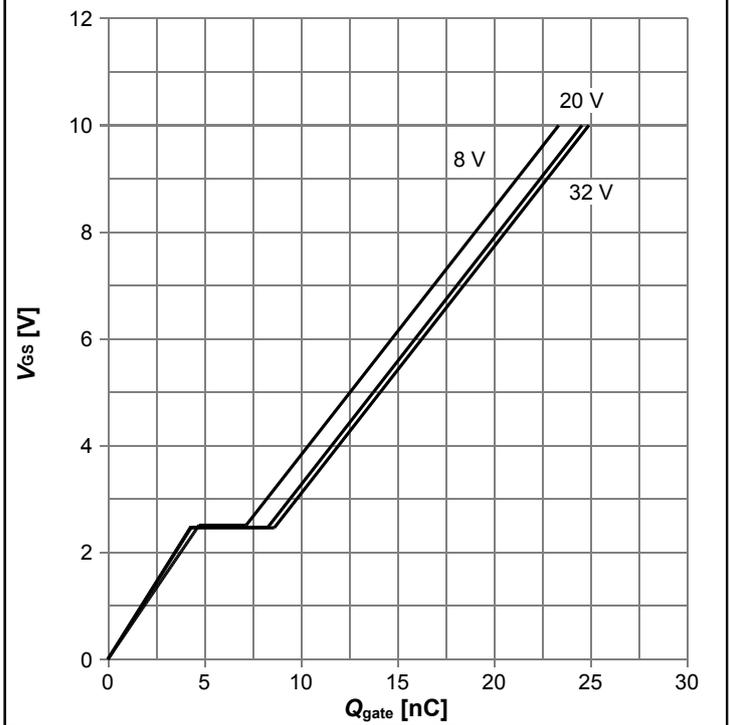
$V_{GS}=f(Q_{gate})$; $I_D=20$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage
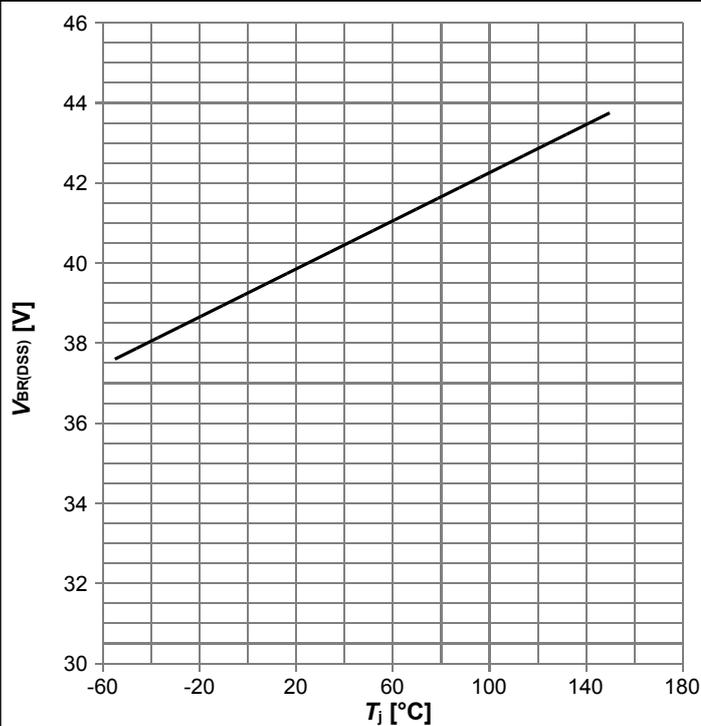
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Gate charge waveforms
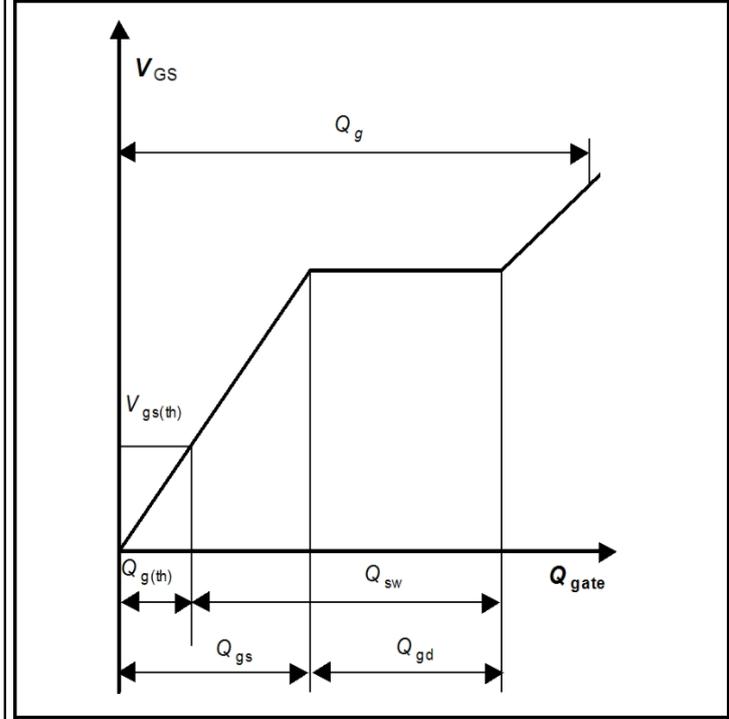
5   Package Outlines
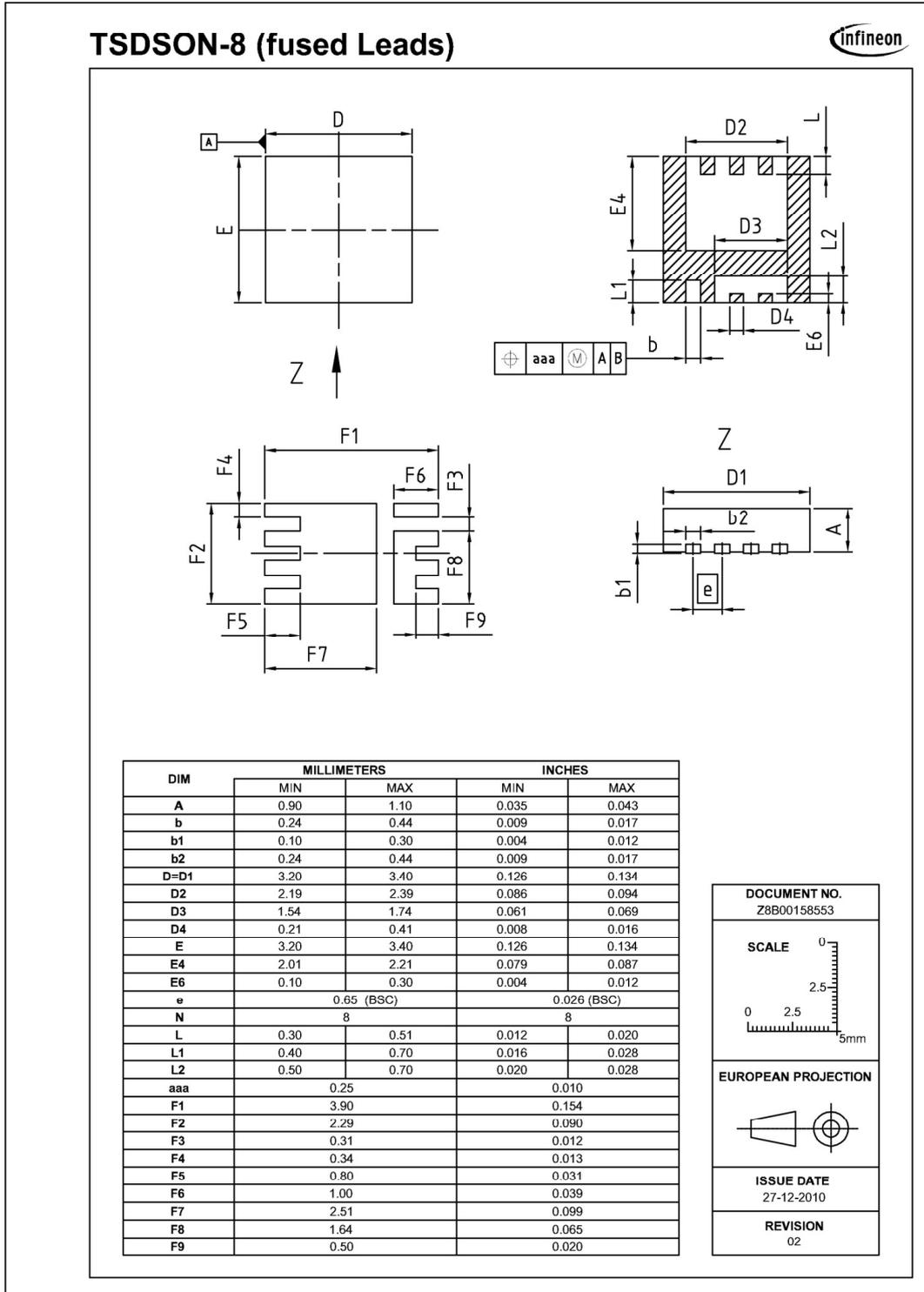
Figure 1   Outline PG-TSDSON-8 FL, dimensions in mm/inches

Revision History

BSZ034N04LS

Revision: 2016-06-09, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2016-06-09	Insert max values and update footnotes

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