*Click **here** to ask an associate for production status of specific part numbers.*

MAX96724/F/R

Quad Tunneling GMSL2/1 to CSI-2 Deserializer

General Description

The MAX96724/F/R deserializer converts four GMSL™2/1 inputs to 1, 2, or 4 MIPI D-PHY or C-PHY outputs. The device allows simultaneous transmit bidirectional transmissions over 50Ω coax or 100Ω STP cables that meet the GMSL channel specification. Contact the factory for the GMSL supporting collateral.

Up to four remotely located sensors can be supported using industry-standard coax or STP interconnects. Each GMSL2 serial link operates at a fixed rate of 3Gbps or 6Gbps in the forward direction and 187.5Mbps in the reverse direction. The MAX96724/F/R supports both aggregation and replication of video data, enabling streams from multiple remotely located sensors to be combined and routed to one or more of the available CSI-2 outputs.

Table 1. Typical Maximum Cable Length

	3.2mm Ø 50Ω Coax, Foam Dielectric	**2.7mm Ø 50Ω Coax, Solid Dielectric**	**100Ω Shielded Twisted Pair, AWG26**
Attenuation at 3GHz (Typ, Room Temp)	0.9dB/m	1.6dB/m	1.8dB/m
Attenuation at 3GHz (Max, Aged, +105°C)	1.1dB/m	2.0dB/m	2.2dB/m
GMSL Fwd/Rev Data Rate	**Typical Maximum Cable Length at +105°C (m)**		
3Gbps/187.5Mbps	20	10	11
6Gbps/187.5Mbps	15	9	8

Applications

- High-Resolution Camera Systems
- Advanced Driver Assistance Systems (ADAS)

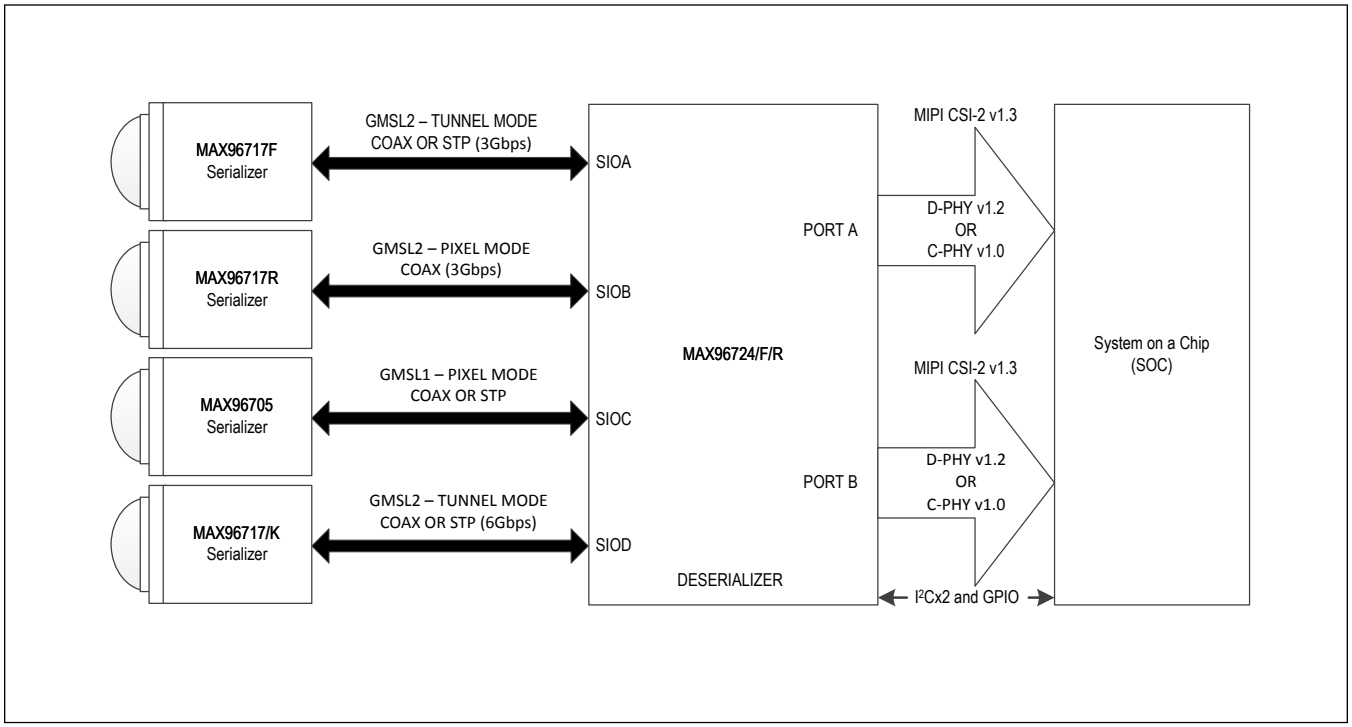
Benefits and Features

- Automotive Grade High Speed Link
  - -21.0dB at 3.0GHz (6Gbps) Max Insertion Loss
  - -19.5dB at 1.5GHz (3Gbps) Max Insertion Loss
  - Auto Adapt for Changes in Channel Conditions
  - Operates at -40°C to +105°C Ambient
- Quad Independently Configurable GMSL Inputs
  - 6/3Gbps GMSL2 and 3.12Gbps GMSL1 Link-Rates
  - 187.5Mbps/1Mbps (GMSL2/1) Reverse Link-Rates
  - Support for Mixed GMSL2/1 Pixel and Tunnel Inputs
- 2x4 or 4x2 Lane MIPI CSI-2 v1.3 Outputs
  - MIPI D-PHY v1.2 Rated at 2.5Gbps/Lane
  - C-PHY v1.0 Rated at 5.7Gbps/Lane
  - Aggregation and Replication Functions
  - 16/32 Virtual channel support for D-PHY/C-PHY
- Auto D-PHY (Imager) to C-PHY (SoC) Conversion
- Reference over Reverse (RoR) Clocking
- Bidirectional Reverse Channel Supports
  - 9 x Configurable GPIOs
  - 2 x I^2C Ports, up to 1Mbps
- ASIL-B Compliant (MAX96724/F)
- Ease of Use Features
- Reduce BOM and Space Savings
  - Small 8x8mm TQFN Standard and Side-Wettable
  - Industry's Smallest Power-over-Coax (PoC)

Ordering Information appears at end of datasheet.

19-101575; Rev 4; 1/23

Simplified Block Diagram



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Absolute Maximum Ratings

(All voltages with respect to ground.) .....
V_{DDIO} ..... -0.3V to +3.9V
V_{DD18} ..... -0.3V to +2.0V
V_{DD} ..... -0.3V to +2.0V
V_{TERM} ..... -0.3V to +1.32V
CAP_VDD ..... -0.3V to +1.2V
SIO_ (Active State) (*Note a*)..... (V_{DD18} - 1.1V) to V_{DD18}
SIO_ (Inactive State) (*Note a*) ..... -0.3V to +1.1V
DA/B_P/N, CKA/B/C/FP/N (*Note b*) ..... -0.3V to (V_{TERM} + 0.1V)
DA_P/N, CKA/CP/N (*Note b*) ..... -0.3V to (V_{TERM} + 0.1V)
XRES, X2 ..... -0.3V to (V_{DD18} + 0.3V)
All Other Pins (*Note c*) ..... -0.3V to (V_{DDIO} + 0.3V)
Continuous Power Dissipation, Multilayer Board (*Note d*) 2619mW
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note a: Active state means the device is powered-up and not power-down mode. Inactive means the device is not in power-down mode.

Note b: Specified maximum voltage or 1.36V, whichever is lower

Note c: Specified maximum voltage or 3.9V, whichever is lower.

Note d: Derate 47.6mW/°C above T_A = +70°C. Maximum dissipation is determined using specified θ_{JA} and assuming maximum acceptable die temperature of +125°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

56-pin TQFN-SW

Package Code	T5688Y+6C
Outline Number	**21-100046**
Land Pattern Number	**90-100048**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25
Junction to Case (θ_{JC})	4

56-pin TQFN

Package Code	T5688+6C
Outline Number	**21-0135**
Land Pattern Number	**90-100041**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25
Junction to Case (θ_{JC})	4

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL SERIAL OUTPUTS — (Figure 3)							
Output Voltage Swing (Single-ended)	V_O	R_L = 100Ω ±1%		190	250	310	mV
Output Voltage Swing (Differential)	V_{ODT}	R_L = 100Ω ±1% peak-to-peak differential voltage		380	500	620	mV
Change in V_{OD} between Complementary Output States	ΔV_{OD}	R_L = 100Ω ±1%, $\lvert V_{OD(H)} - V_{OD(L)} \rvert$				25	mV
Differential Output Offset Voltage	V_{OS}	R_L = 100Ω ±1% offset voltage in each output state		V_{DD18} - 0.45	V_{DD18} - 0.3	V_{DD18} - 0.15	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}	R_L = 100Ω ±1% $\lvert V_{OS(H)} - V_{OS(L)} \rvert$				25	mV
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / GMSL1 REVERSE CHANNEL SERIAL OUTPUTS — (Figure 4)							
Differential High Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODH}	Forward channel disabled STP mode R_L=100Ω	HIM disabled	30		70	mV
			HIM enabled	50		110	
Differential Low Output Peak Voltage $V_{(SIO\_P)}$ - $V_{(SIO\_N)}$	V_{RODL}	Forward channel disabled STP mode R_L=100Ω	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled coax mode R_L=100Ω	HIM disabled	30		70	mV
			HIM enabled	50		110	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled coax mode R_L=100Ω	HIM disabled	-70		-30	mV
			HIM enabled	-110		-50	
Differential Output Offset Voltage ($V_{(SIO\_P)}$ + $V_{(SIO\_N)}$)/2	V_{OS}	STP mode		V_{DD18} - 0.3		V_{DD18}	V
Termination Resistance (Internal)	R_T	Any Pin to V_{DD18}		50	55	60	Ω
DC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER							
Thevenin High-Level Output Voltage	V_{OH}			0.95	1.2	1.3	V
Thevenin Low-Level Output Voltage	V_{OL}			-50		50	mV
Output Impedance	Z_{OLP}			110			Ω

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER						
HS Transmit Static Common-Mode Voltage	V_{CMTX}		150	200	250	mV
V_{CMTX} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{CMTX(1,0)}\rvert$	$\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)}) / 2$			5	mV
HS Transmit Differential Voltage	$\lvert V_{OD}\rvert$		140	200	270	mV
V_{OD} Mismatch when Output is Differential-1 or Differential-0	$\lvert\Delta V_{OD}\rvert$				14	mV
HS Output High Voltage	V_{OHHS}				360	mV
Single-Ended Output Impedance	Z_{OS}		40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				10	%
DC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER						
HS Transmit Static Common-Point Voltage	V_{CPTX}	Z_{ID} = 100Ω	175		310	mV
V_{CPTX} Mismatch when Output is in any of the Six High-Speed States	$\lvert\Delta V_{CPTX(HS)}\rvert$	(Figure 5)			9	mV
HS Transmit Differential Voltage of the Differential Strong 1 and Strong 0	$\lvert V_{OD}\rvert$ strong	Z_{ID} = 100Ω (Figure 6)			300	mV
HS Transmit Differential Voltage of the Differential Weak 1 and Weak 0	$\lvert V_{OD}\rvert$ weak	Z_{ID} = 100Ω (Figure 6)	97			mV
V_{OD} Mismatch Between the Absolute Values of the Differential Strong 1 and Strong 0 Output Voltages in any of the Six Possible High-Speed States	$\lvert\Delta V_{OD}\rvert$	(Figure 5)			17	mV
HS Output High Voltage	V_{OHHS}	Z_{ID} =100Ω			425	mV
Single-Ended Output Impedance	Z_{OS}		40	50	60	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}				10	%
DC ELECTRICAL CHARACTERISTICS / I/O PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup/Pulldown Resistance	R_{IN}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / OPEN-DRAIN PINS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input Current	I_{IN}	All pullup/pulldown devices disabled. V_{IN} = 0V to V_{DDIO}			1	µA
Input Capacitance	C_{IN}			3		pF
Internal Pullup Resistance	R_{PU}	40kΩ enabled		40		kΩ
		1MΩ enabled		1		MΩ
DC ELECTRICAL CHARACTERISTICS / PWDNB INPUT						
High-Level Input Voltage	V_{IH}		0.7 x V_{DDIO}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DDIO}	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DDIO}			6	µA
Internal Pulldown Resistance	R_{PD}			1		MΩ
Input Capacitance	C_{IN}			3		pF
DC ELECTRICAL CHARACTERISTICS / PUSH-PULL OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA	V_{DDIO} - 0.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
DC ELECTRICAL CHARACTERISTICS / LINE FAULT DETECTION INPUTS						
Open Pin Voltage	V_{O0}	LMN0, LMN2		1.25		V
	V_{O1}	LMN1, LMN3		0.75		
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (CRYSTAL) (X1/OSC, X2)						
X1 Input Capacitance	C_{IN_X1}			3		pF

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
X2 Input Capacitance	C_{IN_X2}				1		pF
Internal X2 Limit Resistor	R_{LIM}				1.2		kΩ
Internal Feedback Resistor	R_{FB}				10		kΩ
Transconductance	g_m				28		mA/V
DC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK INPUT (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED)							
High-Level Input Voltage	V_{IH}			0.9			V
Low-Level Input Voltage	V_{IL}					0.4	V
Input Impedance	R_{IN}				10		kΩ
X1 Input Capacitance	C_{IN_X1}				3		pF
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT — GMSL2 MODE							
Supply Current	I_{DD1}	4x 3Gbps input, 4x 2.45Gbps payload input, PRBS24, 1x 4-lane D-PHY, 2500Mbps/lane	V_{TERM} = 1.26V		17	25	mA
			V_{DD18} = 1.9V		280	325	
			V_{DD} = 1.05V		197	625	
			V_{DD} = 1.26V		191	600	
		4x 6Gbps input, 4x 5.2Gbps payload input, PRBS24, 1x 4-lane C-PHY, 5700Mbps/lane (MAX96724)	V_{TERM} = 1.26V		19	35	
			V_{DD18} = 1.9V		280	325	
			V_{DD} = 1.05V		244	675	
			V_{DD} = 1.26V		228	650	
	I_{DD2}	Replicate Mode, 4x 3Gbps input, 4x 2.45Gbps payload input, PRBS24, 2x 4-lane D-PHY, 2500Mbps/lane	V_{TERM} = 1.26V		34	50	
			V_{DD18} = 1.9V		280	325	
			V_{DD} = 1.05V		224	675	
			V_{DD} = 1.26V		218	650	
		Replicate Mode, 4x 6Gbps input, 4x 5.2Gbps payload input, PRBS24, 2x 4-lane C-PHY, 5700Mbps/lane (MAX96724)	V_{TERM} = 1.26V		37	70	
			V_{DD18} = 1.9V		280	325	
			V_{DD} = 1.05V		272	725	
			V_{DD} = 1.26V		265	700	
V_{DDIO} Supply Current (*Note 3*)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V		44		µA/MHz
			V_{DDIO} = 3.3V		81		

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY CURRENT — GMSL1 MODE							
Supply Current	I_{DD1}	4x 3.12Gbps input, 4x 2.45Gbps payload input, PRBS24, 1x 4-lane D-PHY, 2500Mbps/lane	V_{TERM} = 1.2V		16	25	mA
			V_{DD18} = 1.8V		155	200	
			V_{DD} = 1.05V		113	550	
			V_{DD} = 1.26V		107	525	
	I_{DD2}	Replicate Mode, 4x 3.12Gbps input, 4x 2.45Gbps payload input, PRBS24, 2x 4-lane D-PHY, 2500Mbps/lane	V_{TERM} = 1.2V		29	50	
			V_{DD18} = 1.8V		155	200	
			V_{DD} = 1.05V		138	575	
			V_{DD} = 1.26V		132	550	
V_{DDIO} Supply Current (*Note 3*)	I_{DDIO}	Per toggling GPIO, C_L = 20pF	V_{DDIO} = 1.8V		44		µA/MHz
			V_{DDIO} = 3.3V		81		
DC ELECTRICAL CHARACTERISTICS / POWER-DOWN CURRENT							
Power-Down Current	I_{DD}	V_{TERM} = 1.26V	T_A = +25°C		< 1		µA
			T_A = +105°C		< 1		
		V_{DD18} = 1.9V	T_A = +25°C		< 1		
			T_A = +105°C		14		
		V_{DD} = 1.26V	T_A = +25°C		< 1		
			T_A = +105°C		< 1		
		V_{DDIO} = 3.6V	T_A = +25°C		7		
			T_A = +105°C		7		
AC ELECTRICAL CHARACTERISTICS / GMSL2 FORWARD CHANNEL							
Lock Time	t_{LOCK2}	From power-up, one-shot reset, or rising edge of PWDNB to rising edge of LOCK. (*Note 9*, *Note 10*) (Figure 22)			45	60	ms
Maximum Video Initialization Time	$t_{VIDEOSTART}$	Time from GMSL2 video packets at SIO_ to valid packets at the CSI-2 output (assumes link locked and registers configured).			0.1ms + (6600 x t_{PCLK})		ms
Maximum Video Latency	t_{VL}	Time from the first pixel in SIO_ to CSI-2 output. (Figure 7)			1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	Minimum time to reset the device.			1		µs
AC ELECTRICAL CHARACTERISTICS / GMSL2 REVERSE CHANNEL							
GMSL Reverse Channel Transmitter Rise/Fall Time	t_R, t_F	20% to 80%, V_O = 250mV, R_L = 100Ω			2300		ps

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Serial Output p-p Jitter	t_{TSOJ}	PRBS7, single-ended or differential output		0.15		UI
Deterministic Serial Output p-p Jitter	t_{DSOJ}	PRBS7, single-ended or differential output		0.1		UI
GPI-GPO Delay Reverse Path	t_{GPDR}	Delay-Compensated Mode (Figure 8)		15		µs
		Non-Delay-Compensated Mode (Figure 8)		6		
GPI-GPO Skew Reverse Path	t_{SKEW}	Delay-compensated Mode (Figure 8)		7		ns
AC ELECTRICAL CHARACTERISTICS / GMSL1						
Lock Time	t_{LOCK1}	(Figure 9)		4		ms
Power-up Time	t_{PU}	(Figure 10)		8.5		ms
Video Latency	t_{VL}	Time from the first pixel in a video line at SIO_ to the first pixel in the CSI-2 output packet. (Figure 11)		1 video line + (128 x t_{PCLK})		s
PWDNB Hold Time	t_{HOLD_PWDNB}	The minimum duration PWDNB must be held LOW to reset the device		1		µs
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission (Figure 4) (*Note 2*)	100		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission (Figure 4) (*Note 2*)	100		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included) (Figure 12) (*Note 2*)			350	µs
AC ELECTRICAL CHARACTERISTICS / C-PHY and D-PHY LP TRANSMITTER (*Note 2*)						
15%-85% Rise Time and Fall Time	T_{RLP}/T_{FLP}	(*Note 4*)			25	ns
30%-85% Rise Time	T_{REOT}	(*Note 5*)			35	ns
Load Capacitance	C_{LOAD}	(*Note 4*)	0		70	pF
AC ELECTRICAL CHARACTERISTICS / D-PHY HS TRANSMITTER (*Note 2*)						
Common-Level Variations, HF	$\Delta V_{CMTX(HF)}$	> 450MHz			15	mV_{RMS}
Common-Level Variations, LF	$\Delta V_{CMTX(LF)}$	50 to 450MHz			25	mV_{PEAK}
20%-80% Rise Time and Fall Time	t_R and t_F				0.4	UI
			50			ps
Differential-Mode Reflection Coefficient (*Note 6*)	Sdd_{TX}	f_{hMAX} = 1.25GHz		-4.5		dB
		f_{MAX} = 1.875GHz		-2.5		

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Reflection Coefficient (*Note 6*)	Scc_{TX}	f_{MAX} = 1.875GHz		-2.5		dB
Data Lane Bit Rate	DL_{BR}		80		2500	Mbps
Clock Lane Frequency	CL_{FREQ}		40		1250	MHz
CSI-2 Output Inter-packet Spacing	t_{SPACE}			300ns + 370UI		ns
AC ELECTRICAL CHARACTERISTICS / D-PHY DATA-CLOCK TIMING (*Note 2*)						
UI Instantaneous	UI_{INST}		0.4		12.5	ns
UI Variation	ΔUI	UI ≥ 1ns within a single burst	-10%		10%	UI
		0.667ns ≤ UI ≤ 1ns within a single burst	-5%		5%	
Data to Clock Skew	T_{SKEW}	0.08 to 1.0Gbps	-0.15		0.15	UI_{INST}
		> 1.0 to 1.5Gbps	-0.2		0.2	
Static Data to Clock Skew	T_{SKEW} Static	> 1.5Gbps	-0.2		0.2	UI_{INST}
Dynamic Data to Clock Skew	T_{SKEW} Dynamic	> 1.5Gbps	-0.15		0.15	UI_{INST}
AC ELECTRICAL CHARACTERISTICS / D-PHY GLOBAL OPERATION TIMING (*Note 2*)						
Transition from LP to HS Mode	$T_{CLK-PRE}$		8			UI
State Before the HS-0 Line State Starting the HS Transmission	$T_{CLK-PREPARE}$		38		95	ns
$T_{CLK-PREPARE}$ + Time Prior to Starting the Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$		300			ns
$T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to LP-11	T_{EOT}				105 + 12xUI	ns
LP-11 Following a HS Burst	$T_{HS-EXIT}$		100			ns
Data Lane LP-00 Before HS-0	$T_{HS-PREPARE}$		40 + 4xUI		85 + 6xUI	ns
$T_{HS-PREPARE}$ + HS-0 State Prior to Sync	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$		145 + 10xUI			ns
State After Last HS Burst	$T_{HS-TRAIL}$		60 + 4xUI			ns
Initialization Time	T_{INIT}		100			µs
Length of any LP Period	T_{LPX}		50			ns
Skew-Calibration Sync Pattern, 0xFFFF	$T_{SKEWCAL\_SYNC}$			16		UI
Skew-Calibration Initial Time	$T_{SKEWCAL}$				100	µs
			2^{15}			UI

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Skew-Calibration Periodic Time	$T_{SKEWCAL}$				10	µs
			2^{10}			UI
AC ELECTRICAL CHARACTERISTICS / C-PHY HS TRANSMITTER (*Note 2*)						
Common-Level Variations	$\Delta V_{CPTX(HF)}$	> 450MHz			15	mV_{RMS}
	$\Delta V_{CPTX(LF)}$	50 to 450MHz			25	mV_{PEAK}
Rise Time	t_R	Strong 0 to weak 1 transition, -58mV to +58mV, Z_{ID} = 100Ω			0.285	UI
Fall Time	t_F	Strong 1 to weak 0 transition, +58mV to -58mV, Z_{ID} = 100Ω			0.285	UI
Rise Time and Fall Time	$t_{RISE-FALL-MAX}$	-58mV to +58mV, Z_{ID} = 100Ω. (*Note 8*)			360	ps
Differential-Mode Reflection Coefficient (*Note 7*)	Sdd_{TX}	f_{hMAX} = 1.25GHz		-5		dB
		f_{MAX} = 1.875GHz		-3		
Common-Mode Reflection Coefficient (*Note 7*)	Scc_{TX}	f_{MAX} = 1.875GHz		-3		dB
C-PHY Lane Bit Rate	C_{BR}		182		5700	Mbps
CSI-2 Output Inter-packet Spacing	t_{SPACE}			300ns + 370UI		ns
UI Instantaneous	UI_{INST}		0.4		12.5	ns
AC ELECTRICAL CHARACTERISTICS / C-PHY GLOBAL OPERATION TIMING (*Note 2*)						
Time that the Transmitter Drives the 3-Wire LP-000 Line State Immediately Before the HS_+x Line State Starting the HS Transmission	$t_{3-PREPARE}$		38		95	ns
Time that the Transmitter Drives LP-111 Following a HS Burst	$t_{3-HS-EXIT}$		100			ns
Transmitted Length of any Low-Power State Period	t_{LPX}		50			ns
Initialization Time	t_{INIT}		100			µs
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING						
Output Fall Time	t_F	70% to 30%, C_L = 20pF to 100pF, 1kΩ pullup to V_{DDIO} (*Note 2*)	20 x V_{DDIO}/5.5V		150	ns
I^2C Wake Time	t_{WAKEUP}	From power-up or rising edge of PWDNB to local register access. For remote register access, I^2C Wake Time is the same as Lock Time (t_{LOCK1}, t_{LOCK2}).		2.25		ms

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / I²C TIMING						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2C_MST_BT = 010, I2C_SLV_SH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2C_MST_BT = 101, I2C_SLV_SH = 01)	100		400	
		High f_{SCL} range: (I2C_MST_BT = 111, I2C_SLV_SH = 00)	400		1000	
Start Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated Start Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	

Electrical Characteristics (continued)

(V_{TERM} = 1.14V to 1.26V, V_{DD18} = 1.7V to 1.9V, V_{DD} = 0.95V to 1.05V or V_{DD} = 1.14V to 1.26V, V_{DDIO} = 1.7V to 3.6V, T_A = -40°C to +105°C, EP connected to PCB ground, typical values are at V_{TERM} = 1.2V, V_{DD18} = V_{DDIO} = 1.8V, V_{DD} = 1.0V, T_A = +25°C, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load On Each Bus Line	C_B	(*Note 2*)			100	pF
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (CRYSTAL) (X1/OSC, X2) (*Note 2*)						
Frequency	f_{XTAL}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}				±200	ppm
AC ELECTRICAL CHARACTERISTICS / REFERENCE CLOCK REQUIREMENTS (EXTERNAL INPUT ON X1/OSC, X2 UNCONNECTED) (*Note 2*)						
Frequency	F_{REF}			25		MHz
Frequency Stability + Frequency Tolerance	f_{TN}		-200		+200	ppm
Duty Cycle	DC		40	50	60	%
Input Jitter	t_{JIN}	Sinusoidal jitter < 1MHz (rising edge)			150	ps (p-p)
Input Rise Time	t_R	10% to 90%		5		ns
Input Fall Time	t_F	90% to 10%		5		ns

Note 1: Limits are 100% tested at T_A = +105°C unless otherwise noted. Limits within the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: MFP pin speed programmed to fastest setting (TTS = 00). See *Multifunction Pin Configuration* for details regarding MFP speed programming.

Note 4: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

Note 5: Additional capacitance up to 60pF (D-PHY) or 90pF (C-PHY) at RX termination center tap.

Note 6: Differential-mode and common-mode reflection coefficient are compliant with MIPI D-PHY V1.2 requirements over all specified operating frequencies.

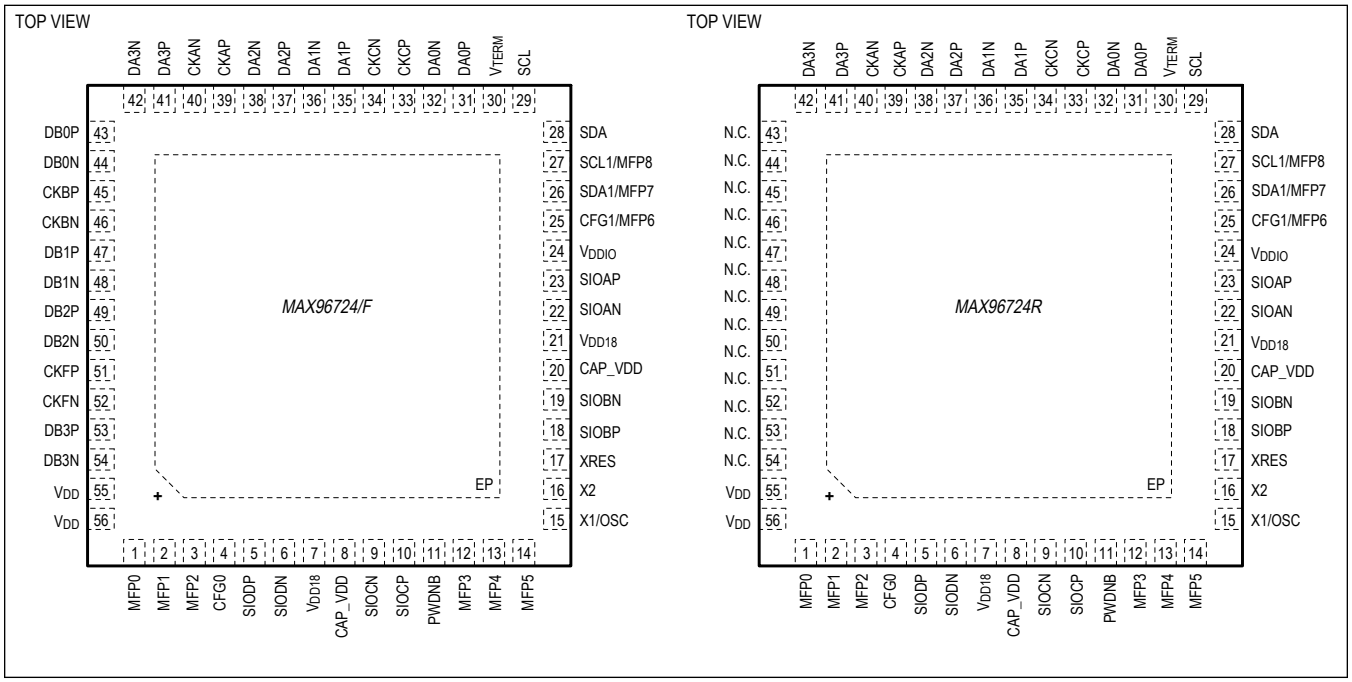
Note 7: Differential-mode and common-mode reflection coefficient are compliant with MIPI C-PHY V1.0 requirements over all specified operating frequencies.

Note 8: For rates ≤ 1.5Gbps, t_R and t_F shall be ≤ min (0.4UI, $t_{RISE-FALL-MAX}$).

Note 9: From power-up, release of RESET_LINK, or rising edge of the PWDNB pin, to rising edge of the LOCK pin. t_{RD} must be <90ms if serializer powers up or is released from link reset before deserializer. For more information, see the GMSL2 Link Lock section.

Note 10: Production tested using ECS ECS-250-18-33Q-DS crystal.

Pin Configurations



Pin Description

PIN	NAME	FUNCTION MODE			FUNCTION
		GMSL2	GMSL1	MAX96724R	
GMSL2/GMSL1 SERIAL LINK					
5	SIODP	SIODP	SIODP	SIODP	Noninverted Serial-Data I/O D.
6	SIODN	SIODN	SIODN	SIODN	Inverted Serial-Data I/O D.
10	SIOCP	SIOCP	SIOCP	SIOCP	Noninverted Serial-Data I/O C.
9	SIOCN	SIOCN	SIOCN	SIOCN	Inverted Serial-Data I/O C.
18	SIOBP	SIOBP	SIOBP	SIOBP	Noninverted Serial-Data I/O B.
19	SIOBN	SIOBN	SIOBN	SIOBN	Inverted Serial-Data I/O B.
23	SIOAP	SIOAP	SIOAP	SIOAP	Noninverted Serial-Data I/O A.
22	SIOAN	SIOAN	SIOAN	SIOAN	Inverted Serial-Data I/O A.
CSI-2 INTERFACE — PORT A/C/D (* denotes default state after power-up)					
31	DA0P	DA0P* DC0P A0A C0A	DA0P* DC0P A0A C0A	DA0P* DC0P A0A C0A	DA0P: D-PHY Port A Data Lane 0 (4-lane) DC0P: D-PHY Port C Data Lane 0 (2-lane) A0A: C-PHY Port A Lane 0 Output A (4-lane) C0A: C-PHY Port C Lane 0 Output A (2-lane)
32	DA0N	DA0N* DC0N A0B C0B	DA0N* DC0N A0B C0B	DA0N* DC0N A0B C0B	DA0N: D-PHY Port A Data Lane 0 (4-lane) DC0N: D-PHY Port C Data Lane 0 (2-lane) A0B: C-PHY Port A Lane 0 Output B (4-lane) C0B: C-PHY Port C Lane 0 Output B (2-lane)

PIN	NAME	FUNCTION MODE			FUNCTION
		GMSL2	GMSL1	MAX96724R	
33	CKCP	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED* CKCP CKAP(alt) A0C C0C	DISABLED: CKCP is Disabled in 4-Lane Mode CKCP: D-PHY Port C Clock Lane (2-lane) CKAP(alt): D-PHY Port A CLK ALT (4-lane) A0C: C-PHY Port A Lane 0 Output C (4-lane) C0C: C-PHY Port C Lane 0 Output C (2-lane)
34	CKCN	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED* CKCN CKAN(alt) A1A C1A	DISABLED: CKCN is Disabled in 4-Lane Mode CKCN: D-PHY Port C Clock Lane (2-lane) CKAN(alt): D-PHY Port A CLK ALT (4-lane) A1A: C-PHY Port A Lane 1 Output A (4-lane) C1A: C-PHY Port C Lane 1 Output A (2-lane)
35	DA1P	DA1P* DC1P A1B C1B	DA1P* DC1P A1B C1B	DA1P* DC1P A1B C1B	DA1P: D-PHY Port A Data Lane 1 (4-lane) DC1P: D-PHY Port C Data Lane 1 (2-lane) A1B: C-PHY Port A Lane 1 Output B (4-lane) C1B: C-PHY Port C Lane 1 Output B (2-lane)
36	DA1N	DA1N* DC1N A1C C1C	DA1N* DC1N A1C C1C	DA1N* DC1N A1C C1C	DA1N: D-PHY Port A Data Lane 1 (4-lane) DC1N: D-PHY Port C Data Lane 1 (2-lane) A1C: C-PHY Port A Lane 1 Output C (4-lane) C1C: C-PHY Port C Lane 1 Output C (2-lane)
37	DA2P	DA2P* DD0P A2A D0A	DA2P* DD0P A2A D0A	DA2P* DD0P A2A D0A	DA2P: D-PHY Port A Data Lane 2 (4-lane) DD0P: D-PHY Port D Data Lane 0 (2-lane) A2A: C-PHY Port A Lane 2 Output A (4-lane) D0A: C-PHY Port D Lane 0 Output A (2-lane)
38	DA2N	DA2N* DD0N A2B D0B	DA2N* DD0N A2B D0B	DA2N* DD0N A2B D0B	DA2N: D-PHY Port A Data Lane 2 (4-lane) DD0N: D-PHY Port D Data Lane 0 (2-lane) A2B: C-PHY Port A Lane 2 Output B (4-lane) D0B: C-PHY Port D Lane 0 Output B (2-lane)
39	CKAP	CKAP* CKDP DISABLED A2C D0C	CKAP* CKDP DISABLED A2C D0C	CKAP* CKDP DISABLED A2C D0C	CKAP: D-PHY Port A Clock Lane (4-lane) CKDP: D-PHY Port D Clock Lane (2-lane) DISABLED: When CKAP/N(alt) is Enabled A2C: C-PHY Port A Lane 2 Output C (4-lane) D0C: C-PHY Port D Lane 0 Output C (2-lane)
40	CKAN	CKAN* CKDN DISABLED A3A D1A	CKAN* CKDN DISABLED A3A D1A	CKAN* CKDN DISABLED A3A D1A	CKAN: D-PHY Port A Clock Lane (4-lane) CKDN: D-PHY Port D Clock Lane (2-lane) DISABLED: When CKAP/N(alt) is Enabled A3A: C-PHY Port A Lane 3 Output A (4-lane) D1A: C-PHY Port D Lane 1 Output A (2-lane)
41	DA3P	DA3P* DD1P A3B D1B	DA3P* DD1P A3B D1B	DA3P* DD1P A3B D1B	DA3P: D-PHY Port A Data Lane 3 (4-lane) DD1P: D-PHY Port D Data Lane 1 (2-lane) A3B: C-PHY Port A Lane 3 Output B (4-lane) D1B: C-PHY Port D Lane 1 Output B (2-lane)
42	DA3N	DA3N* DD1N A3C D1C	DA3N* DD1N A3C D1C	DA3N* DD1N A3C D1C	DA3N: D-PHY Port A Data Lane 3 (4-lane) DD1N: D-PHY Port D Data Lane 1 (2-lane) A3C: C-PHY Port A Lane 3 Output C (4-lane) D1C: C-PHY Port D Lane 1 Output C (2-lane)
CSI-2 INTERFACE — PORT B/E/F (* denotes default state after power-up)					
43	DB0P	DB0P* DE0P B0A E0A	DB0P* DE0P B0A E0A	N.C.	DB0P: D-PHY Port B Data Lane 0 (4-lane) DE0P: D-PHY Port E Data Lane 0 (2-lane) B0A: C-PHY Port B Lane 0 Output A (4-lane) E0A: C-PHY Port E Lane 0 Output A (2-lane) N.C.: No Connect

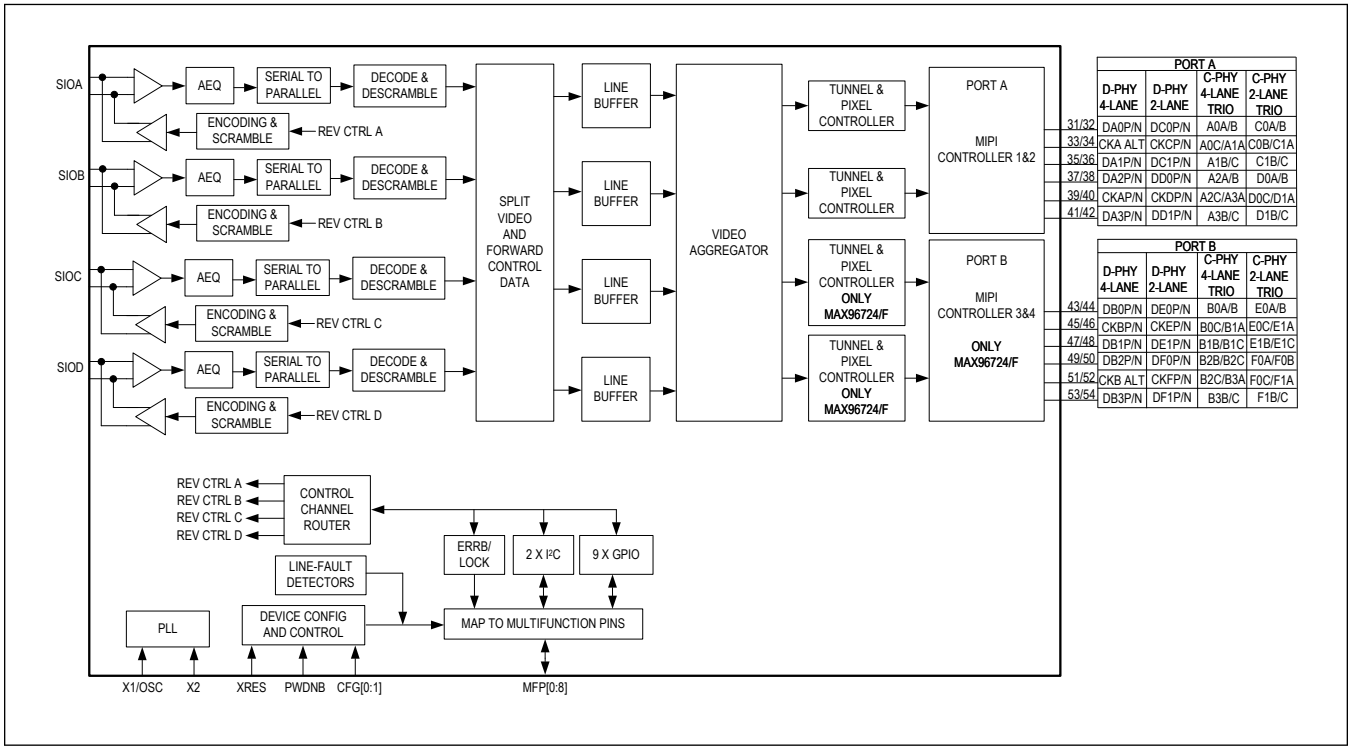
PIN	NAME	FUNCTION MODE			FUNCTION
		GMSL2	GMSL1	MAX96724R	
44	DB0N	DB0N* DE0N B0B E0B	DB0N* DE0N B0B E0B	N.C.	DB0N: D-PHY Port B Data Lane 0 (4-lane) DE0N: D-PHY Port E Data Lane 0 (2-lane) B0B: C-PHY Port B Lane 0 Output B (4-lane) E0B: C-PHY Port E Lane 0 Output B (2-lane) N.C.: No Connect
45	CKBP	CKBP* CKEP DISABLED B0C E0C	CKBP* CKEP DISABLED B0C E0C	N.C.	CKBP: D-PHY Port B Clock Lane (4-lane) CKEP: D-PHY Port E Clock Lane (2-lane) DISABLED: When CKBP/N(alt) is Enabled B0C: C-PHY Port B Lane 0 Output C (4-lane) E0C: C-PHY Port E Lane 0 Output C (2-lane) N.C.: No Connect
46	CKBN	CKBN* CKEN DISABLED B1A E1A	CKBN* CKEN DISABLED B1A E1A	N.C.	CKBN: D-PHY Port B Clock Lane (4-lane) CKEN: D-PHY Port E Clock Lane (2-lane) DISABLED: When CKBP/N(alt) is Enabled B1A: C-PHY Port B Lane 1 Output A (4-lane) E1A: C-PHY Port E Lane 1 Output A (2-lane) N.C.: No Connect
47	DB1P	DB1P* DE1P B1B E1B	DB1P* DE1P B1B E1B	N.C.	DB1P: D-PHY Port B Data Lane 1 (4-lane) DE1P: D-PHY Port E Data Lane 1 (2-lane) B1B: C-PHY Port B Lane 1 Output B (4-lane) E1B: C-PHY Port E Lane 1 Output B (2-lane) N.C.: No Connect
48	DB1N	DB1N* DE1N B1C E1C	DB1N* DE1N B1C E1C	N.C.	DB1N: D-PHY Port B Data Lane 1 (4-lane) DE1N: D-PHY Port E Data Lane 1 (2-lane) B1C: C-PHY Port B Lane 1 Output C (4-lane) E1C: C-PHY Port E Lane 1 Output C (2-lane) N.C.: No Connect
49	DB2P	DB2P* DF0P B2A F0A	DB2P* DF0P B2A F0A	N.C.	DB2P: D-PHY Port B Data Lane 2 (4-lane) DF0P: D-PHY Port F Data Lane 0 (2-lane) B2A: C-PHY Port B Lane 2 Output A (4-lane) F0A: C-PHY Port F Lane 0 Output A (2-lane) N.C.: No Connect
50	DB2N	DB2N* DF0N B2B F0B	DB2N* DF0N B2B F0B	N.C.	DB2N: D-PHY Port B Data Lane 2 (4-lane) DF0N: D-PHY Port F Data Lane 0 (2-lane) B2B: C-PHY Port B Lane 2 Output B (4-lane) F0B: C-PHY Port F Lane 0 Output B (2-lane) N.C.: No Connect
51	CKFP	DISABLED* CKFP CKBP(alt) B2C F0C	DISABLED* CKFP CKBP(alt) B2C F0C	N.C.	DISABLED: CKFP Output is Disabled in 4-Lane CKFP: D-PHY Port F Clock Lane (2-lane) CKBP(alt): D-PHY Port B Clock Lane (4-lane) B2C: C-PHY Port B Lane 2 Output C (4-lane) F0C: C-PHY Port F Lane 0 Output C (2-lane) N.C.: No Connect
52	CKFN	DISABLED* CKFN CKBN(alt) B3A F1A	DISABLED* CKFN CKBN(alt) B3A F1A	N.C.	DISABLED: CKFN is Disabled in 4-Lane CKFN: D-PHY Port F Clock Lane (2-lane) CKBN(alt): D-PHY Port B CLK ALT (4-lane) B3A: C-PHY Port B Lane 3 Output A (4-lane) F1A: C-PHY Port F Lane 1 Output A (2-lane) N.C.: No Connect

PIN	NAME	FUNCTION MODE			FUNCTION
		GMSL2	GMSL1	MAX96724R	
53	DB3P	DB3P* DF1P B3B F1B	DB3P* DF1P B3B F1B	N.C.	DB3P: D-PHY Port B Data Lane 3 (4-lane) DF1P: D-PHY Port F Data Lane 1 (2-lane) B3B: C-PHY Port B Lane 3 Output B (4-lane) F1B: C-PHY Port F Lane 1 Output B (2-lane) N.C.: No Connect
54	DB3N	DB3N* DF1N B3C F1C	DB3N* DF1N B3C F1C	N.C.	DB3N: D-PHY Port B Data Lane 3 (4-lane) DF1N: D-PHY Port F Data Lane 1 (2-lane) B3C: C-PHY Port B Lane 3 Output C (4-lane) F1C: C-PHY Port F Lane 1 Output C (2-lane) N.C.: No Connect
MULTIFUNCTION PINS — (* denotes default state after power-up) (GMSL1 has limited GPIO tunneling capability)**					
1	MFP0	FSYNC LMN0 GPIO0 DISABLED*	FSYNC LMN0 GPI0 GPIO0** DISABLED*	FSYNC LMN0 GPIO0 DISABLED*	FSYNC: FSync Output (Master) or Input (Slave) LMN0: Line Fault Monitor Input GPI0: GPI-GPO Sync Signal GPIO0: General Purpose I/O. Disabled with 1MΩ pulldown. DISABLED: Disabled at Power-Up and is Hi-Z
2	MFP1	VSYNC0 DE0 HSYNC0 LMN1 GPIO1 DISABLED*	VSYNC0 DE0 HSYNC0 CNTL0 CNTL1 LMN1 GPI1 GPIO1** DISABLED*	VSYNC0 DE0 HSYNC0 LMN1 GPIO1 DISABLED*	VSYNC0: Vertical Sync Push-Pull Output DE0: Data Enable Push-Pull Output HSYNC0: Horizontal Sync Push-Pull Output CNTL0: Control 0 with Push-Pull Driver CNTL2: Control 2 with Push-Pull Driver LMN1: Line Fault Monitor Input GPI1: Input GPI-GPO Sync GPIO1: 1MΩ pulldown DISABLED: Pin is Disabled and is Hi-Z
3	MFP2	LMN2 GPIO2 DISABLED*	CNTL1 CNTL3 LMN2 GPI2 GPIO2** DISABLED*	LMN2 GPIO2 DSIABLED*	CNTL1: Control 1 with Push-Pull Driver CNTL3: Control 3 with Push-Pull Driver LMN2: Line Fault Monitor Input GPI2: Input GPI-GPO Sync GPIO2: 1MΩ pulldown DISABLED: Pin is Disabled and is Hi-Z
12	MFP3	VSYNC1 DE1 HSYNC1 LMN3 GPIO3 DISABLED*	VSYNC1 DE1 HSYNC1 CNTL4 LMN3 GPI3 GPIO3** DISABLED*	VSYNC1 DE1 HSYNC1 LMN3 GPIO3 DISABLED*	VSYNC1: Vertical Sync Push-Pull Output DE1: Data Enable Push-Pull Output HSYNC1: Horizontal Sync Push-Pull Output CNTL4: Control Output 4 with Push-Pull Driver LMN3: Line Fault Monitor Input GPI3: Input for GPI-GPO Sync GPIO3: 1MΩ pulldown DISABLED: Pin is Disabled and is Hi-Z
13	MFP4	LOCK* GPIO4	LOCK* GPIO4**	LOCK* GPIO4	LOCK: Open-Drain with 40kΩ Pullup to V_{DDIO} GPIO4: General Purpose I/O
14	MFP5	ERRB* ERRB/LOCK GPIO5	ERRB* ERRB/LOCK GPIO5**	ERRB* ERRB/LOCK GPIO5	ERRB: Open-Drain with 40kΩ Pullup to V_{DDIO} ERRB/LOCK: Open-Drain with 40kΩ Pullup to V_{DDIO} GPIO5: General Purpose I/O
25	CFG1/MFP6	CFG1 GPIO_Aggregation GPO6 DISABLED*	CFG1 GPIO_Aggregation GPO6** DISABLED*	CFG1 GPIO_Aggregation GPO6 DISABLED*	CFG1: Latched at Power-Up. See Table 8. GPIO_Aggregation: See User Guide. GPO6: General-Purpose Output. DISABLED: After Latching CFG1 at Power-Up, Pin is disabled and goes to Hi-Z.

PIN	NAME	FUNCTION MODE			FUNCTION
		GMSL2	GMSL1	MAX96724R	
26	SDA1/MFP7	SDA1* FSYNC(ALT) VSYNC2 DE2 HSYNC2 GPIO7	FSYNC(ALT) VSYNC2 DE2 HSYNC2 GPIO7**	SDA1* FSYNC(ALT) VSYNC2 DE2 HSYNC2 GPIO7	SDA1: Open-Drain with 40kΩ Pullup to V_{DDIO} FSYNC (ALT): ALT. Output (Master) or Input (Slave) VSYNC2: Vertical Sync Push-Pull Output DE2: Data Enable Push-Pull Output HSYNC2: Horizontal Sync Push-Pull Output GPIO7: General Purpose I/O
27	SCL1/MFP8	SCL1* VSYNC3 DE3 HSYNC3 GPIO8	VSYNC3 DE3 HSYNC3 GPIO8**	SCL1* VSYNC3 DE3 HSYNC3 GPIO8	SCL1: Open-Drain Output with 40kΩ Pullup to V_{DDIO} VSYNC3: Vertical Sync Push-Pull Output DE3: Data Enable Push-Pull Output HSYNC3: Horizontal Sync Push-Pull Output GPIO8: General Purpose I/O
MISCELLANEOUS — (Table 3)					
4	CFG0	CFG0	CFG0	CFG0	Latched at Power-Up (Table 7)
8, 20	CAP_VDD	CAP_VDD	CAP_VDD	CAP_VDD	Decoupling for V_{DD} Core Supply.
11	PWDNB	PWDNB	PWDNB	PWDNB	PWDNB: Active-low, Input with a 1MΩ Pulldown to Ground. Set low to enter Power-Down mode. Attach pullup resistor to VDDIO for normal operation.
28	SDA	SDA	SDA	SDA	Open-Drain with 40kΩ Pullup to V_{DDIO}.
29	SCL	SCL	SCL	SCL	Open-Drain with 40kΩ Pullup to V_{DDIO}.
15	X1/OSC	X1/OSC	X1/OSC	X1/OSC	25MHz Crystal/Clock Source.
16	X2	X2	X2	X2	Connect to 25MHz. OSC requires X2 to be floating.
17	XRES	XRES	XRES	XRES	Connect 402Ω 1% resistor to ground.
POWER SUPPLIES — (Table 3)					
7, 21	V_{DD18}	V_{DD18}	V_{DD18}	V_{DD18}	1.8V Analog Supply.
24	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	3.3V or 1.8V I/O Power Supply.
30	V_{TERM}	V_{TERM}	V_{TERM}	V_{TERM}	1.2V CSI C/D-PHY Supply.
55, 56	V_{DD}	V_{DD}	V_{DD}	V_{DD}	1.2/1.0V core supply. 1.2V uses an internal regulator. 1.0V will bypass the regulator.
EP	EP	EP	EP	EP	Exposed Pad connect to ground.

Functional Diagrams

MAX96724



PORT A			
D-PHY 4-LANE	D-PHY 2-LANE	C-PHY 4-LANE TRIO	C-PHY 2-LANE TRIO
DA0P/N	DC0P/N	A0A/B	C0A/B
CKA ALT	CKCP/N	A0C/A1A	C0B/C1A
DA1P/N	DC1P/N	A1B/C	C1B/C
DA2P/N	DD0P/N	A2A/B	D0A/B
CKAP/N	CKDP/N	A2C/A3A	D0C/D1A
DA3P/N	DD1P/N	A3B/C	D1B/C

PORT B			
D-PHY 4-LANE	D-PHY 2-LANE	C-PHY 4-LANE TRIO	C-PHY 2-LANE TRIO
DB0P/N	DE0P/N	B0A/B	E0A/B
CKBP/N	CKEP/N	B0C/B1A	E0C/E1A
DB1P/N	DE1P/N	B1B/B1C	E1B/E1C
DB2P/N	DF0P/N	B2B/B2C	F0A/F0B
CKB ALT	CKFP/N	B2C/B3A	F0C/F1A
DB3P/N	DF1P/N	B3B/C	F1B/C

Detailed Description

Descriptions

Thermal Management

Power consumption of the MAX96724/F/R varies based on the use case. Care must be taken by the user to provide sufficient heat dissipation with proper board design and cooling techniques. The package's exposed pad must be connected to the PCB ground plane by an array of vias. This approach simultaneously provides the lowest electrical and thermal impedances.

System thermal management must keep the operating junction temperature below +125°C to meet electrical specifications and avoid impacting device reliability.

Refer to Tutorial 4083 (*www.maximintegrated.com/thermal-tutorial*) for further guidance.

Control Channel Programming

MAX96724/F/R internal registers can be accessed locally via any of the two available I²C ports. Lower indexed ports have a higher priority in the case of simultaneous queries. By default, remote GMSL serializer register access is available via I²C port 0 only. However, the internal I²C crossover enables any of the two ports to connect to the control channel, which thereby provides access to remote serializer registers. Only one of the two ports can access the control channel at a given time, and the other I²C port then functions essentially as remote pass-throughs from the perspective of the serializer. See I²C for further details regarding the routing of I²C ports in the MAX96724/F/R. For multi-master configurations with microcontrollers connected to both the serializer and deserializer, bus contention can be avoided by using register settings to disable the remote control channel.

Host-to-Peripheral Main I²C and Pass-Through I²C Communication

When communicating between a host and peripheral, main and pass-through I²C operation is the same. An I²C tunnel across the GMSL2 link connects the host's I²C master to the remote I²C slave. This logically connects separated I²C buses, enabling I²C transactions across the serial link to occur (with some delay) as if performed on the same physical I²C bus. The GMSL2 serializer and deserializer are intermediary devices; the host I²C master connects to a GMSL2 device I²C slave, and the peripheral I²C slave connects to a GMSL2 device I²C master.

For example, when the host I²C master transacts on one side of the link (local-side), the I²C slave of the local-side GMSL2 device forwards data to the other side (remote-side). Data is then received by the I²C master of the remote-side GMSL2 device, which in turn generates the same I²C transaction with the peripheral slave I²C. The remote-side GMSL2 device sends back any I²C data expected by the local-side.

The I²C interface uses clock stretching (holding SCL low) to account for timing differences between master and slave and to allow time for data to be forwarded and received across the serial link. The host I²C master and peripheral I²C slave must support clock stretching by the GMSL2 device.

SDA and SCL lines operate as both an input and an open-drain output. External pullup resistors are required on SDA and SCL.

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus a R/W bit, register address bytes, one or more data bytes, and finally a STOP condition.

Register addresses are 16-bits wide. Single or multiple data bytes can be written or read (by address autoincrements).

I²C Write Packet Format

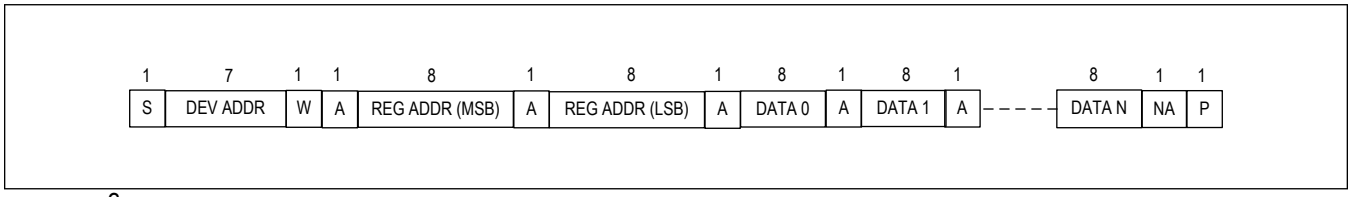


Figure 1. I²C Write Packet Format

I²C Read Packet Format

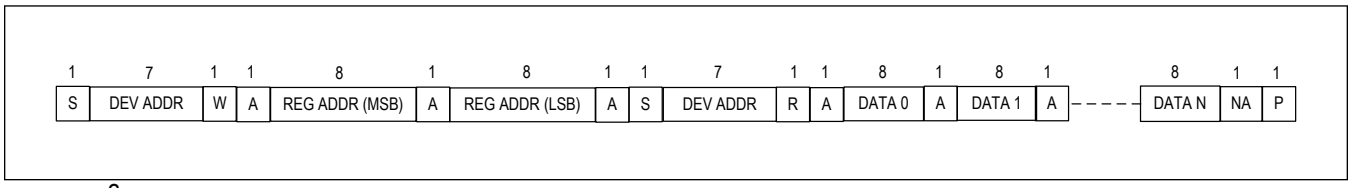


Figure 2. I²C Read Packet Format

Device Address

Each device on the I²C control channel must have a unique address. This includes both peripherals and GMSL devices. The GMSL2 device address is set to one of several 7-bit addresses according to the voltage level of the CFG0 pin at power-up. See CFG Latch at Power-up Pins for further details. Note that the device address can be changed after power-up by writing to the DEV_ADDR register.

Advanced GMSL User Documentation

This data sheet contains electrical specifications, pin and functional descriptions, feature overviews and register definitions. Designers must also have the following information to correctly design using this device:

- The **GMSL2 Channel Specification** contains physical layer requirements for the PCB traces, cables and connectors that constitute the GMSL2 link.
- The **GMSL2 Hardware Design Guide** contains recommendations for PCB design, applications circuits, selection of external components and guidelines for use of GMSL2 signal integrity tools.
- The **GMSL2 User Guide** contains detailed programming guidelines for GMSL2 device features.
- **Errata sheets** contain deviations from published device specifications and are specific to part number and revision ID.

Contact the factory for the above documents and for additional guidance on MAX96724/F/R features.

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

PARAMETER	PIN	NOMINAL VOLTAGE	MIN	TYP	MAX	UNIT
Supply Range	V_{TERM}		1.14	1.2	1.26	V
	V_{DD18}		1.7	1.8	1.9	
	V_{DD}	1.0V	0.95	1.0	1.05	
		1.2V	1.14	1.2	1.26	
	V_{DDIO}		1.7		3.6	
Operating Junction Temperature (T_J)			-40		125	°C

External Component Requirements

Critical components that must be connected to the specified pins for correct functionality.

Table 3. External Component Requirements

COMPONENT	SYMBOL	CONDITION		VALUE	UNIT
XRES	R_{XRES}	Connect the resistor to XRES and ground.		402 ±1%	Ω
Link Isolation Capacitors	C_{LINK}	Place in close proximity to the SIO pins.	GMSL2, GMSL1 - HIM Enabled	0.1	µF
			GMSL2, GMSL1 - HIM Enabled	0.22	
Termination for Coax mode	R_{TERM}	Place near associated SIO_N pin.		49.9 ±1%	Ω
Crystal		Place as close as possible to pins X1 and X2.		25MHz ±200ppm	
V_{DDIO} Decoupling Capacitors*		Place as close as possible to pin V_{DDIO}.		0.01µF + 10µF	
V_{DD18} Decoupling Capacitors*		Place as close as possible to each V_{DD18} pin.		2 x 0.01µF + 10µF	
V_{DD} Decoupling Capacitors*		Place as possible to each V_{DD} pin.		2 x 0.1µF + 10µF	
V_{TERM} Decoupling Capacitors*		Place as close as possible to pin V_{TERM}.		0.01µF + 10µF	
CAP_VDD Decoupling Capacitors		Place as close as possible to each CAP_VDD pin.		2 x 0.1µF + 10µF	
Configuration Pins (CFG0, CFG1/ MFP6)	R1, R2			See Table 7.	
	R1, R2			See Table 8.	
Power-over-Coax (PoC)		Contact the factory, PoC cannot be used with line-fault.			
Line Fault	User Guide	Refer to GMSL User Guide for proper line-fault setup.			

* Power supply decoupling capacitor values are recommendations only. It is the responsibility of the board designer to determine what decoupling is necessary for the specific application.

ESD Protection

Table 4. ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SIO_	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±8		kV
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, Coax Configuration		±6		
		ISO10605, R_D = 330Ω, C_S = 150pF, Contact Discharge, STP Configuration		±4		
		ISO10605, R_D = 330Ω, C_S = 150pF, Air Discharge		±8		
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V
All Other Pins	V_{ESD}	Human Body Model (HBM), R_D = 1.5kΩ, C_S = 100pF		±3		kV
		AEC-Q100-011 Rev-C1, Charged Device Model (CDM)		750		V

Figures

GMSL2 Reverse Channel Serial Outputs

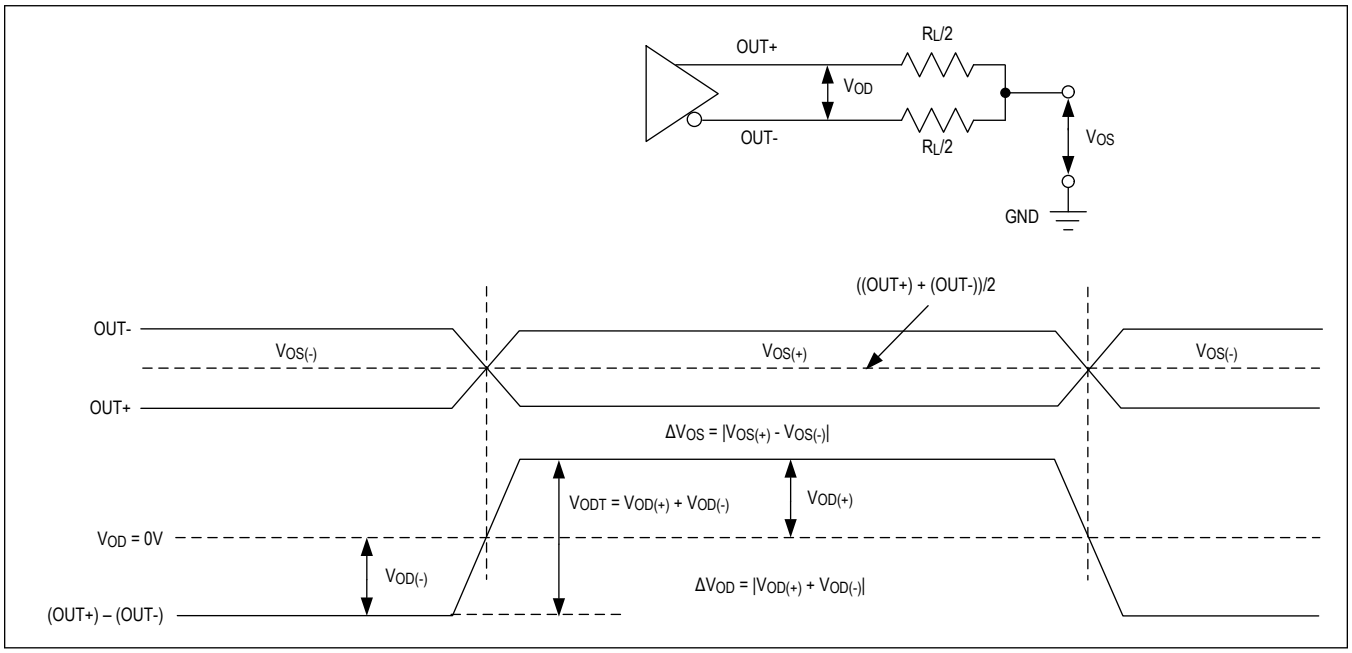


Figure 3. GMSL2 Serial Output Parameters

GMSL1 Serial Output Parameters

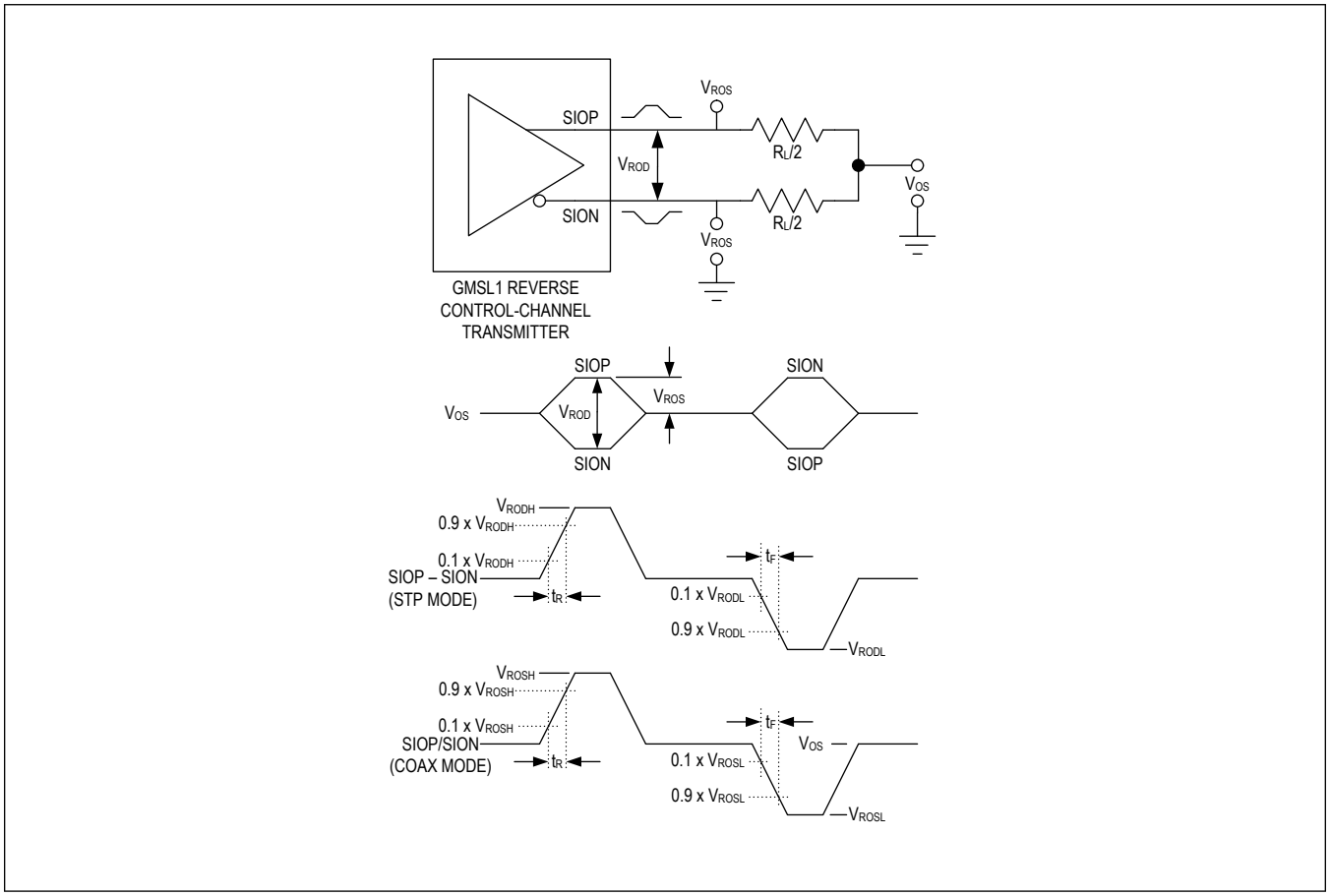


Figure 4. GMSL1 Serial Output Parameters

C-PHY Possible ΔV_{CPTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

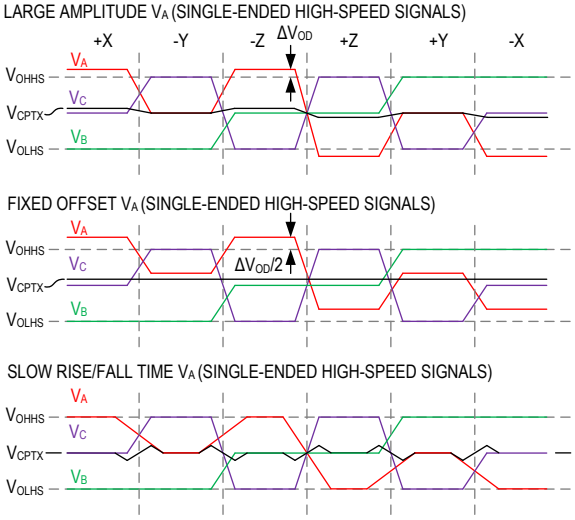


Figure 5. C-PHY Possible ΔV_{CPTX} and ΔV_{OD} Distortions of Single-Ended HS Signals

C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

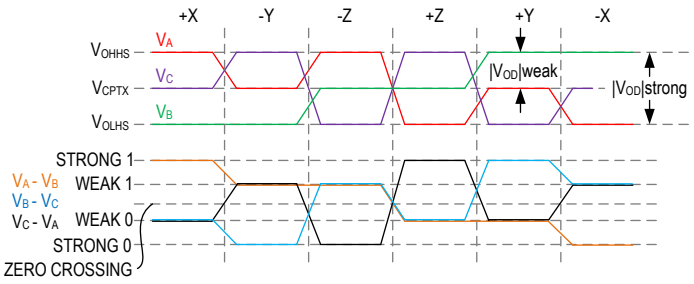


Figure 6. C-PHY Ideal Single-Ended and Resulting Differential High-Speed Signals

GMSL2 Video Latency

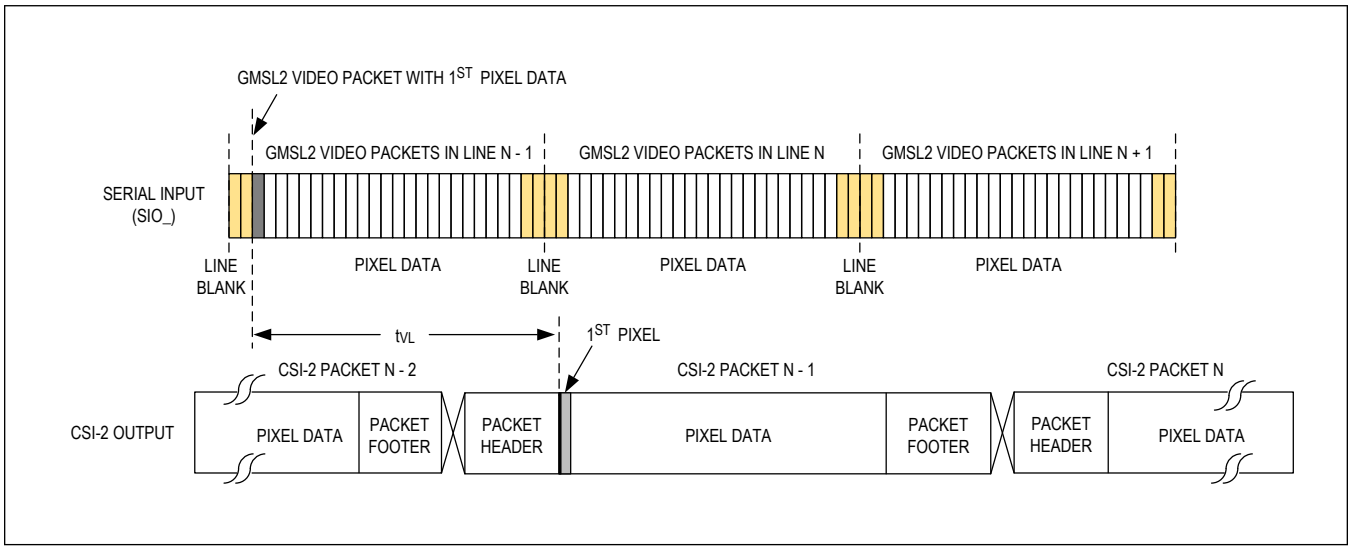


Figure 7. GMSL2 Video Latency

GMSL2 GPI-to-GPO Delay and Skew

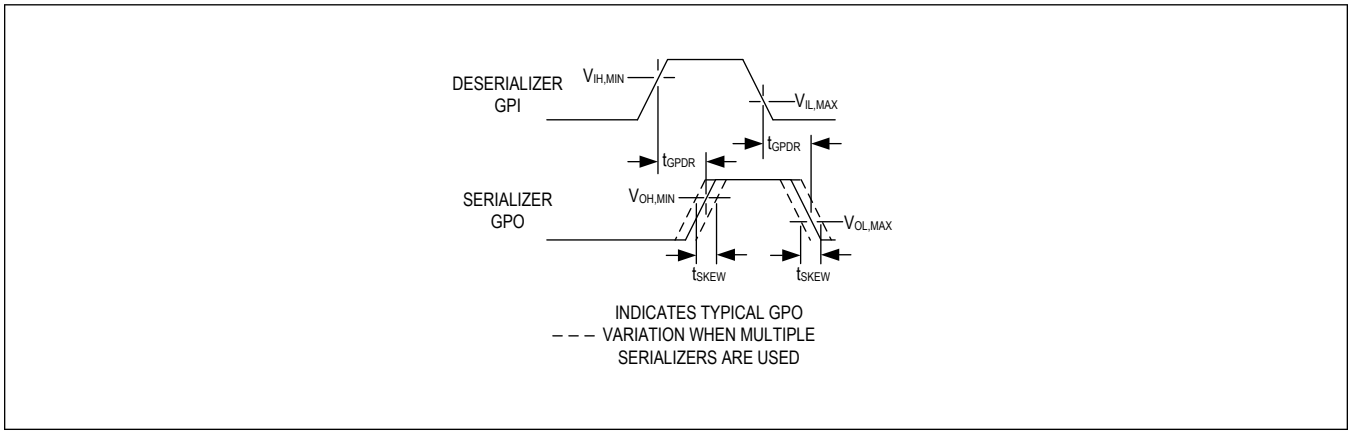


Figure 8. GMSL2 GPI-to-GPO Delay and Skew

GMSL1 Lock Time

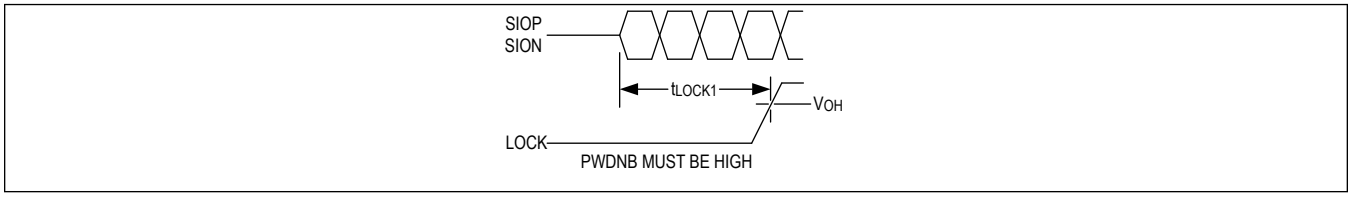


Figure 9. GMSL1 Lock Time

GMSL1 Power-up Delay

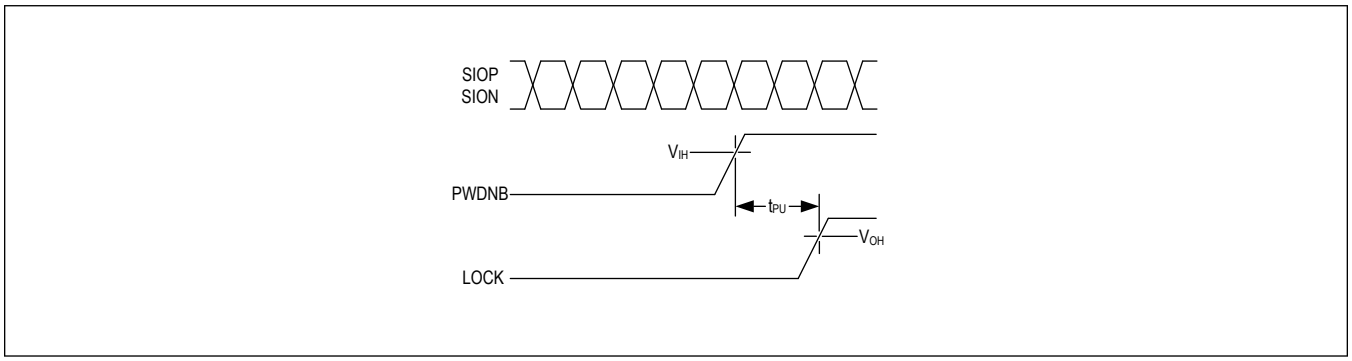


Figure 10. GMSL1 Power-up Delay

GMSL1 Video Latency

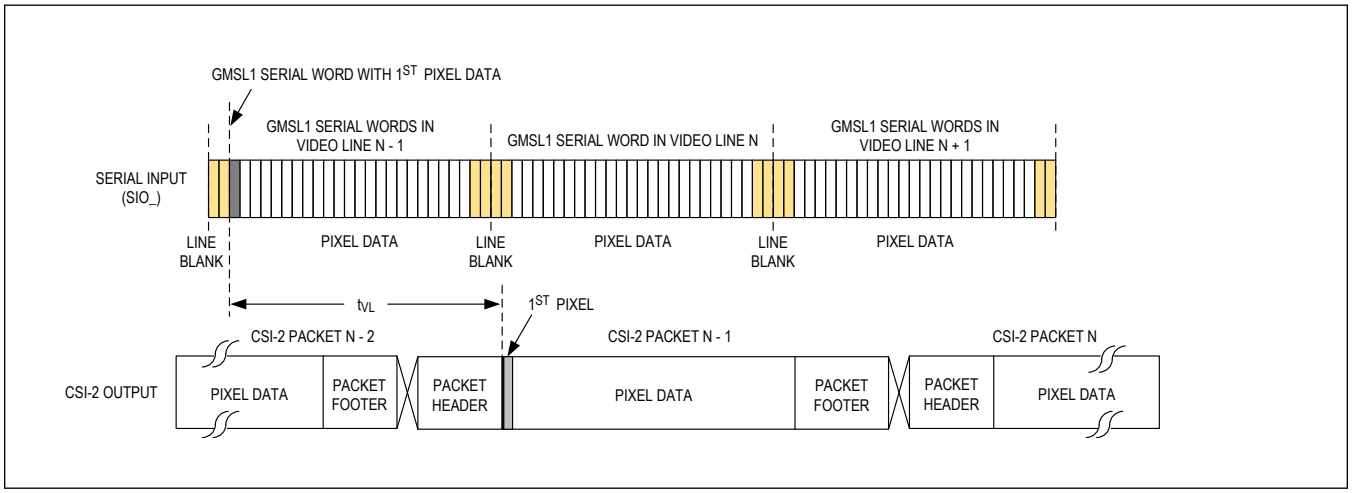


Figure 11. GMSL1 Video Latency

GMSL1 GPI-to-GPO Delay

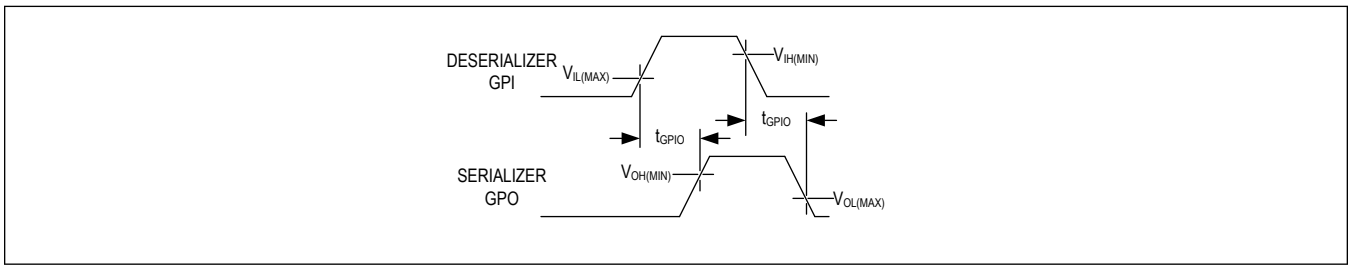


Figure 12. GMSL1 GPI-to-GPO Delay

Product Overview

The MAX96724/F/R deserializer converts four GMSL2 or GMSL1 inputs to up to four independent MIPI CSI-2 C/D-PHY outputs containing a combined total of up to four lanes. It also sends and receives control channel data, enabling full-duplex transmission of forwarding path video and bidirectional control data over low-cost 50Ω coax or 100Ω STP cables

that meet the GMSL2 channel specification. In GMSL1 mode, the MAX96724/F/R can be paired with first-generation GMSL1 serializers or GMSL2 serializers in GMSL1 mode, operating up to 3.12Gbps.

The MAX96724/F/R has 4-lane or dual 2-lane CSI-2 v1.3 output ports that support data rates of 80Mbps to 2.5Gbps per lane in D-PHY mode or 182Mbps to 5.7Gbps per lane in C-PHY mode. The number of active data lanes in each CSI-2 port is programmable with 4-lane ports providing one, two, three, or four lanes and 2-lane ports providing one or two lanes.

The MAX96724/F/R is intended to be paired with GMSL2 serializers or previous generation GMSL1 serializers. Several common multi-sensor use cases are supported with the MAX96724/F/R being particularly well suited to surround-view sensor systems that include four physically separate cameras or other sensors. The simplest conceptual system following this topology includes four independent sensors, each with a serializer routed to the MAX96724/F/R's four GMSL inputs. The resulting CSI-2 streams from each sensor are then routed to two independent CSI-2 C/D-PHY outputs in 2x2-lane mode, providing a system with four independent inputs and two outputs where data from two sensors are aggregated and routed to a dedicated output.

MAX96724/F/R has built-in ease of use functionality:

- Use Case Profiles
- MIPI Controller Mapping
- D-PHY to C-PHY conversion
- Automatic Detection of Pixel or Tunnel Mode per Input

Cabling Options

GMSL1/2 supports operation with either 50Ω coaxial or 100Ω shielded twisted pair (STP) cabling. Contact the factory for GMSL Channel Specifications. Coax or STP operation is determined by the level of CFG pins at power-up as detailed in the *CFG Latch at Power-up Pins* section. In coax mode, use only the noninverted SIO pin. In STP configurations, both the noninverted and inverted SIO pins are enabled by default. Any unused SIO pins should be AC terminated with 50Ω to ground.

GMSL2 Bandwidth Information and Calculation

Forward links have a fixed link rate of 3Gbps or 6Gbps for the MAX96724/F/R. The reverse-link rate is fixed at 187.5Mbps. The GMSL2 protocol and channel coding overhead is roughly 14%. This leaves approximately 2.6Gbps or 5.2Gbps of data throughput in the forward direction and 162Mbps in the reverse direction. Ensure that the worst-case use cases do not exceed the available throughput of the forward and reverse links. The GMSL SerDes GUI includes a bandwidth (BW) calculator that can be used for initial bandwidth requirements estimates. It is recommended to consult the factory for high-bandwidth use cases to ensure error-free performance.

Table 5 provides rough estimates of the bandwidth utilization for each communication channel.

Table 5. Forward- and Reverse-Link Bandwidth Utilization

DATA	APPROXIMATE BANDWIDTH UTILIZATION
Video (Forward Path Only)	H x V x fps x bpp x (1+ (% horizontal blanking)/100 + (% vertical blanking)/100) x 1.14 Maximum bandwidth is limited by pixel clock rate PCLK. Pixel mode: GMSL PCLK = Received MIPI data rate/bpp Pixel mode (double pixel mode): PCLK = MIPI data rate/(2*bpp) Tunneling mode: GMSL PCLK = Received MIPI data rate/24 Maximum GMSL PCLK: 300MHz for 3Gbps link rate Maximum GMSL PCLK = 600MHz for 6Gbps link rate
I^2C	18 to 60 x I^2C clock rate, depending on available link bandwidth
GPIO	60 x GPIO transition rate without delay compensation 80 x GPIO transition rate with delay compensation enabled

Definitions:

H = Horizontal resolution (active pixels)

V = Vertical resolution (active video lines)

fps = Frames per second

bpp = Bits per pixel

MIPI data rate = Aggregate data rate of all lanes in the MIPI interface

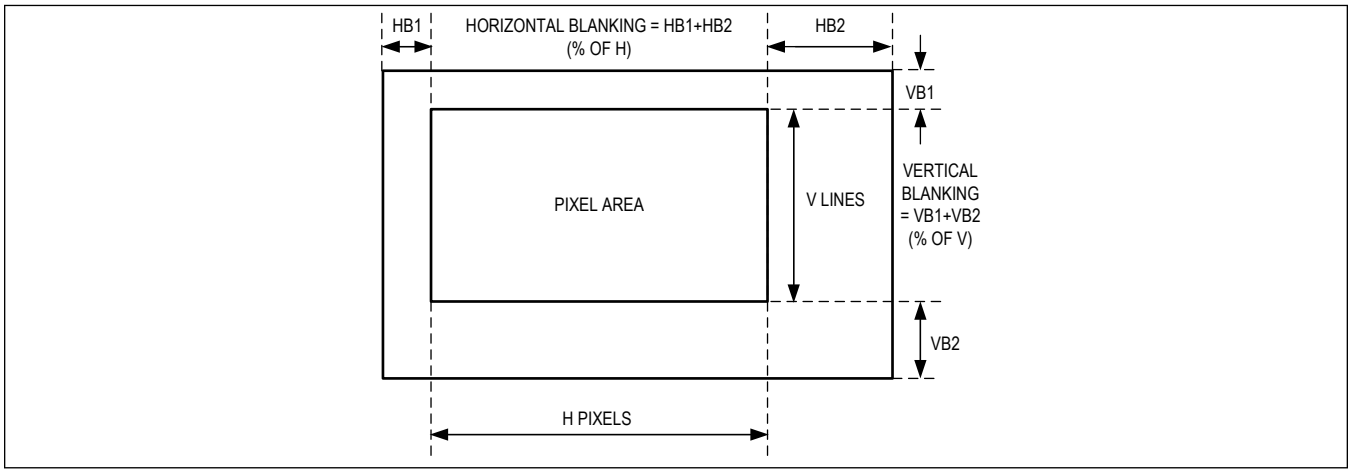


Figure 13. Video Frame Format for Bandwidth Calculation

GMSL2 Minimum Blanking

The minimum horizontal blanking period needed by the CSI-2 serializers and deserializers is the maximum of either 40 pixels or 300ns + 370UI (where UI is defined as the period of CSI-2 lane rate). For most cases, 40 pixels is the larger number. The minimum vertical blanking period is one video line. The minimum vertical front porch is one video line. Recommended vertical back porch is one video line.

Minimum vertical back porch in pixel mode is the maximum of:

- 40 pixels
- 300ns + 370UI

Minimum vertical back porch in tunneling mode is the maximum of:

- 40 pixels
- 200 PCLK periods + 233ns, where PCLK = total MIPI data rate/24
- 300ns + 370UI

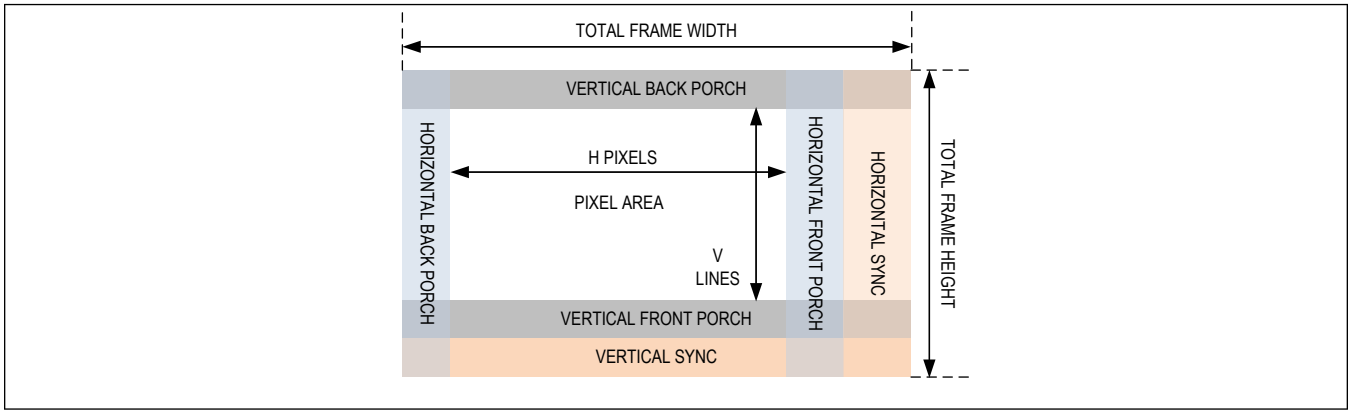


Figure 14. Video Timing

AEQ (Automatic Adaptive Equalization)

The GMSL2 devices automatically adapt the forward path receiver characteristics to compensate for insertion loss and

return loss characteristics of the channel, which consist of the cables, connectors, temperature, and PCBs. This approach optimizes performance on any channel that meets the GMSL2 channel specifications. Initial adaptation is performed during link lock and then is invoked at every second to track temperature and voltage variations. This is critical for a changing automotive safety application.

GMSL2 Overview

GMSL2 uses a packet-based protocol to seamlessly share the link bandwidth between communication channels in a flexible way. Bandwidth allocation is dynamic so that if a certain channel is not active, it does not consume any link bandwidth, and all the remaining active channels can share the full link bandwidth. Maximum packet size is limited to prevent a single channel from utilizing the link bandwidth for an extended time. The same data protocol is used on forward and reverse channels and for both video and control-channel data.

GMSL2 provides extensive data integrity and safety features. Some of these features include CRC error detection that enables identification of errors in the video or control-data streams. In the case of control-channel CRC errors, automatic retransmission of the flagged packet maximizes control-channel speed and reliability.

GMSL2 devices incorporate numerous link-margin optimization and monitoring functions that ensure high link margin and robust functionality. Continuous adaptive equalization occurs every second to optimize link margin to adapt to environmental changes and cable aging. An eye-opening monitor function provides continuous link-margin diagnosis.

Tunneling vs. Pixel Modes

The MAX96724/F/R is specifically designed for Advanced Driver Assistance Systems (ADAS), where data integrity is a key safety requirement. Prior GMSL2 solutions supported only Pixel mode for transporting received data from a MIPI CSI-2 interface over the GMSL link. In Pixel mode, the CSI-2 data is depacketized at the serializer's CSI-2 input interface. The received CSI-2 packet header includes an error correction code (ECC), which is checked and removed at the serializer input. The received CSI-2 packet footer contains the CSI-2 cyclic redundancy check (CRC), which is also checked and removed.

Video line pixel data and video routing information, such as data type and virtual channel, are received and extracted at the CSI-2 interface. Both video pixel data, control channel data, and routing information are input into a scheduler in the serializer. The scheduler packetizes and encapsulates the data using GMSL protocol and sequences data transmission across the GMSL link. Video data transport across the GMSL link is protected by line CRCs that are part of the GMSL protocol.

The deserializer receives the GMSL packets and verifies the GMSL2 line CRCs. A CSI-2 interface at the deserializer output encapsulates each video line using CSI-2 protocol and outputs it in CSI-2 format across a CSI-2 interface to the SoC. See Figure 15.

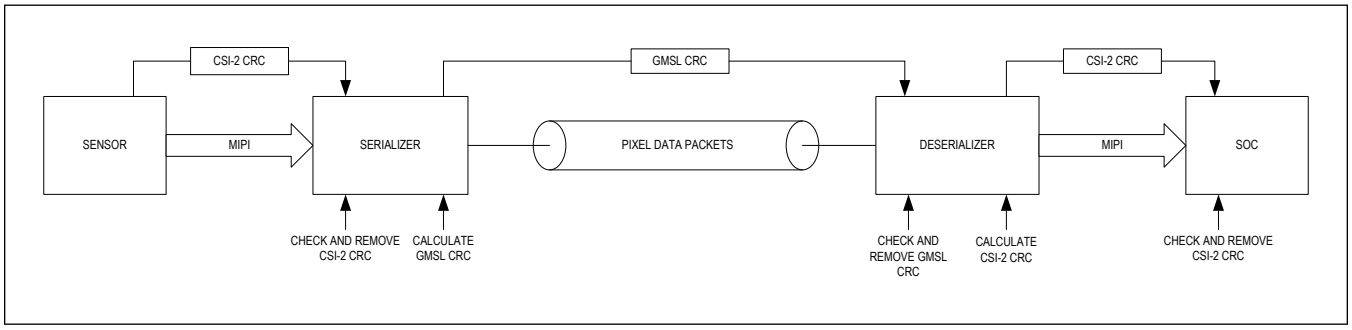


Figure 15. Pixel Mode

In Tunneling mode, the received CSI-2 ECC byte and CRC bytes are checked at the serializer input. These, as well as routing and pixel data, are received as a byte stream. The byte stream is split into smaller packets that are encapsulated using GMSL2 protocol.

The serializer adds a line CRC, protecting transmission across the GMSL channel. This CRC covers the entire GMSL2 packetized byte stream for a video line. See Figure 16. The deserializer receives the transmitted GMSL2 packets

and control channel packets, checks and removes the GMSL CRC, separates the video data from control data, and reconstructs each received CSI-2 packet that is the output to the SoC on a CSI-2 interface. A CRC is calculated on the video data output on the CSI-2 interface. This CRC is compared by the deserializer to the original CRC received from the video source. This comparison guarantees that the entire data packet output on the standard MIPI interface is identical to that received at the serializer input. Tunneling mode is more bandwidth-efficient if multiple data types are being sent. Because data received at the serializer input and data output from the deserializer are verified to be identical, Tunneling mode does not allow for the processing of video data, such as watermarking or lossy data compression. Different data rate and different lane count on serializer and deserializer are still possible. See Figure 16.

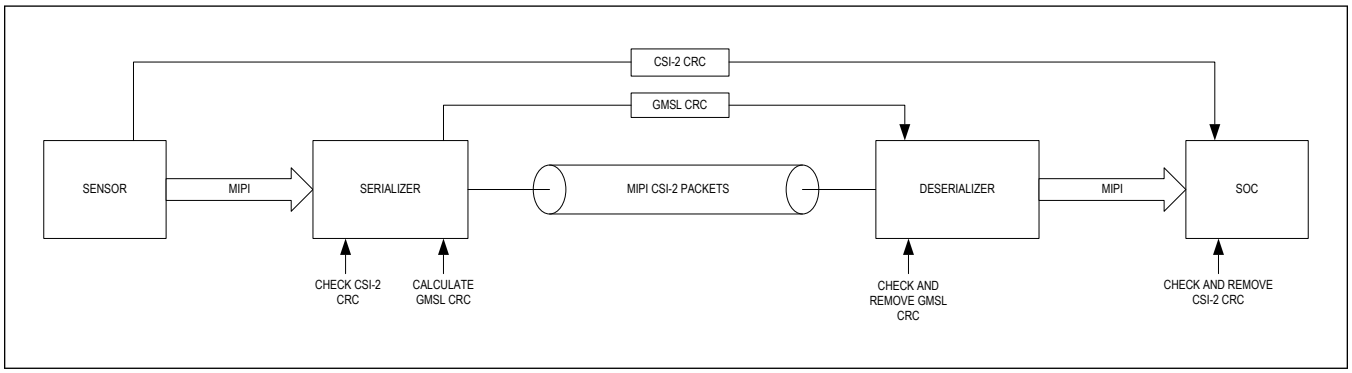


Figure 16. Tunneling Mode

Video Pipes, Aggregation, and Replication

In GMSL2 mode, the transmission of video data is based on the concept of video pipes. Carrying data in pipes allows GMSL2 to bridge different digital video interfaces.

A pipe carries a video stream (or streams) and video synchronization data. Each pipe operates in one of three modes. In all modes, a pipe can carry multiple concurrent video streams, with each stream having different virtual channels and data types.

Mode 1: Streams with constant bits per pixel (bpp) of up to 24bpp. The bpp of the streams must be the same.
Mode 2: Streams with 16, 14, 12, 10 or 8bpp. Streams less than 16bpp are padded with zeros.
Mode 3: Streams with two different bpp. The bpp of one stream must be twice the bpp of the other stream. The higher bpp stream maximum is 24bpp.

Modes 1 and 3 carry data at full bandwidth but put more restrictions on bpp than mode 2. Mode 2 allows streams with different bpp, but streams of less than 16bpp are carried using more bandwidth than necessary on the GMSL2 link because of zero padding. Mode 1 or 3 are sufficient for most applications. Mode 2 requires less programming and is more convenient if the application does not require maximum link bandwidth.

The MAX96724/F/R has four GMSL input ports, each accommodating up to four independent pipes in GMSL2 mode. In GMSL1 mode, only a single, dedicated video pipe is available per link. Each pipe can be mapped to any one of the incoming GMSL video streams; as a result, up to four pipes can be mapped to a single GMSL2 output port. In GMSL1 mode, a total of four video pipes is available with a fixed mapping between each GMSL1 input and a single internal pipe as shown in Figure 17. In mixed GMSL1/GMSL2 systems, the GMSL1 input streams are routed to the dedicated GMSL1 pipe associated with each active GMSL1 input. Incoming GMSL2 streams can be routed to any of the available pipes that are not dedicated to an active GMSL1 input. The pipes are available sources for synchronous aggregation.

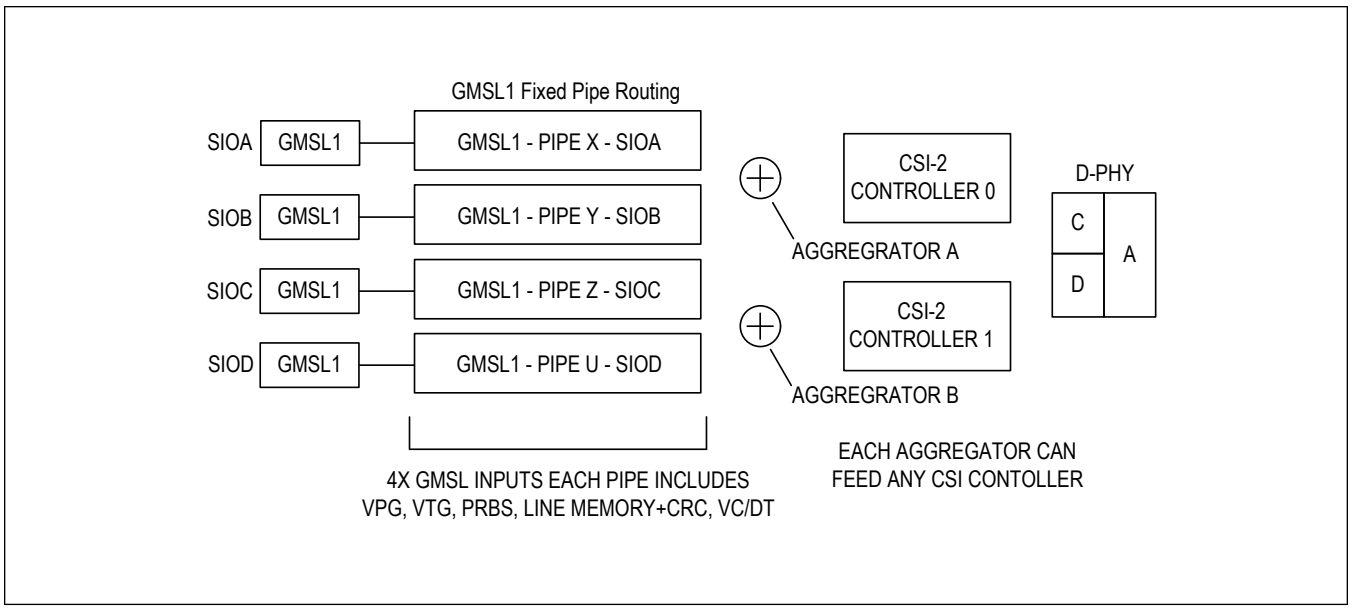


Figure 17. Video Pipes and Routing

A single camera requires either one or two pipes for Pixel mode depending on whether it supports high dynamic range (HDR) imaging. Tunnel mode uses only one pipe, even if there are multiple data types and VC's on the incoming GMSL input. A Pixel mode example is shown in Figure 18 illustrates an application in which one link interfaces to an HDR camera (two dedicated pipes) while the other two links stream video from standard cameras (one dedicated pipe).

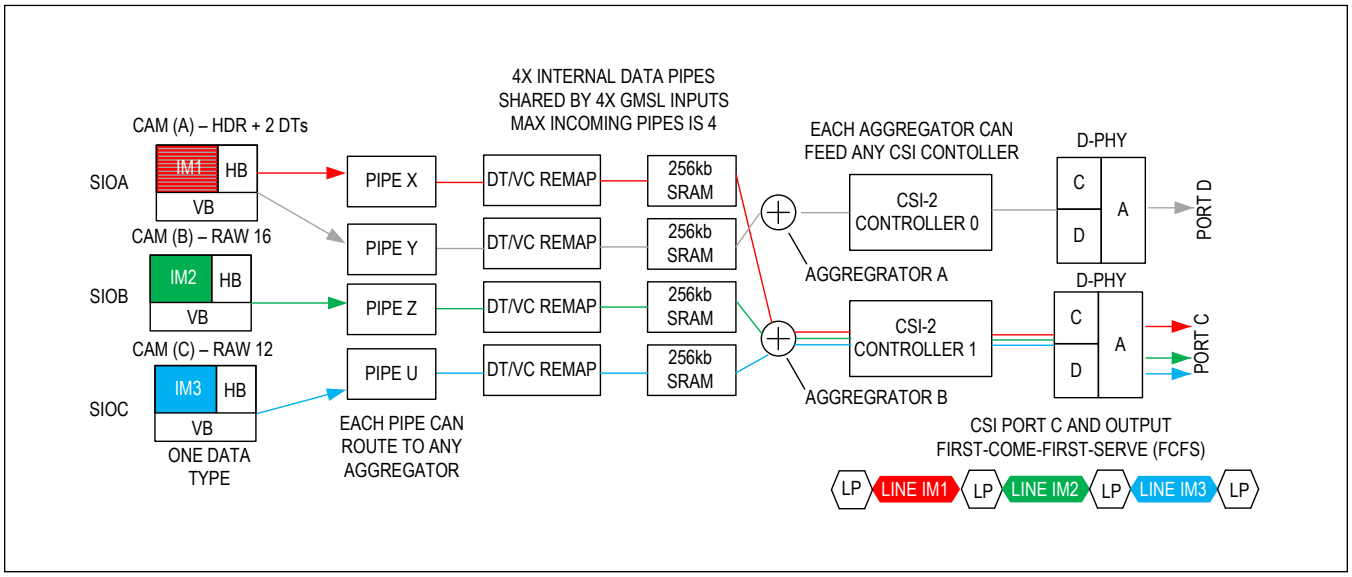


Figure 18. MAX96724/F/R Video Pipe Example with Partial FCFS Aggregation

When video data is received by one of the MAX96724/F/R's GMSL inputs, it is immediately forwarded to one of the internal video pipes. Note that a single pipe can carry many separate streams, provided that they comply with certain mode-dependent format limitations. The channel ID of each incoming CSI stream can be reassigned if desired. Video data then fills the dedicated line buffer associated with each pipe as controlled by the sync data. Each line buffer can be routed to any one of the four aggregators, which can be used to combine data from multiple video pipes and/or virtual

channels within a single CSI-2 stream. Only one aggregator can read data out of a given buffer. Up to four pipes can be aggregated by one aggregator. Video data can be routed according to DT or VC based on the source CSI-2 packet's DT/VC, or it can be routed by a DT/VC assigned in the MAX96724/F/R.

Aggregated data is typically read out from line memory on a first come first served (FCFS) basis. In this case, data from all four video pipes are visible to the aggregators. The order in which the line memories reach filled status is the order in which they are read out. In this case, the outgoing CSI data streams can be viewed as independent parallel streams that may have independent timing, although they may be effectively synchronized depending on the nature of the video sources used. Alternatively, data can be aggregated in specific sequences corresponding to side-by-side (4WxH) or line-interleaved (Wx4H) output formats. All data sources must use the same resolution and virtual channel assignment, and they must be precisely synchronized. The resulting output is a single stream consisting of a superframe that holds video data from all aggregated streams. Synchronous aggregation can effectively provide a single combined image output from multiple sensors, such as a single image surround-view stream. Side-by-side aggregation combines incoming streams from up to four sensors, resulting in a frame that has equal height and up to 4x the width of single sensor output. Pixel mode supports both 4WxH and Wx4H modes. Tunnel mode only supports Wx4H mode.

The MAX96724/F/R includes features that minimize the disruption resulting from one of the links failing in multi-link systems that use aggregation. With systems using synchronous aggregation, the MAX96724/F/R masks the failed link's video data with 0's. This allows overall timing to continue as expected, enabling the remaining video streams to proceed uninterrupted. Similarly, with systems using FCFS aggregation, the video stream associated with a link that has failed will be terminated at the end of a line to avoid a sudden disruption that may impact other streams using the same physical interface.

The MAX96724/F/R supports a new feature called "cut-through" in the Tunnel mode that allows the controller to start reading from the memory sooner. Register PKT_START_ADDR can adjust when to start reading from memory after written to. This allows an extension to the video line memory for lines longer than 4096 pixels and can also reduce latency by allowing the ability to read the memory quicker. Once data is read out, it cannot be read out a second time. Figure 19 shows the MAX96724/F/R memory operation.

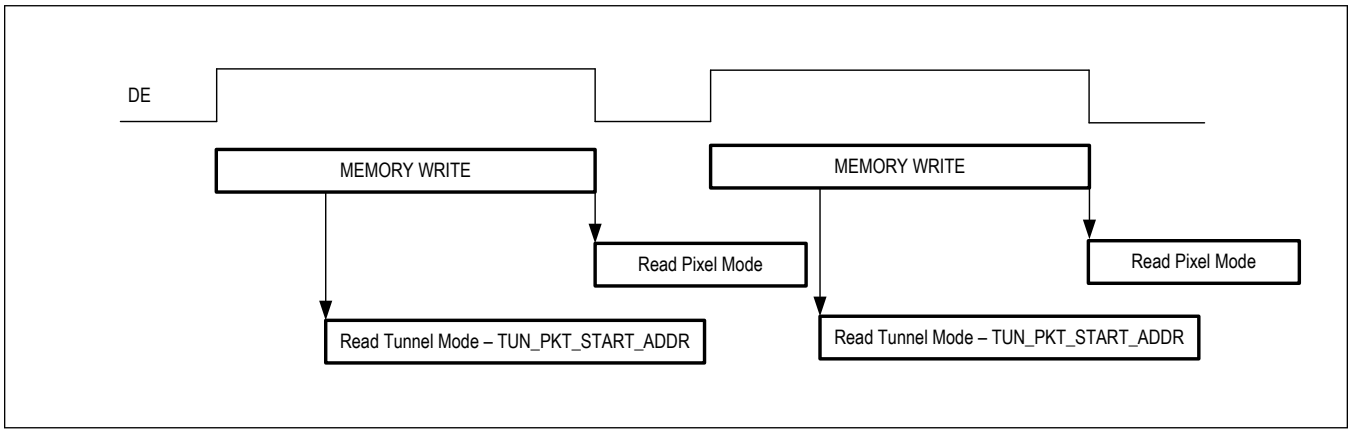


Figure 19. GMSL2 Memory Reading and Writing

To prevent buffer overflow, the CSI-2 port data rate must be programmed to an equal to or greater rate than the incoming data rate. Programming the output rate to be faster than the bandwidth of the incoming video or data increases packet spacing (LP time between packets). The video memory has built-in overflow detection - BACKTOP11. This occurs when the video bandwidth is higher than the data going out on the MIPI port, not giving a chance for the memory to empty. No reformatting of the data occurs in Tunnel mode. It is a requirement for functional safety that the video data is unchanged, such that it can be compared against the tunneled CSI-2 CRC by the host. After data exits a retiming buffer, it goes through a data type (DT) and virtual channel (VC) reassignment stage. If the video source has a CSI-2 output, packets DT and VC can each be left as-is or reassigned by register programming.

The MAX96724/F/R GMSL2 protocols allocate 24 bits of each packet for video content to effectively use the GMSL2 forward channel bandwidth. The serializer and MAX96724/F/R contain the double Pixel mode, which place x2 8bpp/

10bpp/12bpp into the same packet. See bpp8dbl / bpp10dbl / bpp12dbl bitfields in the register map for more information.

Frame Sync

In some camera applications, a frame-sync signal is required by the sensors to synchronize the output of a frame with the other cameras in the system. The MAX96724/F/R can generate FSYNC signal internally or receive an FSYNC signal from external SoC and send it over to the sensor through the GMSL reverse channel. MFP0 or MFP7 is programmed to receive the external FSYNC signal and MAX96724/F/R are programmed as slaves. To generate the internal FSYNC, the MAX96724/F/R are programmed as masters. Refer to the MAX96724/F/R User Guide for more information.

Vertical and Data Enable or Data Valid Sync Outputs

The MAX96724/F/R can output the vertical sync (VS) and data enable/data valid (DE/DV) of a video stream to monitor the video timing by a processor. This feature provides access to VS and DE/DV signals not available directly at the CSI-2 output. Refer to the MAX96724/F/R User Guide for how to use this feature.

D-PHY to C-PHY Packet Conversion

MAX96724/F/R has the ability to convert Imager sensor D-PHY packets to C-PHY packets while still maintaining ASIL functionality. This is done automatically when C-PHY is selected.

Control Channel Latency

All control channels exhibit finite latency. Typical latency for each function is given in Table 6. For I^2C, which requires an immediate ACK from the receiver following each byte, clock stretching is used to temporarily pause communication as the ACK propagates through the control channel. All I^2C devices that communicate over the link must support clock stretching.

Table 6. Control Channel Latency

FUNCTION	FORWARD	REVERSE
I^2C	< 10µs	< 10µs

I^2C

The MAX96724/F/R includes two independent I^2C interfaces. These interfaces are the only means by which local or remote (serializer) registers can be accessed. The master µC is typically located on the MAX96724/F/R side of the link, although this is not strictly required, and communication can be initiated by a device on either side of the link. For correct operation, the control channel of each of the MAX96724/F/R's links must be configured in the same mode as the serializer connected to that link. I^2C outputs are open drain and require appropriately-sized external pullup resistors for proper operation.

In general, each of the I^2C ports can be used to access internal MAX96724/F/R registers, remote serializer registers, and remote peripheral registers. Both ports provide concurrent local register access. Each GMSL2 link provides a dedicated control channel through which any one of the ports can communicate with either a remote serializer connected to that link or with any remote peripherals connected to the serializer's control channel port. Routing of the I^2C ports to each control channel is independent, enabling different combinations of local ports to access the control channel and the tunneled channels of each GMSL link. Regarding local (deserializer) register access, both ports provide simultaneous local access with lower indexed ports having the highest priority. In I^2C mode, a local port's local register access cannot be disconnected unless the port is disabled. Therefore, all active I^2C ports have local register access at all times.

Remote serializer registers are visible only by means of the dedicated GMSL2 link control channel, which supports only a single port. Therefore, only one port at a time can access remote registers over a given link. By default, port 0 is routed to the control channel of each link. With appropriate configuration, port 1 can also be routed to the control channel to support remote serializer register access. Any links operated in GMSL1 mode provide only a single control channel with both serializer and peripheral register access.

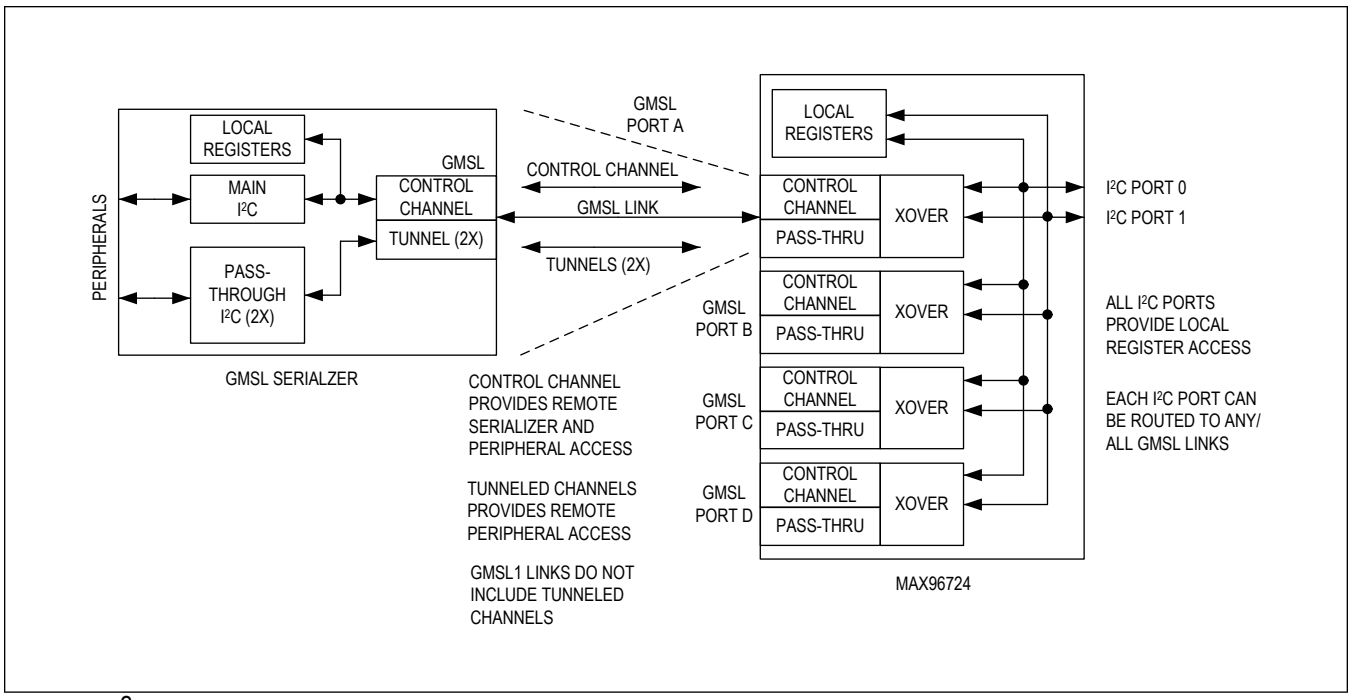


Figure 20. I^2C Routing

General Purpose Inputs and Outputs (GPIO)

Multifunction pins can be programmed as GPI (input), GPO (push-pull output or open-drain output, although some MFP pins only support open-drain output), or GPIO (bidirectional input/output). Most GPIOs can also be programmed for 1MΩ or 40kΩ pullup or pulldown (or none). The state of each GPIO can be read or written by register either locally, using any of the two I^2C ports, or remotely via the I^2C interface that is routed to the GMSL2 control channel. Refer to the MAX96724/F/R User Guide for proper GPIO setup.

Link Error Generator

Each of the GMSL links includes a configurable error generator that injects errors into the outgoing data stream immediately prior to transmission. The deserializer injects errors into the reverse channel; the serializer injects errors into the forward channel. The receiving device detects, counts, and flags the errors, enabling a thorough validation of the system's response to error conditions of varying severity.

GMSL1 Backwards Compatibility

The MAX96724/F/R is designed to pair with any GMSL1 serializer with high immunity mode (HIM). However, the device does not support the entire range of features available across all GMSL1 serializers. GMSL1 backward compatibility is only supported with forward link rates from 500Mbps to 3.12Gbps and a reverse link rate of 1Mbps. When paired with a GMSL2 serializer for GMSL1 operation, both devices must be configured to use GMSL1 compatibility mode. When the MAX96724/F/R is paired with a legacy GMSL1 only serializer, the MAX96724/F/R must be configured for GMSL1 compatibility mode, and the available forward link rate is reduced to the rate limitations of the specified GMSL1 serializer. Refer to the MAX96724/F/R User Guide for more information.

Video PRBS Generator/Checker

GMSL2 devices include built-in video PRBS generators/checkers for video link testing for pixel mode operation. For example, a serializer's PRBS generator can be used in conjunction with a deserializer's PRBS checker to test the GMSL2 video channel that connects the two devices. Here, the MAX96724/F/R's PRBS checker functionality compares the received PRBS stream with the predicted PRBS data to establish any errors. To run the video PRBS test, refer to the MAX96724/F/R GMSL2 User Guide for more information.

RoR (Reference over Reverse)

Reference clock over reverse channel (RoR) is a GMSL clock operating mode where the serializer receives its reference clock from the deserializer over the GMSL link. RoR eliminates the need for a crystal oscillator on the serializer side of the link.

In RoR mode, the serializer’s timing reference is extracted from the signal sent on the reverse channel. The recovered clock coming from the deserializer is used by the serializer on-chip phase-locked loop (PLL) to synthesize the serializer output reference clock RCLKOUT.

RoR mode is automatically supported when the serializer is configured in RoR mode.

The removal of the crystal oscillator in RoR provides several advantages:

- Reduced system cost
- Increased reliability
- Reduced board area
- Simplified board layout

CFG Latch at Power-up Pins

At power-up or after reset, the voltages at the CFG0 and CFG1/MFP6 pins are sampled. The sampled level is used to set the initial value of certain registers.

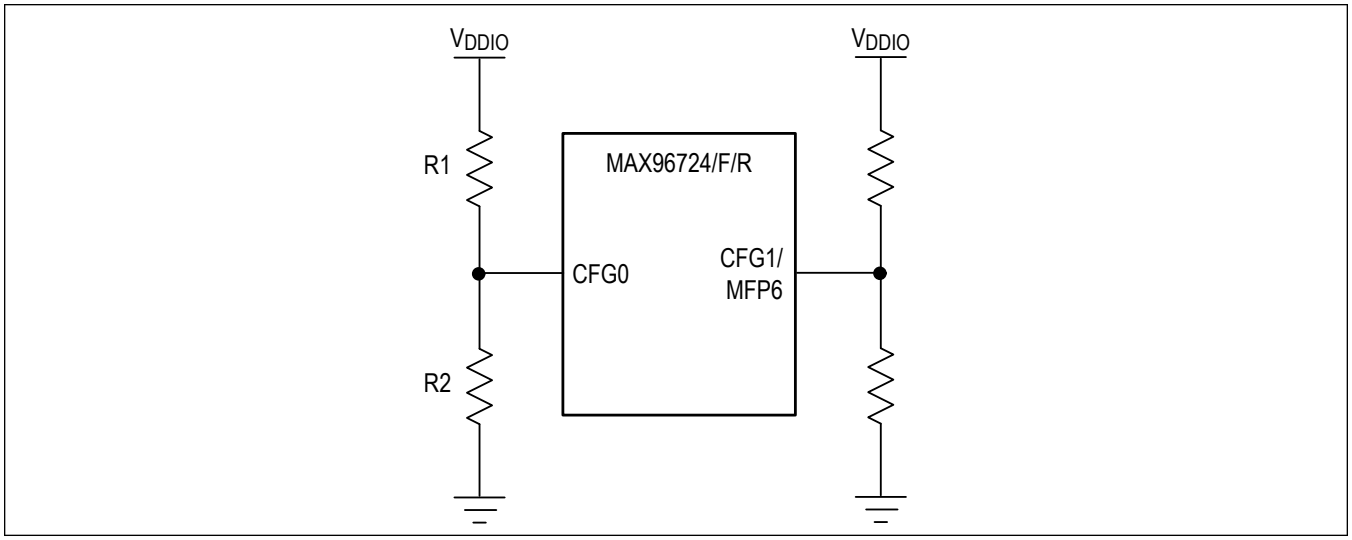


Figure 21. Configuration Pin Connection

The voltage level at each pin is set by an external precision resistor divider connected between V_{DDIO} and ground. Figure 21, Table 7, and Table 8 show the recommended resistor values to select each configuration. The voltage level at the CFG pins is typically latched 11ms after supplies reach the minimum levels required. CFG pins must not be loaded with more than 10pF at power-up to ensure the proper voltage level.

Table 7. CFG0 Input Map

SPECIFICATION (NOTE a) (PERCENTAGE OF V_{DDIO})			SUGGESTED RESISTOR VALUES (NOTES b, c) (1% TOLERANCE)		MAPPED CONFIGURATION		
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	I2CSEL MAX96724/F	I2CSEL MAX96724R	DEVICE ADDRESS
0.0%	0.0%	11.7%	OPEN	10k	I^2C	I^2C	0x4E
16.9%	20.2%	23.6%	80.6k	20.5k			0x5C
28.8%	31.2%	35.5%	68.1k	32.4k			0x9C
40.7%	44.0%	47.4%	56.2k	44.2k			0x9E
All other voltage levels are reserved or not applicable.							

Table 8. CFG1/MFP6 Input Map

CFG1/MFP6 INPUT VOLTAGE (PERCENTAGE of V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (NOTE c)		MAPPED CONFIGURATION (NOTE d)			
MIN	TYP	MAX	R1 (Ω)	R2 (Ω)	CX/ STP	GMSL1/ GMSL2	MAX96724	MAX96724F/R
0.0%	0.0%	11.7%	OPEN	10000	COAX	GMSL2	6Gbps	3Gbps
16.9%	20.2%	23.6%	80600	20500			3Gbps	
28.8%	32.1%	35.5%	68100	32400		GMSL1	HIM Disabled	HIM Disabled
40.7%	44.0%	47.9%	56200	44200	STP	GMSL2	6Gbps	3Gbps
52.6%	56.0%	59.3%	44200	56200			3Gbps	
64.5%	67.9%	71.2%	32400	68100		GMSL1	HIM Enabled	HIM Enabled

Table 8. CFG1/MFP6 Input Map (continued)

CFG1/MFP6 INPUT VOLTAGE (PERCENTAGE of V_{DDIO}) (NOTES a, b)			SUGGESTED RESISTOR VALUES (±1% TOLERANCE) (NOTE c)		MAPPED CONFIGURATION (NOTE d)			
76.4%	79.8%	83.1%	20500	80600			HIM Disabled	HIM Disabled
88.3%	100%	100%	10000	OPEN	COAX	GMSL1	HIM Enabled	HIM Enabled

Notes:

a. CFG0 or CFG1/MFP6 input voltage to exceed the maximum or minimum limits.
b. Until the input voltage is latched, any load on CFG0 or CFG1/MFP6 (other than R1 and R2) must be ≥ 25 x (R1 + R2). Load capacitance (including R1 and R2) must be lumped load ≤ 10pF.
c. Each resistor in the voltage divider must be ≤ 100kΩ.
d. GMSL1 default BWS = 0 (24 bit).

Multifunction Pin Configuration

MAX96724/F/R has several possible MFP states, but only one can be used at a time.

The *Pin Descriptions* section shows default and alternate functions for each MFP, listed in order of priority (highest priority listed first). [[MFP Pin Function Map]] also shows priority, with highest priority on the left. A higher priority function must be disabled when a lower-priority function is enabled, both by register writes.

Table 9. MFP Pin Function Map

PIN	HIGHEST PRIORITY	DECREASING PRIORITY FROM LEFT TO RIGHT					LOWEST PRIORITY	DEFAULT
MFP0	FSYNC				Line Fault 0	GPI0 (GMSL1)	GPIO0	Disabled*
MFP1		VS0/DE0/HS0	CNTL0 (GMSL1)	CNTL2 (GMSL1)	Line Fault 1	GPI1 (GMSL1)	GPIO1	Disabled*
MFP2			CNTL1 (GMSL1)	CNTL3 (GMSL1)	Line Fault 2	GP12 (GMSL1)	GPIO2	Disabled*
MFP3		VS1/DE1/HS1	CNTL4 (GMSL1)		Line Fault 3	GP13 (GMSL1)	GPIO3	Disabled*
MFP4	LOCK						GPIO4	LOCK
MFP5	ERRB	ERRB/LOCK					GPIO5	ERRB
MFP6	CFG1 (Startup Only)	GPIO Aggregation					GPO6	CFG1
MFP7	SDA1	FSYNC (Alternate)	VS2/DE2/ HS2				GPIO7	SDA1
MFP8	SCL1		VS3/DE3/ HS3				GPIO8	SCL1

*Disabled represents a high impedance state where the MFP pin receiver is disabled and the 1MΩ internal pull-down resistor enabled.

Power-Up and Link Start-Up

GMSL2 ICs are in power-down mode when the PWDNB pin is low or when any of the power supplies are disabled. When in power-down mode, the device configuration is reset to the default power-up state.

The serializer and deserializer can power up in any order. After PWDNB is released and all power supplies have settled, each device starts its power-up sequence and performs the following operations:

1. Latch CFG pin states and set internal registers accordingly. See Table 7 and Table 8.
2. Main control channel I2C is functional on local side. Local device registers are writable and readable. Perform local configuration as needed to establish links.
3. Links are established based on default configuration specified by CFG[1:0] pin power-up state, which specifies the global configuration for all links.
4. Perform link calibration, equalizer adaptation, and data channel locking. LOCK pin is driven high when all enabled links are locked and ready. The status of individual links can be monitored by reading individual link lock status bits.
5. Control channel is available from/to the remote side.

Device Reset

There are three general reset options available through register writes:

1. RESET_ALL resets all blocks, including all registers and digital and analog blocks. This bit is auto cleared.
2. Setting RESET_LINK_x resets all GMSL PHY related logic as well as the data pipeline for the specified link (where x is A, B, C, or D). After this bit is set, all local control registers are still accessible. The link remains in RESET until the bit is cleared.
3. Setting RESET_ONESHOT_x resets all GMSL PHY related logic and the data pipeline for the associated link (where x is A, B, C, or D). This bit is auto cleared.

When configuring a GMSL link, program registers that control operation of the desired GMSL link first, then issue a RESET_LINK_x or RESET_ONESHOT_x bits.

Link and Video Lock

GMSL2 Link Lock

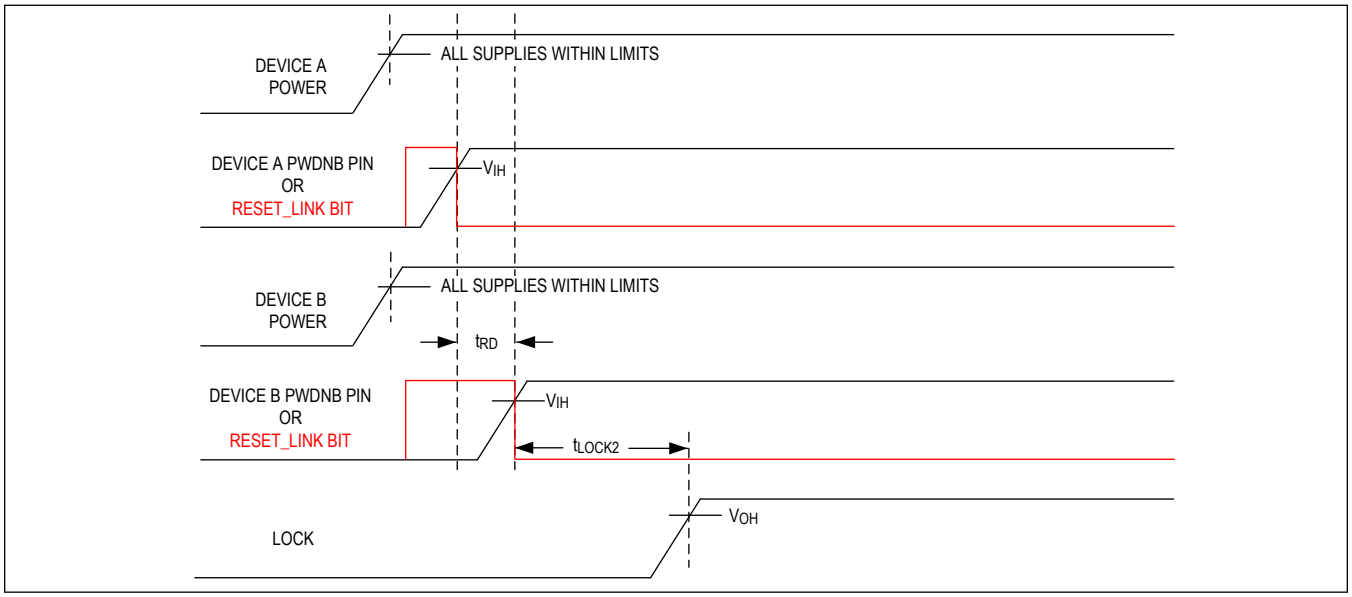


Figure 22. GMSL2 Lock Time

Figure 22 illustrates the sequence that is used to characterize GMSL2 link lock time. Device A is the first device (serializer or deserializer) to power-up or resume operation from a RESET_LINK state. Device B is the device (deserializer or serializer) at the other end of the GMSL link.

Link lock indicates that the data receive paths are locked (forward channel in the deserializer, reverse channel in the serializer). Video and control channel functions (I2C, GPIO) can be used immediately after link lock is asserted.

The device will establish single link GMSL2 connectivity and link lock automatically following power-up. This is an indication that the cable is plugged in and the system is up and running. Lock is obtained with no interaction between

the µC and GMSL devices. Both serializers and deserializers have an open-drain LOCK output pin and a related status register.

The GMSL2 link uses the crystal as the reference clock for GMSL2 links, so a valid video input (PCLK) is not needed for the GMSL2 link to lock.

Notes:

1. The lock sequence is initiated by the release of the PWDNB pin or the RESET_LINK bit in either the serializer or the deserializer.
2. Lock time is measured from the later of PWDNB or RESET_LINK release in either the serializer or deserializer to LOCK being asserted.
3. The PWDNB/RESET_LINK states on the two sides of the link must have overlap when both devices are in PWDNB/RESET_LINK mode prior to the lock process starting.
4. If RESET_LINK is used to initiate lock, PWDNB is assumed to be high after power-up (normal operation).
5. If PWDNB is used to initiate the lock, RESET_LINK is assumed to be low after power-up (normal operation).
6. To achieve the specified lock time, time delay t_{RD} (delay between release of the PWDNB/RESET_LINK on the two devices) must be less than the threshold specified in *Note 9*. Contact the factory for guidance if this timing cannot be guaranteed.
7. Lock time and maximum allowed t_{RD} vary between different families of GMSL devices. They depend on the characteristics of both the serializer and the deserializer. The typical lock time of a specific link can be best estimated as the longer of the lock times specified in each device data sheet. Similarly, the maximum permissible t_{RD} for a specific link can be estimated as the smaller of the values specified in each device data sheet. For further guidance, contact the factory.
8. If there is an instantaneous interruption to link lock, a period of 100ms following loss of lock should be provided to enable the link to automatically recover prior to any ECU initiated resets being issued. This will minimize any disruptions caused by a transient loss in connectivity.

Video Lock

Video lock indicates that the deserializer is receiving valid video data. After the GMSL2 link is locked, the deserializer video output PLL starts its locking sequence. The deserializer normally starts outputting video data several milliseconds after it asserts line lock, provided that it is receiving video packets from the serializer. Video lock status is typically read from a register.

Spread-Spectrum Clocking

MAX96724/F/R can accept forward channel 6/3Gbps spread spectrum which can be used to mitigate electromagnetic interference emitted from the device. Narrow frequency peaks are reduced by modulating the internal 6GHz clock at a rate of 25kHz with a saw-tooth profile. To enable this functionality, refer to the GMSL2 User Guide and contact the factory. Registers are not visible to customers for this feature.

Error and Fault Condition Monitoring

The MAX96724/F/R includes an open-drain, multipurpose error reporting, and interrupt status output. The active-low ERRB pin is driven by the logical OR of a wide variety of error and event status indicators. Errors can be automatically forwarded across the link from the serializer so certain serializer side errors, such as CSI-2 input CRC errors, can automatically be flagged by the MAX96724/F/R's LOCK output. The ability of each error condition to drive ERRB is maskable by register settings. Each error and event that can drive ERRB has a status flag within a sub-block of registers, so the reason for assertion of ERRB can be determined by reading the register status.

GPIO Aggregation

MFP6 has the ability to aggregate the error signals from the serializer, image sensor, and other peripherals connected to the same quad deserializer. Aggregation allows for a single pin on the quad deserializer to be the error-reporting mechanism for everything connected upstream. This reduces the number of connections between deserializer MFPs and SoC inputs.

More information on this feature can be found in the MAX96724/F/R User Guide.

EMB8 — ERRB Forwarding

MAX96724/F has the ability to capture any ERRB information and forward this information to an EMB8 packet on the MIPI data. The EMB8 packet can be inserted at the start of frame/end of frame. More information on this feature can be found in the MAX96724/F/R User Guide.

Functional Safety Features

The MAX96724/F integrates a number of safety features. For more information on these safety features, contact the factory for the MAX96724/F Safety Items and Implementation Guide.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	SPEED
MAX96724GTN/VY+	-40°C to +105°C	56 TQFN-SW-EP	6Gbps
MAX96724GTN/VY+T	-40°C to +105°C	56 TQFN-SW-EP	6Gbps
MAX96724FGTN/V+	-40°C to +105°C	56 TQFN-EP	3Gbps
MAX96724FGTN/V+T	-40°C to +105°C	56 TQFN-EP	3Gbps
MAX96724FGTN/VY+	-40°C to +105°C	56 TQFN-SW-EP	3Gbps
MAX96724FGTN/VY+T	-40°C to +105°C	56 TQFN-SW-EP	3Gbps
MAX96724RGTN/V+	-40°C to +105°C	56 TQFN-EP	3Gbps
MAX96724RGTN/V+T	-40°C to +105°C	56 TQFN-EP	3Gbps

/V Denotes an Automotive Qualified Product.

Y Denotes Wettable Flank.

+ Denotes a lead(Pb)-free/RoHS-compliant Package.

T Denotes tape-and-reel.

EP Denotes Exposed Pad.

Register Map

MAX96724/F/R

ADDRESS	RESET	NAME	MSB							LSB
DEV										
0x00	0x4E	REG0[7:0]	DEV_ADDR[6:0]							CFG_BLOCK
0x01	0xC0	REG1[7:0]	RSVD[1:0]		DIS_LOC_CC[1:0]		–	–	–	–
0x03	0xAA	REG3[7:0]	DIS_REM_CC_D[1:0]		DIS_REM_CC_C[1:0]		DIS_REM_CC_B[1:0]		DIS_REM_CC_A[1:0]	
0x04	0x0F	REG4[7:0]	–	–	–	–	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
0x05	0xC0	REG5[7:0]	LOCK_EN	ERRB_EN	LOCK_CFG	ERRB_LOCK_OEN	ERRB_MST_RST	–	–	RSVD
0x06	0xFF	REG6[7:0]	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
0x07	0x00	REG7[7:0]	CC_CROSSOVER_SEL[3:0]				RSVD[3:0]			
0x0A	0x00	CTRL12[7:0]	RSVD	RSVD	–	–	LOCKED_B	–	–	–
0x0B	0x00	CTRL13[7:0]	RSVD	RSVD	–	–	LOCKED_C	–	–	–
0x0C	0x00	CTRL14[7:0]	RSVD	RSVD	–	–	LOCKED_D	–	–	–
0x0D	0xA2	REG13[7:0]	DEV_ID[7:0]							
0x10	0x22	REG26[7:0]	TX_RATE_PHYB[1:0]		RX_RATE_PHYB[1:0]		TX_RATE_PHYA[1:0]		RX_RATE_PHYA[1:0]	
0x11	0x22	REG27[7:0]	TX_RATE_PHYD[1:0]		RX_RATE_PHYD[1:0]		TX_RATE_PHYC[1:0]		RX_RATE_PHYC[1:0]	
TOP_CTRL										
0x12	0x00	PWR0[7:0]	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
0x13	0x00	PWR1[7:0]	RSVD	RESET_ALL	RSVD[5:0]					
0x18	0x00	CTRL1[7:0]	RESET_LINK_D	RESET_LINK_C	RESET_LINK_B	RESET_LINK_A	RESET_ONESHOT_D	RESET_ONESHOT_C	RESET_ONESHOT_B	RESET_ONESHOT_A
0x1A	0x10	CTRL3[7:0]	RSVD	RSVD	RSVD[1:0]		LOCKED_A	ERROR	CMU_LOCKED	LOCK_PIN
0x22	0xFF	CTRL11[7:0]	RSVD	CXTP_D	RSVD	CXTP_C	RSVD	CXTP_B	RSVD	CXTP_A
0x25	0x0F	INTR2[7:0]	RSVD	RSVD	RSVD	RSVD	DEC_ERR_OEN_D	DEC_ERR_OEN_C	DEC_ERR_OEN_B	DEC_ERR_OEN_A
0x26	0x00	INTR3[7:0]	RSVD	RSVD	RSVD	RSVD	DEC_ERR_FLAG_D	DEC_ERR_FLAG_C	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
0x27	0xF4	INTR4[7:0]	EOM_ERR_OEN_D	EOM_ERR_OEN_C	EOM_ERR_OEN_B	EOM_ERR_OEN_A	RSVD	LFLT_INT_OEN	–	–

ADDRESS	RESET	NAME	MSB							LSB
0x28	0x00	INTR5[7:0]	EOM_ERR_FLAG_D	EOM_ERR_FLAG_C	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	RSVD	LFLT_INT	–	–
0x29	0xFF	INTR6[7:0]	G1_D_ERR_OEN	G1_C_ERR_OEN	G1_B_ERR_OEN	G1_A_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	REM_ERR_OEN	FSYNC_ERR_OEN
0x2A	0x00	INTR7[7:0]	G1_D_ERR_FLAG	G1_C_ERR_FLAG	G1_B_ERR_FLAG	G1_A_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	REM_ERR_FLAG	FSYNC_ERR_FLAG
0x2B	0x00	INTR8[7:0]	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_OEN_D	IDLE_ERR_OEN_C	IDLE_ERR_OEN_B	IDLE_ERR_OEN_A
0x2C	0x00	INTR9[7:0]	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_FLAG_D	IDLE_ERR_FLAG_C	IDLE_ERR_FLAG_B	IDLE_ERR_FLAG_A
0x2D	0x0F	INTR10[7:0]	RT_CNT_OEN_D	RT_CNT_OEN_C	RT_CNT_OEN_B	RT_CNT_OEN_A	MAX_RT_OEN_D	MAX_RT_OEN_C	MAX_RT_OEN_B	MAX_RT_OEN_A
0x2E	0x00	INTR11[7:0]	RT_CNT_FLAG_D	RT_CNT_FLAG_C	RT_CNT_FLAG_B	RT_CNT_FLAG_A	MAX_RT_FLAG_D	MAX_RT_FLAG_C	MAX_RT_FLAG_B	MAX_RT_FLAG_A
0x2F	0x9F	INTR12[7:0]	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
0x30	0xDF	INTR13[7:0]	ERR_RX_EN_A	ERR_RX_RECVED_A	–	ERR_RX_ID_A[4:0]				
0x31	0xDF	INTR14[7:0]	ERR_RX_EN_B	ERR_RX_RECVED_B	–	ERR_RX_ID_B[4:0]				
0x32	0xDF	INTR15[7:0]	ERR_RX_EN_C	ERR_RX_RECVED_C	–	ERR_RX_ID_C[4:0]				
0x33	0xDF	INTR16[7:0]	ERR_RX_EN_D	ERR_RX_RECVED_D	–	ERR_RX_ID_D[4:0]				
0x35	0x00	CNT0[7:0]	DEC_ERR_A[7:0]							
0x36	0x00	CNT1[7:0]	DEC_ERR_B[7:0]							
0x37	0x00	CNT2[7:0]	DEC_ERR_C[7:0]							
0x38	0x00	CNT3[7:0]	DEC_ERR_D[7:0]							
0x39	0x00	CNT4[7:0]	IDLE_ERR_A[7:0]							
0x3A	0x00	CNT5[7:0]	IDLE_ERR_B[7:0]							
0x3B	0x00	CNT6[7:0]	IDLE_ERR_C[7:0]							
0x3C	0x00	CNT7[7:0]	IDLE_ERR_D[7:0]							
0x44	0xFF	VID_PXL_CRC_ERR_VIDEOMASK_OEN[7:0]	VIDEO_MASKED_3_OEN	VIDEO_MASKED_2_OEN	VIDEO_MASKED_1_OEN	VIDEO_MASKED_0_OEN	VID_PXL_CRC_ERR_OEN_D	VID_PXL_CRC_ERR_OEN_C	VID_PXL_CRC_ERR_OEN_B	VID_PXL_CRC_ERR_OEN_A
0x45	0x00	VID_PXL_CRC_VIDEOMASK_INT_FLAG[7:0]	VIDEO_MASKED_3_FLAG	VIDEO_MASKED_2_FLAG	VIDEO_MASKED_1_FLAG	VIDEO_MASKED_0_FLAG	VID_PXL_CRC_ERR_D	VID_PXL_CRC_ERR_C	VID_PXL_CRC_ERR_B	VID_PXL_CRC_ERR_A

ADDRESS	RESET	NAME	MSB							LSB
0x48	0xC1	PWR_STATUS_OEN[7:0]	VDDBAD_INT_OEN	RSVD	–	RSVD	–	–	RSVD[1:0]	
0x49	0x00	PWR_STATUS_OV_FLAG[7:0]	VDDBAD_INT_FLAG	RSVD	RSVD	RSVD	CMP_STATUS_VDD_OV	CMP_STATUS_VDD12_OV	CMP_STATUS_vddio_ov	CMP_STATUS_VDD18_OV
0x4A	0xA7	VDDCMP_MASK[7:0]	VDDCMP_INT_OEN	–	CMP_VTERM_MASK	VDDCMP_MASK[4:0]				
0x4B	0x00	VDDCMP_STATUS_FLAG[7:0]	VDDCMP_INT_FLAG	–	CMP_VTERM_STATUS	–	–	–	–	–
0x4C	0x01	DEV_REV[7:0]	–	–	–	–	DEV_REV[3:0]			
0x4D	0x10	EFUSE_CTRL[7:0]	–	EFUSE_CRC_ERR_RST_OS	EFUSE_CRC_ERR_RST	EFUSE_CRC_ERR_OEN	–	–	–	–
0x4E	0x00	EFUSE_CRC_ERR[7:0]	–	–	–	EFUSE_CRC_ERR	–	–	–	–
CFGH_VIDEO_CRC										
0x60	0x00	CFGH_VIDEO_CRC0[7:0]	RX_CRC_EN_A_B[7:0]							
0x61	0x00	CFGH_VIDEO_CRC1[7:0]	RX_CRC_EN_C_D[7:0]							
CFGI_A INFOFR										
0x70	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
0x71	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x72	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x73	0xFF	TR3[7:0]	RX_SRC_SEL[7:0]							
CFGI_B INFOFR										
0x74	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
0x75	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x76	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x77	0xFF	TR3[7:0]	RX_SRC_SEL_B[7:0]							
CFGI_C INFOFR										
0x78	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
0x79	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x7A	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x7B	0xFF	TR3[7:0]	RX_SRC_SEL_C[7:0]							
CFGI_D INFOFR										
0x7C	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x7D	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x7E	0x00	TR2[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x7F	0xFF	TR3[7:0]	RX_SRC_SEL_D[7:0]							
CFGL_A GPIO										
0xA0	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
0xA1	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0xA3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0xA4	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0xA6	0x72	ARQ1[7:0]	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0xA7	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGL_B GPIO										
0xA8	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
0xA9	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0xAB	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0xAC	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0xAE	0x72	ARQ1[7:0]	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0xAF	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGL_C GPIO										
0xB0	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
0xB1	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0xB3	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0xB4	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0xB6	0x72	ARQ1[7:0]	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0xB7	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGL_D GPIO										
0xB8	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
0xB9	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0xBB	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0xBC	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0xBE	0x72	ARQ1[7:0]	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0xBF	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
CC										
0xC7	0x66	I2C_7[7:0]	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_REGSLV_0_TIMED_OUT	I2C_INTREG_SLV_0_TO[2:0]		
LINE_FAULT										
0xE0	0x00	REG0[7:0]	–	–	–	–	PU_LF3	PU_LF2	PU_LF1	PU_LF0
0xE1	0x22	REG1[7:0]	–	LF_1[2:0]			–	LF_0[2:0]		
0xE2	0x22	REG2[7:0]	–	LF_3[2:0]			–	LF_2[2:0]		
0xE5	0x00	REG5[7:0]	–	–	–	–	LFLT_INT_FLAG[3:0]			
0xE6	0x00	REG6[7:0]	–	–	–	–	MASK_LF3	MASK_LF2	MASK_LF1	MASK_LF0
VIDEO_PIPE_SEL										
0xF0	0x62	VIDEO_PIPE_SEL_0[7:0]	VIDEO_PIPE_SEL_1[3:0]				VIDEO_PIPE_SEL_0[3:0]			
0xF1	0xEA	VIDEO_PIPE_SEL_1[7:0]	VIDEO_PIPE_SEL_3[3:0]				VIDEO_PIPE_SEL_2[3:0]			
0xF4	0x1F	VIDEO_PIPE_EN[7:0]	–	–	–	STREAM_SEL_ALL	VIDEO_PIPE_EN[3:0]			
HVD_GPIO_CTRL										
0xFA	0x00	HVD_GPIO_CTRL_EN[7:0]	–	–	–	–	HVD_OUT_EN[3:0]			
0xFB	0x00	HVD_GPIO_CTRL_HS[7:0]	HVD_HS_SEL3[1:0]		HVD_HS_SEL2[1:0]		HVD_HS_SEL1[1:0]		HVD_HS_SEL0[1:0]	
0xFC	0x00	HVD_GPIO_CTRL_VS[7:0]	HVD_VS_SEL3[1:0]		HVD_VS_SEL2[1:0]		HVD_VS_SEL1[1:0]		HVD_VS_SEL0[1:0]	
0xFD	0x00	HVD_GPIO_CTRL_DE[7:0]	HVD_DE_SEL3[1:0]		HVD_DE_SEL2[1:0]		HVD_DE_SEL1[1:0]		HVD_DE_SEL0[1:0]	
0xFE	0x00	HVD_GPIO_CTRL_SEL[7:0]	HVD_OUT_SEL3[1:0]		HVD_OUT_SEL2[1:0]		HVD_OUT_SEL1[1:0]		HVD_OUT_SEL0[1:0]	
0xFF	0x00	HVD_GPIO_CTRL_ST[7:0]	HVD_ST_SEL3[1:0]		HVD_ST_SEL2[1:0]		HVD_ST_SEL1[1:0]		HVD_ST_SEL0[1:0]	
VID_RX 0										
0x100	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x106	0x12	VIDEO_RX6[7:0]	RSVD[2:0]			VID_SEQ_ERR_OEN	LIM_HEART	–	RSVD	RSVD
0x108	0x02	VIDEO_RX8[7:0]	RSVD	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
VID_RX 1										
0x112	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET

ADDRESS	RESET	NAME	MSB							LSB
0x118	0x12	VIDEO_RX6[7:0]	RSVD[2:0]			VID_SEQ_ERR_OEN	LIM_HEART	–	RSVD	RSVD
0x11A	0x02	VIDEO_RX8[7:0]	RSVD	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
VID_RX 2										
0x124	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x12A	0x12	VIDEO_RX6[7:0]	RSVD[2:0]			VID_SEQ_ERR_OEN	LIM_HEART	–	RSVD	RSVD
0x12C	0x02	VIDEO_RX8[7:0]	RSVD	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
VID_RX 3										
0x136	0x32	VIDEO_RX0[7:0]	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
0x13C	0x12	VIDEO_RX6[7:0]	RSVD[2:0]			VID_SEQ_ERR_OEN	LIM_HEART	–	RSVD	RSVD
0x13E	0x02	VIDEO_RX8[7:0]	RSVD	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
VID_RX_PKT_DET										
0x160	0x0A	LIM_HEART_TIMEOUT_0[7:0]	–	LIM_HEART_TIMEOUT_0[6:0]						
0x161	0x0A	LIM_HEART_TIMEOUT_1[7:0]	–	LIM_HEART_TIMEOUT_1[6:0]						
0x162	0x0A	LIM_HEART_TIMEOUT_2[7:0]	–	LIM_HEART_TIMEOUT_2[6:0]						
0x163	0x0A	LIM_HEART_TIMEOUT_3[7:0]	–	LIM_HEART_TIMEOUT_3[6:0]						
VRX__0 0										
0x1D8	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x1D9	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1DA	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1DB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1DC	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	VPRBS_CHECK	VPRBS_FAIL	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
VRX__0 1										
0x1F8	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x1F9	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x1FA	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x1FB	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x1FC	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	VPRBS_CHECK	VPRBS_FAIL	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
VRX__0 2										
0x218	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x219	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x21A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x21B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x21C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	VPRBS_CHECK	VPRBS_FAIL	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
VRX__0 3										
0x238	0x18	CROSS_HS[7:0]	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
0x239	0x19	CROSS_VS[7:0]	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
0x23A	0x1A	CROSS_DE[7:0]	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
0x23B	0x00	PRBS_ERR[7:0]	VPRBS_ERR[7:0]							
0x23C	0x80	VPRBS[7:0]	PATGEN_CLK_SRC	VPRBS_CHECK	VPRBS_FAIL	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
GPIO_AGGR0										
0x2E0	0x00	POLARITY_A_L[7:0]	POLARITY_A_L[7:0]							
0x2E1	0x00	POLARITY_B_L[7:0]	POLARITY_B_L[7:0]							
0x2E2	0x00	POLARITY_C_L[7:0]	POLARITY_C_L[7:0]							
0x2E3	0x00	POLARITY_D_L[7:0]	POLARITY_D_L[7:0]							
0x2E4	0x00	POLARITY_AB_H[7:0]	–	POLARITY_B_H[2:0]			–	POLARITY_A_H[2:0]		
0x2E5	0x00	POLARITY_CD_H[7:0]	–	POLARITY_D_H[2:0]			–	POLARITY_C_H[2:0]		
0x2E6	0x00	ENABLE_A_L[7:0]	ENABLE_A_L[7:0]							
0x2E7	0x00	ENABLE_B_L[7:0]	ENABLE_B_L[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x2E8	0x00	ENABLE_C_L[7:0]	ENABLE_C_L[7:0]							
0x2E9	0x00	ENABLE_D_L[7:0]	ENABLE_D_L[7:0]							
0x2EA	0x00	ENABLE_AB_H[7:0]	–	ENABLE_B_H[2:0]			–	ENABLE_A_H[2:0]		
0x2EB	0x00	ENABLE_CD_H[7:0]	–	ENABLE_D_H[2:0]			–	ENABLE_C_H[2:0]		
0x2EC	0x00	READ_A_L[7:0]	READ_A_L[7:0]							
0x2ED	0x00	READ_B_L[7:0]	READ_B_L[7:0]							
0x2EE	0x00	READ_C_L[7:0]	READ_C_L[7:0]							
0x2EF	0x00	READ_D_L[7:0]	READ_D_L[7:0]							
0x2F0	0x00	READ_AB_H[7:0]	–	READ_B_H[2:0]			–	READ_A_H[2:0]		
0x2F1	0x00	READ_CD_H[7:0]	–	READ_D_H[2:0]			–	READ_C_H[2:0]		
0x2F2	0x00	OUTPUT[7:0]	–	–	–	–	OUTPUT_INVERT	OUTPUT_ENABLE	DESTINATION	READ_FLAG
GPIO0 0										
0x300	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x301	0xA0	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x302	0x40	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO1 1										
0x303	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x304	0xA1	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x305	0x41	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO2 2										
0x306	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x307	0xA2	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x308	0x42	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO3 3										
0x309	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x30A	0xA3	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x30B	0x43	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO4 4										
0x30C	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x30D	0xA4	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x30E	0x44	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO5 5										
0x310	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x311	0xA5	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x312	0x45	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO6 6										
0x313	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x314	0x26	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x315	0x46	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO7 7										
0x316	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x317	0xA7	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x318	0x47	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO8 8										
0x319	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x31A	0xA8	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x31B	0x48	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO9 9										
0x31C	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
0x31D	0xA9	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x31E	0x49	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO10 10										
0x320	0x81	GPIO_A[7:0]	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS

ADDRESS	RESET	NAME	MSB							LSB
0x321	0xAA	GPIO_B[7:0]	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
0x322	0x4A	GPIO_C[7:0]	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
GPIO0_B 0										
0x337	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x338	0x40	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 1										
0x33A	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x33B	0x41	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 2										
0x33D	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x33E	0x42	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 3										
0x341	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x342	0x43	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 4										
0x344	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x345	0x44	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 5										
0x347	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x348	0x45	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 6										
0x34A	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x34B	0x46	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 7										
0x34D	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x34E	0x47	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 8										
0x351	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x352	0x48	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 9										
0x354	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x355	0x49	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_B 10										
0x357	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
0x358	0x4A	GPIO_C[7:0]	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
GPIO0_C 0										
0x36D	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x36E	0x40	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 1										
0x371	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x372	0x41	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 2										
0x374	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x375	0x42	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 3										
0x377	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x378	0x43	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 4										
0x37A	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x37B	0x44	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 5										
0x37D	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x37E	0x45	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 6										
0x381	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x382	0x46	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 7										
0x384	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x385	0x47	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 8										
0x387	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x388	0x48	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 9										
0x38A	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x38B	0x49	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_C 10										
0x38D	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
0x38E	0x4A	GPIO_C[7:0]	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
GPIO0_D 0										
0x3A4	0x00	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3A5	0x40	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 1										
0x3A7	0x01	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
0x3A8	0x41	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 2										
0x3AA	0x02	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3AB	0x42	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 3										
0x3AD	0x03	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3AE	0x43	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 4										
0x3B1	0x04	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B2	0x44	GPIO_C[7:0]	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 5										
0x3B4	0x05	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B5	0x45	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 6										
0x3B7	0x06	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3B8	0x46	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 7										
0x3BA	0x07	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3BB	0x47	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 8										
0x3BD	0x08	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3BE	0x48	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
GPIO0_D 9										
0x3C1	0x09	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3C2	0x49	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				

ADDRESS	RESET	NAME	MSB							LSB
GPIO0_D 10										
0x3C4	0x0A	GPIO_B[7:0]	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
0x3C5	0x4A	GPIO_C[7:0]	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
BACKTOP										
0x400	0x01	BACKTOP1[7:0]	CSIPLL3_LOCK	CSIPLL2_LOCK	CSIPLL1_LOCK	CSIPLL0_LOCK	RSVD	RSVD	RSVD	RSVD
0x401	0x00	BACKTOP2[7:0]	VS_VC0_L[7:0]							
0x402	0x00	BACKTOP3[7:0]	VS_VC0_H[7:0]							
0x403	0x00	BACKTOP4[7:0]	VS_VC1_L[7:0]							
0x404	0x00	BACKTOP5[7:0]	VS_VC1_H[7:0]							
0x405	0x00	BACKTOP6[7:0]	VS_VC2_L[7:0]							
0x406	0x00	BACKTOP7[7:0]	VS_VC2_H[7:0]							
0x407	0x00	BACKTOP8[7:0]	VS_VC3_L[7:0]							
0x408	0x00	BACKTOP9[7:0]	VS_VC3_H[7:0]							
0x409	0x00	BACKTOP10[7:0]	DE_SEL3	DE_SEL2	DE_SEL1	DE_SEL0	RSVD	RSVD	RSVD	RSVD
0x40A	0x00	BACKTOP11[7:0]	cmd_overflow3	cmd_overflow2	cmd_overflow1	cmd_overflow0	LMO_3	LMO_2	LMO_1	LMO_0
0x40B	0x02	BACKTOP12[7:0]	soft_bpp_0[4:0]					–	CSI_OUT_EN	RSVD
0x40C	0x00	BACKTOP13[7:0]	soft_vc_1[3:0]				soft_vc_0[3:0]			
0x40D	0x00	BACKTOP14[7:0]	soft_vc_3[3:0]				soft_vc_2[3:0]			
0x40E	0x00	BACKTOP15[7:0]	soft_dt_1_h[1:0]		soft_dt_0[5:0]					
0x40F	0x00	BACKTOP16[7:0]	soft_dt_2_h[3:0]				soft_dt_1_l[3:0]			
0x410	0x00	BACKTOP17[7:0]	soft_dt_3[5:0]						soft_dt_2_l[1:0]	
0x411	0x00	BACKTOP18[7:0]	soft_bpp_2_h[2:0]			soft_bpp_1[4:0]				
0x412	0x00	BACKTOP19[7:0]	–	soft_bpp_3[4:0]					soft_bpp_2_l[1:0]	
0x413	0x00	BACKTOP20[7:0]	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x414	0x00	BACKTOP21[7:0]	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x415	0x2F	BACKTOP22[7:0]	override_bpp_vc_dt_1	override_bpp_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
0x416	0x00	BACKTOP23[7:0]	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x417	0x00	BACKTOP24[7:0]	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x418	0x2F	BACKTOP25[7:0]	override_bpp_vc_dt_3	override_bpp_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
0x419	0x00	BACKTOP26[7:0]	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x41A	0x00	BACKTOP27[7:0]	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	yuv_8_10_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x41B	0x2F	BACKTOP28[7:0]	–	–	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
0x41C	0x00	BACKTOP29[7:0]	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
0x41D	0x00	BACKTOP30[7:0]	–	–	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
0x41E	0x2F	BACKTOP31[7:0]	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
0x41F	0x00	BACKTOP32[7:0]	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0
BACKTOP_1										
0x420	0x01	BACKTOP1[7:0]	ERRB_PKT_EN[3:0]				–	–	RSVD[1:0]	
0x421	0x55	BACKTOP2[7:0]	ERRB_PKT_Insert_Mode_4[1:0]		ERRB_PKT_Insert_Mode_3[1:0]		ERRB_PKT_Insert_Mode_2[1:0]		ERRB_PKT_Insert_Mode_1[1:0]	
0x422	0x00	BACKTOP3[7:0]	–	ERRB_PKT_EDGE_SEL_4	–	ERRB_PKT_EDGE_SEL_3	–	ERRB_PKT_EDGE_SEL_2	–	ERRB_PKT_EDGE_SEL_1
0x423	0x12	BACKTOP4[7:0]	ERRB_PKT_DBL_MODE_1	–	ERRB_PKT_DT_1[5:0]					
0x424	0x12	BACKTOP5[7:0]	ERRB_PKT_DBL_MODE_2	–	ERRB_PKT_DT_2[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x425	0x12	BACKTOP6[7:0]	ERRB_PKT_DBL_MODE_3	–	ERRB_PKT_DT_3[5:0]					
0x426	0x12	BACKTOP7[7:0]	ERRB_PKT_DBL_MODE_4	–	ERRB_PKT_DT_4[5:0]					
0x427	0x0F	BACKTOP8[7:0]	ERRB_PKT_VC_OVRD_EN_1	–	–	ERRB_PKT_VC_OVRD_1[4:0]				
0x428	0x0F	BACKTOP9[7:0]	ERRB_PKT_VC_OVRD_EN_2	–	–	ERRB_PKT_VC_OVRD_2[4:0]				
0x429	0x0F	BACKTOP10[7:0]	ERRB_PKT_VC_OVRD_EN_3	–	–	ERRB_PKT_VC_OVRD_3[4:0]				
0x42A	0x0F	BACKTOP11[7:0]	ERRB_PKT_VC_OVRD_EN_4	–	–	ERRB_PKT_VC_OVRD_4[4:0]				
0x42B	0x00	BACKTOP12[7:0]	–	–	–	ERRB_PKT_VC_1[4:0]				
0x42C	0x00	BACKTOP13[7:0]	–	–	–	ERRB_PKT_VC_2[4:0]				
0x42D	0x00	BACKTOP14[7:0]	–	–	–	ERRB_PKT_VC_3[4:0]				
0x42E	0x00	BACKTOP15[7:0]	–	–	–	ERRB_PKT_VC_4[4:0]				
0x435	0x01	BACKTOP22[7:0]	–	–	–	–	n_vs_block[3:0]			
0x436	0x00	BACKTOP23[7:0]	–	–	–	–	dis_vs3	dis_vs2	dis_vs1	dis_vs0
0x437	0x00	BACKTOP24[7:0]	ERRB_PKT_WC_OVRD_EN_4	ERRB_PKT_WC_OVRD_EN_3	ERRB_PKT_WC_OVRD_EN_2	ERRB_PKT_WC_OVRD_EN_1	–	–	–	–
0x438	0x00	BACKTOP25[7:0]	ERRB_PKT_WC_1_H[7:0]							
0x439	0x00	BACKTOP26[7:0]	ERRB_PKT_WC_1_L[7:0]							
0x43A	0x00	BACKTOP27[7:0]	ERRB_PKT_WC_2_H[7:0]							
0x43B	0x00	BACKTOP28[7:0]	ERRB_PKT_WC_2_L[7:0]							
0x43C	0x00	BACKTOP29[7:0]	ERRB_PKT_WC_3_H[7:0]							
0x43D	0x00	BACKTOP30[7:0]	ERRB_PKT_WC_3_L[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x43E	0x00	BACKTOP31[7:0]	ERRB_PKT_WC_4_H[7:0]							
0x43F	0x00	BACKTOP32[7:0]	ERRB_PKT_WC_4_L[7:0]							
0x440	0x00	BACKTOP33[7:0]	–	–	–	–	FIFO_EMPTY_3	FIFO_EMPTY_2	FIFO_EMPTY_1	FIFO_EMPTY_0
0x442	0x80	BACKTOP1_HDR_ERR[7:0]	TUN_HDR_ERR_FLAG_0_OEN	TUN_HDR_ERR_FLAG_0	TUN_HDR_CRC_ERR_3_FLAG_0	TUN_HDR_CRC_ERR_2_FLAG_0	TUN_HDR_CRC_ERR_1_FLAG_0	TUN_HDR_CRC_ERR_0_FLAG_0	TUN_HDR_ECC_ERR_FLAG_0	TUN_HDR_ECC_FLAG_0
0x443	0x80	BACKTOP2_HDR_ERR[7:0]	TUN_HDR_ERR_FLAG_1_OEN	TUN_HDR_ERR_FLAG_1	TUN_HDR_CRC_ERR_3_FLAG_1	TUN_HDR_CRC_ERR_2_FLAG_1	TUN_HDR_CRC_ERR_1_FLAG_1	TUN_HDR_CRC_ERR_0_FLAG_1	TUN_HDR_ECC_ERR_FLAG_1	TUN_HDR_ECC_FLAG_1
0x444	0x80	BACKTOP3_HDR_ERR[7:0]	TUN_HDR_ERR_FLAG_2_OEN	TUN_HDR_ERR_FLAG_2	TUN_HDR_CRC_ERR_3_FLAG_2	TUN_HDR_CRC_ERR_2_FLAG_2	TUN_HDR_CRC_ERR_1_FLAG_2	TUN_HDR_CRC_ERR_0_FLAG_2	TUN_HDR_ECC_ERR_FLAG_2	TUN_HDR_ECC_FLAG_2
0x445	0x80	BACKTOP4_HDR_ERR[7:0]	TUN_HDR_ERR_FLAG_3_OEN	TUN_HDR_ERR_FLAG_3	TUN_HDR_CRC_ERR_3_FLAG_3	TUN_HDR_CRC_ERR_2_FLAG_3	TUN_HDR_CRC_ERR_1_FLAG_3	TUN_HDR_CRC_ERR_0_FLAG_3	TUN_HDR_ECC_ERR_FLAG_3	TUN_HDR_ECC_FLAG_3
0x446	0xF0	BACKTOP39[7:0]	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP2_LINE_LEN_OVRD	BKTP1_LINE_LEN_OVRD	BKTP0_LINE_LEN_OVRD
0x447	0x07	BACKTOP40[7:0]	BKTP0_LINE_LEN_H[7:0]							
0x448	0x53	BACKTOP41[7:0]	BKTP0_LINE_LEN_L[7:0]							
0x449	0x07	BACKTOP42[7:0]	BKTP1_LINE_LEN_H[7:0]							
0x44A	0x53	BACKTOP43[7:0]	BKTP1_LINE_LEN_L[7:0]							
0x44B	0x07	BACKTOP44[7:0]	BKTP2_LINE_LEN_H[7:0]							
0x44C	0x53	BACKTOP45[7:0]	BKTP2_LINE_LEN_L[7:0]							
0x44D	0x07	BACKTOP46[7:0]	BKTP3_LINE_LEN_H[7:0]							
0x44E	0x53	BACKTOP47[7:0]	BKTP3_LINE_LEN_L[7:0]							
0x44F	0xFF	BACKTOP48[7:0]	BKTP4_VM_TIMEOUT_DIV[1:0]		BKTP3_VM_TIMEOUT_DIV[1:0]		BKTP2_VM_TIMEOUT_DIV[1:0]		BKTP1_VM_TIMEOUT_DIV[1:0]	
0x450	0x00	BACKTOP_EMBED0[7:0]	EMBED_LL_EN_BKTP0	–	EMBED_LL_NUM_BKTP0[1:0]		EMBED_FL_EN_BKTP0	–	EMBED_FL_NUM_BKTP0[1:0]	
0x451	0x00	BACKTOP_EMBED1[7:0]	EMBED_LL_EN_BKTP1	–	EMBED_LL_NUM_BKTP1[1:0]		EMBED_FL_EN_BKTP1	–	EMBED_FL_NUM_BKTP1[1:0]	
0x452	0x00	BACKTOP_EMBED2[7:0]	EMBED_LL_EN_BKTP2	–	EMBED_LL_NUM_BKTP2[1:0]		EMBED_FL_EN_BKTP2	–	EMBED_FL_NUM_BKTP2[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x453	0x00	BACKTOP_EMBED3[7:0]	EMBED_LL_EN_BKTP3	–	EMBED_LL_NUM_BKTP3[1:0]		EMBED_FL_EN_BKTP3	–	EMBED_FL_NUM_BKTP3[1:0]	
0x454	0xFF	CMD_LMO_ERRB_EN[7:0]	CMD_OVFL_3_ERRB_OEN	CMD_OVFL_2_ERRB_OEN	CMD_OVFL_1_ERRB_OEN	CMD_OVFL_0_ERRB_OEN	LMO_3_ERRB_OEN	LMO_2_ERRB_OEN	LMO_1_ERRB_OEN	LMO_0_ERRB_OEN
0x455	0x0F	DPLL_ERRB_OEN[7:0]	CSIPLL3_LOL_STICKY_FLAG	CSIPLL2_LOL_STICKY_FLAG	CSIPLL1_LOL_STICKY_FLAG	CSIPLL0_LOL_STICKY_FLAG	CSI_DPLL3_ERRB_OEN	CSI_DPLL2_ERRB_OEN	CSI_DPLL1_ERRB_OEN	CSI_DPLL0_ERRB_OEN
0x456	0x00	BACKTOP_OVERRIDE_BPP_DT[7:0]	OVERRIDE_VC_3	OVERRIDE_VC_2	OVERRIDE_VC_1	OVERRIDE_VC_0	OVERRIDE_BPP_DT_3	OVERRIDE_BPP_DT_2	OVERRIDE_BPP_DT_1	OVERRIDE_BPP_DT_0
0x457	0x00	BACKTOP_OVERRIDE_VC[7:0]	–	–	–	–	–	–	–	OVERRIDE_VC_BITS_2_AND_3
0x458	0xF0	SRAM_LCRC_ERR[7:0]	SRAM_LCRC_ERR_OEN_3	SRAM_LCRC_ERR_OEN_2	SRAM_LCRC_ERR_OEN_1	SRAM_LCRC_ERR_OEN_0	SRAM_LCRC_ERR_3	SRAM_LCRC_ERR_2	SRAM_LCRC_ERR_1	SRAM_LCRC_ERR_0
0x459	0x00	SRAM_LCRC_EN[7:0]	SRAM_LCRC_TUN_CHK_DIS_3	SRAM_LCRC_TUN_CHK_DIS_2	SRAM_LCRC_TUN_CHK_DIS_1	SRAM_LCRC_TUN_CHK_DIS_0	SRAM_LCRC_PIXEL_CHK_DIS_3	SRAM_LCRC_PIXEL_CHK_DIS_2	SRAM_LCRC_PIXEL_CHK_DIS_1	SRAM_LCRC_PIXEL_CHK_DIS_0
0x45A	0x00	SRAM_LCRC_RESET[7:0]	INIT_SRAM_LCRC_ERR_DIS_3	INIT_SRAM_LCRC_ERR_DIS_2	INIT_SRAM_LCRC_ERR_DIS_1	INIT_SRAM_LCRC_ERR_DIS_0	SRAM_LCRC_MATCH_RESET_3	SRAM_LCRC_MATCH_RESET_2	SRAM_LCRC_MATCH_RESET_1	SRAM_LCRC_MATCH_RESET_0
ERR_INJ										
0x480	0x00	BKTOP_ERR_INJ_1[7:0]	–	–	–	–	SRAM_LCRC_ERR_INJ_DIS_3	SRAM_LCRC_ERR_INJ_DIS_2	SRAM_LCRC_ERR_INJ_DIS_1	SRAM_LCRC_ERR_INJ_DIS_0
0x481	0x00	MEM_ERR_INJ_1BIT[7:0]	–	–	–	–	MEM_ERR_INJ_1BIT_BKTP4	MEM_ERR_INJ_1BIT_BKTP3	MEM_ERR_INJ_1BIT_BKTP2	MEM_ERR_INJ_1BIT_BKTP1
0x482	0x00	MEM_ERR_INJ_2BIT[7:0]	–	–	–	–	MEM_ERR_INJ_2BIT_BKTP4	MEM_ERR_INJ_2BIT_BKTP3	MEM_ERR_INJ_2BIT_BKTP2	MEM_ERR_INJ_2BIT_BKTP1
0x483	0x01	MEM_ERR_INJ_WORD_LOC_EN[7:0]	–	–	–	–	–	–	MEM_ERR_INJ_WORD_LOC_2_EN	MEM_ERR_INJ_WORD_LOC_1_EN
0x484	0x00	MEM_ERR_INJ_WORD_LOC_1[7:0]	MEM_ERR_INJ_WORD_LOC_1[7:0]							
0x485	0x00	MEM_ERR_INJ_WORD_LOC_2[7:0]	MEM_ERR_INJ_WORD_LOC_2[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x486	0x00	MEM_ERR_INJ_PKT_NUM[7:0]	–	–	–	–	MEM_ERR_INJ_PKT_NUM[3:0]			
0x487	0x03	MEM_ERR_INJ_BIT1_LOC[7:0]	–	–	–	MEM_ERR_INJ_BIT1_LOC[4:0]				
0x488	0x00	MEM_ERR_INJ_BIT2_LOC[7:0]	–	–	–	MEM_ERR_INJ_BIT2_LOC[4:0]				
FSYNC										
0x4A0	0x0C	FSYNC_0[7:0]	RSVD	RSVD	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
0x4A1	0x00	FSYNC_1[7:0]	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
0x4A2	0x81	FSYNC_2[7:0]	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
0x4A3	0x00	FSYNC_3[7:0]	P_VAL_L[7:0]							
0x4A4	0x00	FSYNC_4[7:0]	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
0x4A5	0x00	FSYNC_5[7:0]	FSYNC_PERIOD_L[7:0]							
0x4A6	0x00	FSYNC_6[7:0]	FSYNC_PERIOD_M[7:0]							
0x4A7	0x00	FSYNC_7[7:0]	FSYNC_PERIOD_H[7:0]							
0x4A8	0x00	FSYNC_8[7:0]	FRM_DIFF_ERR_THR_L[7:0]							
0x4A9	0x0F	FSYNC_9[7:0]	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
0x4AA	0x00	FSYNC_10[7:0]	OVLP_WINDOW_L[7:0]							
0x4AB	0x00	FSYNC_11[7:0]	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
0x4AF	0xCF	FSYNC_15[7:0]	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0
0x4B0	0x00	FSYNC_16[7:0]	FSYNC_ERR_CNT[7:0]							
0x4B1	0xF0	FSYNC_17[7:0]	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
0x4B2	0x00	FSYNC_18[7:0]	CALC_FRM_LEN_L[7:0]							
0x4B3	0x00	FSYNC_19[7:0]	CALC_FRM_LEN_M[7:0]							
0x4B4	0x00	FSYNC_20[7:0]	CALC_FRM_LEN_H[7:0]							
0x4B5	0x00	FSYNC_21[7:0]	FRM_DIFF_L[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x4B6	0x00	FSYNC_22[7:0]	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
0x4B7	0x00	FSYNC_23[7:0]	RSVD	RSVD	FSYNC_RST_MODE	–	RSVD	RSVD	RSVD	RSVD
CFGC_A CC_0										
0x500	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x501	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x503	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x504	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x506	0x72	ARQ1[7:0]	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0x507	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC_B CC_0										
0x510	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x511	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x513	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x514	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x516	0x72	ARQ1[7:0]	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0x517	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGC_C CC_0										
0x520	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
0x521	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x523	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x524	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x526	0x72	ARQ1[7:0]	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0x527	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGC_D CC_0										
0x530	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
0x531	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x533	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x534	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0x536	0x72	ARQ1[7:0]	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D

ADDRESS	RESET	NAME	MSB							LSB
0x537	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						
CFGC_A CC_1										
0x560	0xF0	TR0[7:0]	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
0x561	0xB0	TR1[7:0]	BW_MULT[1:0]		BW_VAL[5:0]					
0x563	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID[2:0]		
0x564	0xFF	TR4[7:0]	RX_SRC_SEL[7:0]							
0x566	0x72	ARQ1[7:0]	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
0x567	0x00	ARQ2[7:0]	MAX_RT_ERR	RT_CNT[6:0]						
CFGC_B CC_1										
0x570	0xF0	TR0[7:0]	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
0x571	0xB0	TR1[7:0]	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
0x573	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_B[2:0]		
0x574	0xFF	TR4[7:0]	RX_SRC_SEL_B[7:0]							
0x576	0x72	ARQ1[7:0]	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
0x577	0x00	ARQ2[7:0]	MAX_RT_ERR_B	RT_CNT_B[6:0]						
CFGC_C CC_1										
0x580	0xF0	TR0[7:0]	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
0x581	0xB0	TR1[7:0]	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
0x583	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_C[2:0]		
0x584	0xFF	TR4[7:0]	RX_SRC_SEL_C[7:0]							
0x586	0x72	ARQ1[7:0]	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
0x587	0x00	ARQ2[7:0]	MAX_RT_ERR_C	RT_CNT_C[6:0]						
CFGC_D CC_1										
0x590	0xF0	TR0[7:0]	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
0x591	0xB0	TR1[7:0]	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
0x593	0x00	TR3[7:0]	–	–	–	–	–	TX_SRC_ID_D[2:0]		
0x594	0xFF	TR4[7:0]	RX_SRC_SEL_D[7:0]							
0x596	0x72	ARQ1[7:0]	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
0x597	0x00	ARQ2[7:0]	MAX_RT_ERR_D	RT_CNT_D[6:0]						

ADDRESS	RESET	NAME	MSB							LSB
CC_G2P0_A										
0x640	0x26	I2C_0[7:0]	–	RSVD	SLV_SH_P0_A[1:0]		–	SLV_TO_P0_A[2:0]		
0x641	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_A[2:0]			–	MST_TO_P0_A[2:0]		
0x642	0x00	I2C_2[7:0]	SRC_A_P0_A[6:0]							–
0x643	0x00	I2C_3[7:0]	DST_A_P0_A[6:0]							–
0x644	0x00	I2C_4[7:0]	SRC_B_P0_A[6:0]							–
0x645	0x00	I2C_5[7:0]	DST_B_P0_A[6:0]							–
CC_G2P0_B										
0x650	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_B[1:0]		–	SLV_TO_P0_B[2:0]		
0x651	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_B[2:0]			–	MST_TO_P0_B[2:0]		
0x652	0x00	I2C_2[7:0]	SRC_A_P0_B[6:0]							–
0x653	0x00	I2C_3[7:0]	DST_A_P0_B[6:0]							–
0x654	0x00	I2C_4[7:0]	SRC_B_P0_B[6:0]							–
0x655	0x00	I2C_5[7:0]	DST_B_P0_B[6:0]							–
CC_G2P0_C										
0x660	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_C[1:0]		–	SLV_TO_P0_C[2:0]		
0x661	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_C[2:0]			–	MST_TO_P0_C[2:0]		
0x662	0x00	I2C_2[7:0]	SRC_A_P0_C[6:0]							–
0x663	0x00	I2C_3[7:0]	DST_A_P0_C[6:0]							–
0x664	0x00	I2C_4[7:0]	SRC_B_P0_C[6:0]							–
0x665	0x00	I2C_5[7:0]	DST_B_P0_C[6:0]							–
CC_G2P0_D										
0x670	0x26	I2C_0[7:0]	–	–	SLV_SH_P0_D[1:0]		–	SLV_TO_P0_D[2:0]		
0x671	0x56	I2C_1[7:0]	RSVD	MST_BT_P0_D[2:0]			–	MST_TO_P0_D[2:0]		
0x672	0x00	I2C_2[7:0]	SRC_A_P0_D[6:0]							–
0x673	0x00	I2C_3[7:0]	DST_A_P0_D[6:0]							–
0x674	0x00	I2C_4[7:0]	SRC_B_P0_D[6:0]							–
0x675	0x00	I2C_5[7:0]	DST_B_P0_D[6:0]							–
CC_G2P1_A										
0x680	0x26	I2C_0[7:0]	–	I2C_HS M_P1	SLV_SH_P1_A[1:0]		–	SLV_TO_P1_A[2:0]		
0x681	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_A[2:0]			–	MST_TO_P1_A[2:0]		
0x682	0x00	I2C_2[7:0]	SRC_A_P1_A[6:0]							–
0x683	0x00	I2C_3[7:0]	DST_A_P1_A[6:0]							–
0x684	0x00	I2C_4[7:0]	SRC_B_P1_A[6:0]							–
0x685	0x00	I2C_5[7:0]	DST_B_P1_A[6:0]							–
CC_G2P1_B										
0x690	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_B[1:0]		–	SLV_TO_P1_B[2:0]		
0x691	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_B[2:0]			–	MST_TO_P1_B[2:0]		
0x692	0x00	I2C_2[7:0]	SRC_A_P1_B[6:0]							–
0x693	0x00	I2C_3[7:0]	DST_A_P1_B[6:0]							–
0x694	0x00	I2C_4[7:0]	SRC_B_P1_B[6:0]							–
0x695	0x00	I2C_5[7:0]	DST_B_P1_B[6:0]							–

ADDRESS	RESET	NAME	MSB							LSB
CC_G2P1_C										
0x6A0	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_C[1:0]		–	SLV_TO_P1_C[2:0]		
0x6A1	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_C[2:0]			–	MST_TO_P1_C[2:0]		
0x6A2	0x00	I2C_2[7:0]	SRC_A_P1_C[6:0]							–
0x6A3	0x00	I2C_3[7:0]	DST_A_P1_C[6:0]							–
0x6A4	0x00	I2C_4[7:0]	SRC_B_P1_C[6:0]							–
0x6A5	0x00	I2C_5[7:0]	DST_B_P1_C[6:0]							–
CC_G2P1_D										
0x6B0	0x26	I2C_0[7:0]	–	–	SLV_SH_P1_D[1:0]		–	SLV_TO_P1_D[2:0]		
0x6B1	0x56	I2C_1[7:0]	RSVD	MST_BT_P1_D[2:0]			–	MST_TO_P1_D[2:0]		
0x6B2	0x00	I2C_2[7:0]	SRC_A_P1_D[6:0]							–
0x6B3	0x00	I2C_3[7:0]	DST_A_P1_D[6:0]							–
0x6B4	0x00	I2C_4[7:0]	SRC_B_P1_D[6:0]							–
0x6B5	0x00	I2C_5[7:0]	DST_B_P1_D[6:0]							–
PROFILE_CTRL										
0x6E1	0x00	PROFILE_MIPI_SEL[7:0]	–	–	PROFILE_MIPI_SEL[5:0]					
0x6EA	0x00	PROFILE_GMSL_1_0[7:0]	–	PROFILE_GMSL_1[2:0]			–	PROFILE_GMSL_0[2:0]		
0x6EB	0x00	PROFILE_GMSL_3_2[7:0]	–	PROFILE_GMSL_3[2:0]			–	PROFILE_GMSL_2[2:0]		
MIPI_TX_EXT 0										
0x800	0x00	MIPI_TX_EXT0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x801	0x00	MIPI_TX_EXT1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x802	0x00	MIPI_TX_EXT2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x803	0x00	MIPI_TX_EXT3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x804	0x00	MIPI_TX_EXT4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x805	0x00	MIPI_TX_EXT5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x806	0x00	MIPI_TX_EXT6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x807	0x00	MIPI_TX_EXT7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x808	0x00	MIPI_TX_EXT8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x809	0x00	MIPI_TX_EXT9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x80A	0x00	MIPI_TX_EXT10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x80B	0x00	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–

ADDRESS	RESET	NAME	MSB							LSB
0x80C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x80D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x80E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x80F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 1										
0x810	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x811	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x812	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x813	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x814	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x815	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x816	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x817	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x818	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x819	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x81A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x81B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x81C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x81D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x81E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x81F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 2										
0x820	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x821	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x822	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–

ADDRESS	RESET	NAME	MSB							LSB
0x823	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x824	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x825	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x826	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x827	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x828	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x829	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x82A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
0x82B	0x00	MIPI_TX_EXT 11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x82C	0x00	MIPI_TX_EXT 12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x82D	0x00	MIPI_TX_EXT 13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x82E	0x00	MIPI_TX_EXT 14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x82F	0x00	MIPI_TX_EXT 15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_TX_EXT 3										
0x830	0x00	MIPI_TX_EXT 0[7:0]	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
0x831	0x00	MIPI_TX_EXT 1[7:0]	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
0x832	0x00	MIPI_TX_EXT 2[7:0]	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
0x833	0x00	MIPI_TX_EXT 3[7:0]	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
0x834	0x00	MIPI_TX_EXT 4[7:0]	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
0x835	0x00	MIPI_TX_EXT 5[7:0]	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
0x836	0x00	MIPI_TX_EXT 6[7:0]	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
0x837	0x00	MIPI_TX_EXT 7[7:0]	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
0x838	0x00	MIPI_TX_EXT 8[7:0]	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
0x839	0x00	MIPI_TX_EXT 9[7:0]	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
0x83A	0x00	MIPI_TX_EXT 10[7:0]	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–

ADDRESS	RESET	NAME	MSB							LSB
0x83B	0x00	MIPI_TX_EXT11[7:0]	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
0x83C	0x00	MIPI_TX_EXT12[7:0]	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
0x83D	0x00	MIPI_TX_EXT13[7:0]	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
0x83E	0x00	MIPI_TX_EXT14[7:0]	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
0x83F	0x00	MIPI_TX_EXT15[7:0]	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
MIPI_PHY										
0x8A0	0x04	MIPI_PHY0[7:0]	force_csi_out_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	RSVD	phy_4x2
0x8A1	0x00	MIPI_PHY1[7:0]	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
0x8A2	0xF4	MIPI_PHY2[7:0]	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
0x8A3	0xE4	MIPI_PHY3[7:0]	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
0x8A4	0xE4	MIPI_PHY4[7:0]	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
0x8A5	0x00	MIPI_PHY5[7:0]	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
0x8A6	0x00	MIPI_PHY6[7:0]	–	–	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
0x8A8	0x00	MIPI_PHY8[7:0]	t_lpxesc[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
0x8A9	0x00	MIPI_PHY9[7:0]	phy_cp0[4:0]					–	RSVD	RSVD
0x8AA	0x02	MIPI_PHY10[7:0]	phy_cp1[4:0]					–	RSVD	RSVD
0x8AB	0x00	MIPI_PHY11[7:0]	phy_cp_err[3:0]				–	–	RSVD	–
0x8AD	0x1F	MIPI_PHY13[7:0]	–	–	t_t3_prebegin[5:0]					
0x8AE	0x5D	MIPI_PHY14[7:0]	–	t_t3_post[4:0]					t_t3_prep[1:0]	
0x8B0	0x78	MIPI_PHY16[7:0]	–	TUN_CONV_DATA_CRC_ERR_OEN	TUN_DATA_CRC_ERR_OEN	TUN_EC_UNCORR_ERR_OEN	TUN_EC_CORR_ERR_OEN	–	–	–
0x8B1	0x00	MIPI_PHY17[7:0]	–	TUN_CONV_DATA_CRC_ERR	TUN_DATA_CRC_ERR	TUN_EC_UNCORR_ERR	TUN_EC_CORR_ERR	–	–	–
0x8B2	0x00	MIPI_PHY18[7:0]	csipll3_PLLORangeH	csipll3_PLLORangeL	csipll2_PLLORangeH	csipll2_PLLORangeL	csipll1_PLLORangeH	csipll1_PLLORangeL	csipll0_PLLORangeH	csipll0_PLLORangeL

ADDRESS	RESET	NAME	MSB							LSB
0x8B3	0x00	MIPI_PHY19[7:0]	csipll3_PLLORangeH_flag	csipll3_PLLORangeL_flag	csipll2_PLLORangeH_flag	csipll2_PLLORangeL_flag	csipll1_PLLORangeH_flag	csipll1_PLLORangeL_flag	csipll0_PLLORangeH_flag	csipll0_PLLORangeL_flag
0x8B4	0xFF	MIPI_PHY20[7:0]	csipll3_PLLORangeH_oen	csipll3_PLLORangeL_oen	csipll2_PLLORangeH_oen	csipll2_PLLORangeL_oen	csipll1_PLLORangeH_oen	csipll1_PLLORangeL_oen	csipll0_PLLORangeH_oen	csipll0_PLLORangeL_oen
0x8C0	0x00	MIPI_PRBS_0[7:0]	MIPI_PRBS_EN_P1_LN1[1:0]		MIPI_PRBS_EN_P1_LN0[1:0]		MIPI_PRBS_EN_P0_LN1[1:0]		MIPI_PRBS_EN_P0_LN0[1:0]	
0x8C1	0x00	MIPI_PRBS_1[7:0]	MIPI_PRBS_EN_P3_LN1[1:0]		MIPI_PRBS_EN_P3_LN0[1:0]		MIPI_PRBS_EN_P2_LN1[1:0]		MIPI_PRBS_EN_P2_LN0[1:0]	
0x8C2	0x00	MIPI_PRBS_2[7:0]	MIPI_CUST_SEED_EN_P3_LN1	MIPI_CUST_SEED_EN_P3_LN0	MIPI_CUST_SEED_EN_P2_LN1	MIPI_CUST_SEED_EN_P2_LN0	MIPI_CUST_SEED_EN_P1_LN1	MIPI_CUST_SEED_EN_P1_LN0	MIPI_CUST_SEED_EN_P0_LN1	MIPI_CUST_SEED_EN_P0_LN0
0x8C3	0xF2	MIPI_PRBS_3[7:0]	RSVD	RSVD	RSVD	RSVD	–	–	MIPI_CUSTOM_SEED_2[1:0]	
0x8C4	0x78	MIPI_PRBS_4[7:0]	MIPI_CUSTOM_SEED_1[7:0]							
0x8C5	0x9A	MIPI_PRBS_5[7:0]	MIPI_CUSTOM_SEED_0[7:0]							
0x8C6	0x0F	MIPI_PHY21[7:0]	Force_Video_Mask[3:0]				Auto_Mask_En[3:0]			
0x8C7	0x0F	MIPI_PHY22[7:0]	Video_Mask_Latch_Reset	–	–	–	Video_Mask_Restart_En[3:0]			
0x8C9	0x00	MIPI_PHY24[7:0]	–	–	–	–	RST_MIPITX_LOC[3:0]			
0x8CA	0xE4	MIPI_CTRL_SEL[7:0]	MIPI_CTRL_SEL_3[1:0]		MIPI_CTRL_SEL_2[1:0]		MIPI_CTRL_SEL_1[1:0]		MIPI_CTRL_SEL_0[1:0]	
0x8D0	0x00	MIPI_PHY25[7:0]	csi2_tx1_pkt_cnt[3:0]				csi2_tx0_pkt_cnt[3:0]			
0x8D1	0x00	MIPI_PHY26[7:0]	csi2_tx3_pkt_cnt[3:0]				csi2_tx2_pkt_cnt[3:0]			
0x8D2	0x00	MIPI_PHY27[7:0]	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
0x8D3	0x00	MIPI_PHY28[7:0]	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
0x8D4	0xF0	MIPI_PHY_CP_ERR_OE[7:0]	PHY_CP1_UF_ERR_OEN	PHY_CP1_OV_ERR_OEN	PHY_CP0_UF_ERR_OEN	PHY_CP0_OV_ERR_OEN	–	–	–	–
0x8D5	0x00	MIPI_PHY_FLAGS[7:0]	–	–	–	–	DESKEW_START_OVERLAP_FLAG_3	DESKEW_START_OVERLAP_FLAG_2	DESKEW_START_OVERLAP_FLAG_1	DESKEW_START_OVERLAP_FLAG_0
0x8D6	0x0F	MIPI_PHY_OEN[7:0]	–	–	–	–	DESKEW_START_OVERLAP_OEN_3	DESKEW_START_OVERLAP_OEN_2	DESKEW_START_OVERLAP_OEN_1	DESKEW_START_OVERLAP_OEN_0
0x8D8	0x3E	MIPI_ERR_PKT_0[7:0]	ERR_PKT_EN_0	–	ERR_PKT_DT_0[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x8D9	0x3E	MIPI_ERR_PKT_1[7:0]	ERR_PKT_EN_1	–	ERR_PKT_DT_1[5:0]					
0x8DA	0x3E	MIPI_ERR_PKT_2[7:0]	ERR_PKT_EN_2	–	ERR_PKT_DT_2[5:0]					
0x8DB	0x3E	MIPI_ERR_PKT_3[7:0]	ERR_PKT_EN_3	–	ERR_PKT_DT_3[5:0]					
0x8DC	0x0F	MIPI_ERR_PKT_4[7:0]	ERR_PKT_VC_OVRD_EN_0	–	–	ERR_PKT_VC_OVRD_0[4:0]				
0x8DD	0x0F	MIPI_ERR_PKT_5[7:0]	ERR_PKT_VC_OVRD_EN_1	–	–	ERR_PKT_VC_OVRD_1[4:0]				
0x8DE	0x0F	MIPI_ERR_PKT_6[7:0]	ERR_PKT_VC_OVRD_EN_2	–	–	ERR_PKT_VC_OVRD_2[4:0]				
0x8E0	0x0F	MIPI_ERR_PKT_7[7:0]	ERR_PKT_VC_OVRD_EN_3	–	–	ERR_PKT_VC_OVRD_3[4:0]				
0x8E1	0x00	MIPI_ERR_PKT_8[7:0]	–	–	–	ERR_PKT_VC_0[4:0]				
0x8E2	0x00	MIPI_ERR_PKT_9[7:0]	–	–	–	ERR_PKT_VC_1[4:0]				
0x8E3	0x00	MIPI_ERR_PKT_10[7:0]	–	–	–	ERR_PKT_VC_2[4:0]				
0x8E4	0x00	MIPI_ERR_PKT_11[7:0]	–	–	–	ERR_PKT_VC_3[4:0]				
0x8E5	0x00	MIPI_ERR_PKT_12[7:0]	ERR_PKT_WC_OVRD_EN_3	ERR_PKT_WC_OVRD_EN_2	ERR_PKT_WC_OVRD_EN_1	ERR_PKT_WC_OVRD_EN_0	–	–	–	–
0x8E6	0x00	MIPI_ERR_PKT_13[7:0]	ERR_PKT_WC_0_H[7:0]							
0x8E7	0x00	MIPI_ERR_PKT_14[7:0]	ERR_PKT_WC_0_L[7:0]							
0x8E8	0x00	MIPI_ERR_PKT_15[7:0]	ERR_PKT_WC_1_H[7:0]							
0x8E9	0x00	MIPI_ERR_PKT_16[7:0]	ERR_PKT_WC_1_L[7:0]							
0x8EA	0x00	MIPI_ERR_PKT_17[7:0]	ERR_PKT_WC_2_H[7:0]							
0x8EB	0x00	MIPI_ERR_PKT_18[7:0]	ERR_PKT_WC_2_L[7:0]							
0x8EC	0x00	MIPI_ERR_PKT_19[7:0]	ERR_PKT_WC_3_H[7:0]							
0x8ED	0x00	MIPI_ERR_PKT_20[7:0]	ERR_PKT_WC_3_L[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
MIPI_TX 0										
0x901	0x00	MIPI_TX1[7:0]	MODE[7:0]							
0x902	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x903	0x87	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x904	0x81	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x905	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x906	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x907	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x908	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x909	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x90A	0xD0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x90B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x90C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x90D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x90E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x90F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x910	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x911	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x912	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x913	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x914	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x915	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x916	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x917	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x918	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x919	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x91A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x91B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x91C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x91D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x91E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x91F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x920	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x921	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x922	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x923	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x924	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x925	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x926	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x927	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x928	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x929	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x92A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x92B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x92C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x92D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x92E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x92F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x930	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x931	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x932	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x933	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x934	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x936	0x08	MIPI_TX54[7:0]	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
0x938	0x00	MIPI_TX56[7:0]	PKT_START_ADDR[7:0]							
0x939	0x10	MIPI_TX57[7:0]	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	RSVD
0x93A	0x00	MIPI_ERR_INJ_B1[7:0]	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
0x93B	0x00	MIPI_ERR_INJ_B2[7:0]	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
0x93C	0x00	MIPI_ERRB_DESKEW_ORDER[7:0]	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
MIPI_TX 1										
0x941	0x00	MIPI_TX1[7:0]	MODE[7:0]							
0x942	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x943	0x87	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x944	0x81	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x945	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x946	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x947	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x948	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x949	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x94A	0xD0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x94B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x94C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x94D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x94E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x94F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x950	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x951	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x952	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x953	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x954	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x955	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x956	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x957	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x958	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x959	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x95A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x95B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x95C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x95D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x95E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x95F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x960	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x961	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x962	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x963	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x964	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x965	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x966	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x967	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x968	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x969	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x96A	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x96B	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x96C	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x96D	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x96E	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x96F	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x970	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x971	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x972	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x973	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x974	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
0x976	0x08	MIPI_TX54[7:0]	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
0x978	0x00	MIPI_TX56[7:0]	PKT_START_ADDR[7:0]							
0x979	0x10	MIPI_TX57[7:0]	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	RSVD
0x97A	0x00	MIPI_ERR_INJ_B1[7:0]	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
0x97B	0x00	MIPI_ERR_INJ_B2[7:0]	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
0x97C	0x00	MIPI_ERRB_DESKEW_ORDER[7:0]	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
MIPI_TX 2										
0x981	0x00	MIPI_TX1[7:0]	MODE[7:0]							
0x982	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x983	0x87	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x984	0x81	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x985	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x986	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x987	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x988	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x989	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x98A	0xD0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x98B	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x98C	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x98D	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x98E	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x98F	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x990	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x991	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x992	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x993	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x994	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x995	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x996	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							
0x997	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x998	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x999	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x99A	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x99B	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x99C	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x99D	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x99E	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x99F	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x9A0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x9A1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x9A2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x9A3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x9A4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x9A5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x9A6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x9A7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x9A8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x9A9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x9AA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x9AB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x9AC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x9AD	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x9AE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x9AF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
0x9B0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x9B1	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x9B2	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x9B3	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x9B4	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
0x9B6	0x08	MIPI_TX54[7:0]	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
0x9B8	0x00	MIPI_TX56[7:0]	PKT_START_ADDR[7:0]							
0x9B9	0x10	MIPI_TX57[7:0]	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	TUN_NO_CORR_LENGTH

ADDRESS	RESET	NAME	MSB							LSB
0x9BA	0x00	MIPI_ERR_INJ_B1[7:0]	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
0x9BB	0x00	MIPI_ERR_INJ_B2[7:0]	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
0x9BC	0x00	MIPI_DESKEW_ERRB_ORDER[7:0]	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
MIPI_TX 3										
0x9C1	0x00	MIPI_TX1[7:0]	MODE[7:0]							
0x9C2	0x00	MIPI_TX2[7:0]	STATUS[7:0]							
0x9C3	0x87	MIPI_TX3[7:0]	DESKEW_INIT[7:0]							
0x9C4	0x81	MIPI_TX4[7:0]	DESKEW_PER[7:0]							
0x9C5	0x71	MIPI_TX5[7:0]	CSI2_T_PRE[7:0]							
0x9C6	0x19	MIPI_TX6[7:0]	CSI2_T_POST[7:0]							
0x9C7	0x1C	MIPI_TX7[7:0]	CSI2_TX_GAP[7:0]							
0x9C8	0x00	MIPI_TX8[7:0]	CSI2_TWAKEUP_L[7:0]							
0x9C9	0x01	MIPI_TX9[7:0]	CSI2_TWAKEUP_M[7:0]							
0x9CA	0xD0	MIPI_TX10[7:0]	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
0x9CB	0x00	MIPI_TX11[7:0]	MAP_EN_L[7:0]							
0x9CC	0x00	MIPI_TX12[7:0]	MAP_EN_H[7:0]							
0x9CD	0x00	MIPI_TX13[7:0]	MAP_SRC_0[7:0]							
0x9CE	0x00	MIPI_TX14[7:0]	MAP_DST_0[7:0]							
0x9CF	0x00	MIPI_TX15[7:0]	MAP_SRC_1[7:0]							
0x9D0	0x00	MIPI_TX16[7:0]	MAP_DST_1[7:0]							
0x9D1	0x00	MIPI_TX17[7:0]	MAP_SRC_2[7:0]							
0x9D2	0x00	MIPI_TX18[7:0]	MAP_DST_2[7:0]							
0x9D3	0x00	MIPI_TX19[7:0]	MAP_SRC_3[7:0]							
0x9D4	0x00	MIPI_TX20[7:0]	MAP_DST_3[7:0]							
0x9D5	0x00	MIPI_TX21[7:0]	MAP_SRC_4[7:0]							
0x9D6	0x00	MIPI_TX22[7:0]	MAP_DST_4[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x9D7	0x00	MIPI_TX23[7:0]	MAP_SRC_5[7:0]							
0x9D8	0x00	MIPI_TX24[7:0]	MAP_DST_5[7:0]							
0x9D9	0x00	MIPI_TX25[7:0]	MAP_SRC_6[7:0]							
0x9DA	0x00	MIPI_TX26[7:0]	MAP_DST_6[7:0]							
0x9DB	0x00	MIPI_TX27[7:0]	MAP_SRC_7[7:0]							
0x9DC	0x00	MIPI_TX28[7:0]	MAP_DST_7[7:0]							
0x9DD	0x00	MIPI_TX29[7:0]	MAP_SRC_8[7:0]							
0x9DE	0x00	MIPI_TX30[7:0]	MAP_DST_8[7:0]							
0x9DF	0x00	MIPI_TX31[7:0]	MAP_SRC_9[7:0]							
0x9E0	0x00	MIPI_TX32[7:0]	MAP_DST_9[7:0]							
0x9E1	0x00	MIPI_TX33[7:0]	MAP_SRC_10[7:0]							
0x9E2	0x00	MIPI_TX34[7:0]	MAP_DST_10[7:0]							
0x9E3	0x00	MIPI_TX35[7:0]	MAP_SRC_11[7:0]							
0x9E4	0x00	MIPI_TX36[7:0]	MAP_DST_11[7:0]							
0x9E5	0x00	MIPI_TX37[7:0]	MAP_SRC_12[7:0]							
0x9E6	0x00	MIPI_TX38[7:0]	MAP_DST_12[7:0]							
0x9E7	0x00	MIPI_TX39[7:0]	MAP_SRC_13[7:0]							
0x9E8	0x00	MIPI_TX40[7:0]	MAP_DST_13[7:0]							
0x9E9	0x00	MIPI_TX41[7:0]	MAP_SRC_14[7:0]							
0x9EA	0x00	MIPI_TX42[7:0]	MAP_DST_14[7:0]							
0x9EB	0x00	MIPI_TX43[7:0]	MAP_SRC_15[7:0]							
0x9EC	0x00	MIPI_TX44[7:0]	MAP_DST_15[7:0]							
0x9ED	0x00	MIPI_TX45[7:0]	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
0x9EE	0x00	MIPI_TX46[7:0]	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
0x9EF	0x00	MIPI_TX47[7:0]	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0x9F0	0x00	MIPI_TX48[7:0]	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
0x9F1	0x00	MIPI_TX49[7:0]	MAP_CON[7:0]							
0x9F2	0x00	MIPI_TX50[7:0]	SKEW_PER_SEL[7:0]							
0x9F3	0x00	MIPI_TX51[7:0]	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
0x9F4	0x00	MIPI_TX52[7:0]	video_masked_latched[3:0]				video_masked[3:0]			
0x9F6	0x08	MIPI_TX54[7:0]	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
0x9F8	0x00	MIPI_TX56[7:0]	PKT_START_ADDR[7:0]							
0x9F9	0x10	MIPI_TX57[7:0]	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	TUN_NO_CORR_LENGTH
0x9FA	0x00	MIPI_ERR_INJ_B1[7:0]	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
0x9FB	0x00	MIPI_ERR_INJ_B2[7:0]	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
0x9FC	0x00	MIPI_DESKEW_ERRB_ORDER[7:0]	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
GMSL1 A										
0xB04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
0xB05	0x39	GMSL1_5[7:0]	RSVD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xB06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xB07	0x04	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xB08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xB0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xB0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xB0F	0x01	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE

ADDRESS	RESET	NAME	MSB							LSB
0xB10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xB11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xB12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xB13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xB14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xB15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xB16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xB17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xB18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xB19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xB1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xB1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xB1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xB1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xB20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xB21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xB22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xB23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xB96	0x3B	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	DBL_ALIGN_TO
0xBCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
GMSL1 B										
0xC04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN

ADDRESS	RESET	NAME	MSB							LSB
0xC05	0x39	GMSL1_5[7:0]	RSVD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xC06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xC07	0x04	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xC08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xC0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xC0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xC0F	0x01	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xC10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xC11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]			RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]		
0xC12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]	LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN	
0xC13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xC14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xC15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xC16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xC17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xC18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xC19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xC1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xC1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xC1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xC1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xC20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0xC21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xC22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xC23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xC96	0x3B	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	DBL_ALIGN_TO
0xCCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
GMSL1 C										
0xD04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
0xD05	0x39	GMSL1_5[7:0]	RSVD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xD06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xD07	0x04	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xD08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xD0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xD0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xD0F	0x01	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xD10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xD11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
0xD12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xD13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xD14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xD15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xD16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xD17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–

ADDRESS	RESET	NAME	MSB							LSB
0xD18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xD19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xD1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xD1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xD1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xD1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDER BOOST_DET	AEQ_BST[3:0]			
0xD20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xD21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xD22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xD23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xD96	0x3B	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	DBL_ALIGN_TO
0xDCB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
GMSL1 D										
0xE04	0x03	GMSL1_4[7:0]	–	–	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
0xE05	0x39	GMSL1_5[7:0]	RSVD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
0xE06	0x6F	GMSL1_6[7:0]	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
0xE07	0x04	GMSL1_7[7:0]	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
0xE08	0x21	GMSL1_8[7:0]	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
0xE0D	0x00	GMSL1_D[7:0]	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
0xE0E	0x00	GMSL1_E[7:0]	DET_THR[7:0]							
0xE0F	0x01	GMSL1_F[7:0]	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
0xE10	0x02	GMSL1_10[7:0]	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
0xE11	0xF0	GMSL1_11[7:0]	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	

ADDRESS	RESET	NAME	MSB							LSB
0xE12	0x52	GMSL1_12[7:0]	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
0xE13	0xC0	GMSL1_13[7:0]	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
0xE14	0x80	GMSL1_14[7:0]	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
0xE15	0x00	GMSL1_15[7:0]	DET_ERR[7:0]							
0xE16	0x00	GMSL1_16[7:0]	PRBS_ERR[7:0]							
0xE17	0x00	GMSL1_17[7:0]	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
0xE18	0x00	GMSL1_18[7:0]	CC_RETR_CNT[7:0]							
0xE19	0x00	GMSL1_19[7:0]	CC_CRC_ERRCNT[7:0]							
0xE1A	0x00	GMSL1_1A[7:0]	RCEG_ERR_CNT[7:0]							
0xE1B	0x00	GMSL1_1B[7:0]	–	–	–	–	–	LINE_CRC_ERR	–	–
0xE1C	0x00	GMSL1_1C[7:0]	–	–	EOM_EYE_WIDTH[5:0]					
0xE1D	0x00	GMSL1_1D[7:0]	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
0xE20	0x00	GMSL1_20[7:0]	CRC_VALUE_0[7:0]							
0xE21	0x00	GMSL1_21[7:0]	CRC_VALUE_1[7:0]							
0xE22	0x00	GMSL1_22[7:0]	CRC_VALUE_2[7:0]							
0xE23	0x00	GMSL1_23[7:0]	CRC_VALUE_3[7:0]							
0xE96	0x3B	GMSL1_96[7:0]	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	DBL_ALIGN_TO
0xECB	0x00	GMSL1_CB[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
GMSL A										
0x1001	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1002	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1003	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1004	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x1008	0x41	GPIOA[7:0]	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x1009	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL B										
0x1011	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1012	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1013	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1014	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1018	0x41	GPIOA[7:0]	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x1019	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL C										
0x1021	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1022	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1023	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1024	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1028	0x41	GPIOA[7:0]	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x1029	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
GMSL D										
0x1031	0x00	TX1[7:0]	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
0x1032	0x20	TX2[7:0]	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
0x1033	0x44	TX3[7:0]	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
0x1034	0x00	RX0[7:0]	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
0x1038	0x41	GPIOA[7:0]	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
0x1039	0x88	GPIOB[7:0]	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
VRX_PATGEN_0 0										
0x1050	0x03	PATGEN_0[7:0]	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
0x1051	0x00	PATGEN_1[7:0]	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
0x1052	0x00	VS_DLY_2[7:0]	VS_DLY_2[7:0]							
0x1053	0x00	VS_DLY_1[7:0]	VS_DLY_1[7:0]							
0x1054	0x00	VS_DLY_0[7:0]	VS_DLY_0[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1055	0x00	VS_HIGH_2[7:0]	VS_HIGH_2[7:0]							
0x1056	0x2A	VS_HIGH_1[7:0]	VS_HIGH_1[7:0]							
0x1057	0xF8	VS_HIGH_0[7:0]	VS_HIGH_0[7:0]							
0x1058	0x26	VS_LOW_2[7:0]	VS_LOW_2[7:0]							
0x1059	0x40	VS_LOW_1[7:0]	VS_LOW_1[7:0]							
0x105A	0x00	VS_LOW_0[7:0]	VS_LOW_0[7:0]							
0x105B	0x00	V2H_2[7:0]	V2H_2[7:0]							
0x105C	0x00	V2H_1[7:0]	V2H_1[7:0]							
0x105D	0x00	V2H_0[7:0]	V2H_0[7:0]							
0x105E	0x00	HS_HIGH_1[7:0]	HS_HIGH_1[7:0]							
0x105F	0xD0	HS_HIGH_0[7:0]	HS_HIGH_0[7:0]							
0x1060	0x09	HS_LOW_1[7:0]	HS_LOW_1[7:0]							
0x1061	0x50	HS_LOW_0[7:0]	HS_LOW_0[7:0]							
0x1062	0x04	HS_CNT_1[7:0]	HS_CNT_1[7:0]							
0x1063	0xDA	HS_CNT_0[7:0]	HS_CNT_0[7:0]							
0x1064	0x00	V2D_2[7:0]	V2D_2[7:0]							
0x1065	0x55	V2D_1[7:0]	V2D_1[7:0]							
0x1066	0xF0	V2D_0[7:0]	V2D_0[7:0]							
0x1067	0x07	DE_HIGH_1[7:0]	DE_HIGH_1[7:0]							
0x1068	0x80	DE_HIGH_0[7:0]	DE_HIGH_0[7:0]							
0x1069	0x00	DE_LOW_1[7:0]	DE_LOW_1[7:0]							
0x106A	0x40	DE_LOW_0[7:0]	DE_LOW_0[7:0]							
0x106B	0x04	DE_CNT_1[7:0]	DE_CNT_1[7:0]							
0x106C	0xB0	DE_CNT_0[7:0]	DE_CNT_0[7:0]							
0x106D	0x06	GRAD_INCR[7:0]	GRAD_INCR[7:0]							
0x106E	0x80	CHKR_COLOR_A_L[7:0]	CHKR_COLOR_A_L[7:0]							
0x106F	0x00	CHKR_COLOR_A_M[7:0]	CHKR_COLOR_A_M[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x1070	0x04	CHKR_COLOR_A_H[7:0]	CHKR_COLOR_A_H[7:0]							
0x1071	0x00	CHKR_COLOR_B_L[7:0]	CHKR_COLOR_B_L[7:0]							
0x1072	0x08	CHKR_COLOR_B_M[7:0]	CHKR_COLOR_B_M[7:0]							
0x1073	0x80	CHKR_COLOR_B_H[7:0]	CHKR_COLOR_B_H[7:0]							
0x1074	0x50	CHKR_RPT_A[7:0]	CHKR_RPT_A[7:0]							
0x1075	0x50	CHKR_RPT_B[7:0]	CHKR_RPT_B[7:0]							
0x1076	0x50	CHKR_ALT[7:0]	CHKR_ALT[7:0]							
TEST_CTRL										
0x1191	0xFF	DP_ORSTB_CTL[7:0]	DPLL_AUTO_RST	DP_RST_MIPI3	DP_RST_STABLE	DP_RST_MIPI2	DP_RST_MIPI	DP_RST_VP	DP_RST_FS	DP_RST_CC
VID_PXL_CRC_ERR										
0x11D0	0x00	CNT_AX[7:0]	VID_PXL_CRC_ERR_AX[7:0]							
0x11D1	0x00	CNT_AY[7:0]	VID_PXL_CRC_ERR_AY[7:0]							
0x11D2	0x00	CNT_AZ[7:0]	VID_PXL_CRC_ERR_AZ[7:0]							
0x11E0	0x00	CNT_AU[7:0]	VID_PXL_CRC_ERR_AU[7:0]							
0x11E1	0x00	CNT_BX[7:0]	VID_PXL_CRC_ERR_BX[7:0]							
0x11E2	0x00	CNT_BY[7:0]	VID_PXL_CRC_ERR_BY[7:0]							
0x11E3	0x00	CNT_BZ[7:0]	VID_PXL_CRC_ERR_BZ[7:0]							
0x11E4	0x00	CNT_BU[7:0]	VID_PXL_CRC_ERR_BU[7:0]							
0x11E5	0x00	CNT_CX[7:0]	VID_PXL_CRC_ERR_CX[7:0]							
0x11E6	0x00	CNT_CY[7:0]	VID_PXL_CRC_ERR_CY[7:0]							
0x11E7	0x00	CNT_CZ[7:0]	VID_PXL_CRC_ERR_CZ[7:0]							
0x11E8	0x00	CNT_CU[7:0]	VID_PXL_CRC_ERR_CU[7:0]							
0x11E9	0x00	CNT_DX[7:0]	VID_PXL_CRC_ERR_DX[7:0]							
0x11EA	0x00	CNT_DY[7:0]	VID_PXL_CRC_ERR_DY[7:0]							
0x11EB	0x00	CNT_DZ[7:0]	VID_PXL_CRC_ERR_DZ[7:0]							
0x11EC	0x00	CNT_DU[7:0]	VID_PXL_CRC_ERR_DU[7:0]							
VID_HVD_DET										
0x11F0	0x00	DE_DET[7:0]	–	–	–	–	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
0x11F1	0x00	HS_DET[7:0]	–	–	–	–	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
0x11F2	0x00	VS_DET[7:0]	–	–	–	–	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
0x11F3	0x00	HS_POL[7:0]	–	–	–	–	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
0x11F4	0x00	VS_POL[7:0]	–	–	–	–	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0

ADDRESS	RESET	NAME	MSB							LSB
0x11F9	0x0F	HVD_CNT_CTRL[7:0]	HVD_CNT_RST_3	HVD_CNT_RST_2	HVD_CNT_RST_1	HVD_CNT_RST_0	HVD_CNT_EN_3	HVD_CNT_EN_2	HVD_CNT_EN_1	HVD_CNT_EN_0
0x11FA	0x00	HVD_CNT_OS[7:0]	–	–	–	–	HVD_CNT_OS_EN_3	HVD_CNT_OS_EN_2	HVD_CNT_OS_EN_1	HVD_CNT_OS_EN_0
0x1200	0x03	VS_CNT_WNDW_0_MSB[7:0]	–	–	–	–	–	–	VS_CNT_WINDOW_0_MSB[1:0]	
0x1201	0xE8	VS_CNT_WNDW_0_LSB[7:0]	VS_CNT_WINDOW_0_LSB[7:0]							
0x1202	0x00	VS_CNT_0_CMP[7:0]	–	–	VS_CNT_0_CMP[5:0]					
0x1203	0x00	HS_CNT_0_CMP_MSB[7:0]	–	–	–	–	HS_CNT_0_CMP_MSB[3:0]			
0x1204	0x00	HS_CNT_0_CMP_LSB[7:0]	HS_CNT_0_CMP_LSB[7:0]							
0x1205	0x00	DE_CNT_0_CMP_MSB[7:0]	–	–	–	–	DE_CNT_0_CMP_MSB[3:0]			
0x1206	0x00	DE_CNT_0_CMP_LSB[7:0]	DE_CNT_0_CMP_LSB[7:0]							
0x1207	0x00	VS_CNT_0[7:0]	–	–	VS_CNT_0[5:0]					
0x1208	0x00	HS_CNT_0_MSB[7:0]	–	–	–	–	HS_CNT_0_MSB[3:0]			
0x1209	0x00	HS_CNT_0_LSB[7:0]	HS_CNT_0_LSB[7:0]							
0x120A	0x00	DE_CNT_0_MSB[7:0]	–	–	–	–	DE_CNT_0_MSB[3:0]			
0x120B	0x00	DE_CNT_0_LSB[7:0]	DE_CNT_0_LSB[7:0]							
0x120C	0xE0	VRX_0_CMP_ERR_OEN[7:0]	VS_CNT_0_CMP_ERR_OEN	HS_CNT_0_CMP_ERR_OEN	DE_CNT_0_CMP_ERR_OEN	–	–	–	–	–
0x120D	0x00	VRX_0_CMP_ERR_FLAG[7:0]	VS_CNT_0_CMP_ERR_FLAG	HS_CNT_0_CMP_ERR_FLAG	DE_CNT_0_CMP_ERR_FLAG	–	–	–	–	–
0x1210	0x03	VS_CNT_WNDW_1_MSB[7:0]	–	–	–	–	–	–	VS_CNT_WINDOW_1_MSB[1:0]	
0x1211	0xE8	VS_CNT_WNDW_1_LSB[7:0]	VS_CNT_WINDOW_1_LSB[7:0]							
0x1212	0x00	VS_CNT_1_CMP[7:0]	–	–	VS_CNT_1_CMP[5:0]					
0x1213	0x00	HS_CNT_1_CMP_MSB[7:0]	–	–	–	–	HS_CNT_1_CMP_MSB[3:0]			

ADDRESS	RESET	NAME	MSB							LSB
0x1214	0x00	HS_CNT_1_CMP_LSB[7:0]	HS_CNT_1_CMP_LSB[7:0]							
0x1215	0x00	DE_CNT_1_CMP_MSB[7:0]	–	–	–	–	DE_CNT_1_CMP_MSB[3:0]			
0x1216	0x00	DE_CNT_1_CMP_LSB[7:0]	DE_CNT_1_CMP_LSB[7:0]							
0x1217	0x00	VS_CNT_1[7:0]	–	–	VS_CNT_1[5:0]					
0x1218	0x00	HS_CNT_1_MSB[7:0]	–	–	–	–	HS_CNT_1_MSB[3:0]			
0x1219	0x00	HS_CNT_1_LSB[7:0]	HS_CNT_1_LSB[7:0]							
0x121A	0x00	DE_CNT_1_MSB[7:0]	–	–	–	–	DE_CNT_1_MSB[3:0]			
0x121B	0x00	DE_CNT_1_LSB[7:0]	DE_CNT_1_LSB[7:0]							
0x121C	0xE0	VRX_1_CMP_ERR_OEN[7:0]	VS_CNT_1_CMP_ERR_OEN	HS_CNT_1_CMP_ERR_OEN	DE_CNT_1_CMP_ERR_OEN	–	–	–	–	–
0x121D	0x00	VRX_1_CMP_ERR_FLAG[7:0]	VS_CNT_1_CMP_ERR_FLAG	HS_CNT_1_CMP_ERR_FLAG	DE_CNT_1_CMP_ERR_FLAG	–	–	–	–	–
0x1220	0x03	VS_CNT_WNDW_2_MSB[7:0]	–	–	–	–	–	–	VS_CNT_WINDOW_2_MSB[1:0]	
0x1221	0xE8	VS_CNT_WNDW_2_LSB[7:0]	VS_CNT_WINDOW_2_LSB[7:0]							
0x1222	0x00	VS_CNT_2_CMP[7:0]	–	–	VS_CNT_2_CMP[5:0]					
0x1223	0x00	HS_CNT_2_CMP_MSB[7:0]	–	–	–	–	HS_CNT_2_CMP_MSB[3:0]			
0x1224	0x00	HS_CNT_2_CMP_LSB[7:0]	HS_CNT_2_CMP_LSB[7:0]							
0x1225	0x00	DE_CNT_2_CMP_MSB[7:0]	–	–	–	–	DE_CNT_2_CMP_MSB[3:0]			
0x1226	0x00	DE_CNT_2_CMP_LSB[7:0]	DE_CNT_2_CMP_LSB[7:0]							
0x1227	0x00	VS_CNT_2[7:0]	–	–	VS_CNT_2[5:0]					
0x1228	0x00	HS_CNT_2_MSB[7:0]	–	–	–	–	HS_CNT_2_MSB[3:0]			
0x1229	0x00	HS_CNT_2_LSB[7:0]	HS_CNT_2_LSB[7:0]							
0x122A	0x00	DE_CNT_2_MSB[7:0]	–	–	–	–	DE_CNT_2_MSB[3:0]			
0x122B	0x00	DE_CNT_2_LSB[7:0]	DE_CNT_2_LSB[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x122C	0xE0	VRX_2_CMP_ERR_OEN[7:0]	VS_CNT_2_CMP_ERR_OEN	HS_CNT_2_CMP_ERR_OEN	DE_CNT_2_CMP_ERR_OEN	–	–	–	–	–
0x122D	0x00	VRX_2_CMP_ERR_FLAG[7:0]	VS_CNT_2_CMP_ERR_FLAG	HS_CNT_2_CMP_ERR_FLAG	DE_CNT_2_CMP_ERR_FLAG	–	–	–	–	–
0x1230	0x03	VS_CNT_WNDW_3_MSB[7:0]	–	–	–	–	–	–	VS_CNT_WINDOW_3_MSB[1:0]	
0x1231	0xE8	VS_CNT_WNDW_3_LSB[7:0]	VS_CNT_WINDOW_3_LSB[7:0]							
0x1232	0x00	VS_CNT_3_CMP[7:0]	–	–	VS_CNT_3_CMP[5:0]					
0x1233	0x00	HS_CNT_3_CMP_MSB[7:0]	–	–	–	–	HS_CNT_3_CMP_MSB[3:0]			
0x1234	0x00	HS_CNT_3_CMP_LSB[7:0]	HS_CNT_3_CMP_LSB[7:0]							
0x1235	0x00	DE_CNT_3_CMP_MSB[7:0]	–	–	–	–	DE_CNT_3_CMP_MSB[3:0]			
0x1236	0x00	DE_CNT_3_CMP_LSB[7:0]	DE_CNT_3_CMP_LSB[7:0]							
0x1237	0x00	VS_CNT_3[7:0]	–	–	VS_CNT_3[5:0]					
0x1238	0x00	HS_CNT_3_MSB[7:0]	–	–	–	–	HS_CNT_3_MSB[3:0]			
0x1239	0x00	HS_CNT_3_LSB[7:0]	HS_CNT_3_LSB[7:0]							
0x123A	0x00	DE_CNT_3_MSB[7:0]	–	–	–	–	DE_CNT_3_MSB[3:0]			
0x123B	0x00	DE_CNT_3_LSB[7:0]	DE_CNT_3_LSB[7:0]							
0x123C	0xE0	VRX_3_CMP_ERR_OEN[7:0]	VS_CNT_3_CMP_ERR_OEN	HS_CNT_3_CMP_ERR_OEN	DE_CNT_3_CMP_ERR_OEN	–	–	–	–	–
0x123D	0x00	VRX_3_CMP_ERR_FLAG[7:0]	VS_CNT_3_CMP_ERR_FLAG	HS_CNT_3_CMP_ERR_FLAG	DE_CNT_3_CMP_ERR_FLAG	–	–	–	–	–
TUN_DET										
0x1260	0x00	TUN_MODE_DET[7:0]	CPHY_MODE_OVRD_EN	–	–	–	BACKTOP4_TUN_DET	BACKTOP3_TUN_DET	BACKTOP2_TUN_DET	BACKTOP1_TUN_DET
0x1261	0xF0	TUN_CPHY_DET[7:0]	BACKTOP4_CPHY_MODE_OVRD	BACKTOP3_CPHY_MODE_OVRD	BACKTOP2_CPHY_MODE_OVRD	BACKTOP1_CPHY_MODE_OVRD	BACKTOP4_CPHY_MODE_DET	BACKTOP3_CPHY_MODE_DET	BACKTOP2_CPHY_MODE_DET	BACKTOP1_CPHY_MODE_DET

ADDRESS	RESET	NAME	MSB							LSB
0x1262	0x00	TUN_CPHY_LANE_DET[7:0]	BACKTOP4_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP3_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP2_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP1_TUN_CPHY_SER_LANE_DET[1:0]	
0x1264	0x00	TMD_HEADER_ERR_FLAGS_1[7:0]	BACKTOP1_TMD_SP_DET_ERR	–	BACKTOP1_TMD_CRC_2L_ERR_FLAG	BACKTOP1_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP1_TMD_ECC_ERR_FLAG	BACKTOP1_TMD_ECC_FLAG
0x1265	0x00	TMD_HEADER_ERR_FLAGS_2[7:0]	BACKTOP2_TMD_SP_DET_ERR	–	BACKTOP2_TMD_CRC_2L_ERR_FLAG	BACKTOP2_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP2_TMD_ECC_ERR_FLAG	BACKTOP2_TMD_ECC_FLAG
0x1266	0x00	TMD_HEADER_ERR_FLAGS_3[7:0]	BACKTOP3_TMD_SP_DET_ERR	–	BACKTOP3_TMD_CRC_2L_ERR_FLAG	BACKTOP3_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP3_TMD_ECC_ERR_FLAG	BACKTOP3_TMD_ECC_FLAG
0x1267	0x00	TMD_HEADER_ERR_FLAGS_4[7:0]	BACKTOP4_TMD_SP_DET_ERR	–	BACKTOP4_TMD_CRC_2L_ERR_FLAG	BACKTOP4_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP4_TMD_ECC_ERR_FLAG	BACKTOP4_TMD_ECC_FLAG
0x126A	0x00	TMD_PKT_CNT_1[7:0]	TMD_PKT_CNT_1[7:0]							
0x126B	0x00	TMD_PKT_CNT_2[7:0]	TMD_PKT_CNT_2[7:0]							
0x126C	0x00	TMD_PKT_CNT_3[7:0]	TMD_PKT_CNT_3[7:0]							
0x126D	0x00	TMD_PKT_CNT_4[7:0]	TMD_PKT_CNT_4[7:0]							
0x126E	0x00	TMD_PKT_CNT_1_H[7:0]	–	–	–	TMD_PKT_CNT_1_H[4:0]				
0x126F	0x00	TMD_PKT_CNT_2_H[7:0]	–	–	–	TMD_PKT_CNT_2_H[4:0]				
0x1270	0x00	TMD_PKT_CNT_3_H[7:0]	–	–	–	TMD_PKT_CNT_3_H[4:0]				
0x1271	0x00	TMD_PKT_CNT_4_H[7:0]	–	–	–	TMD_PKT_CNT_4_H[4:0]				

Register Details

REG0 (0x0)

Device I²C address and Blocks I²C register writes

BIT	7	6	5	4	3	2	1	0
Field	DEV_ADDR[6:0]							CFG_BLOCK
Reset	0b0100111							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ADDR	7:1	Device Address Default address is set by the CFG0 pin at power-up. Refer to data sheet discussion of the CFG0 pin for further information. Address can be changed following power-up by updating the contents of this register.	0b0000000: I2C write/read address is 0x00/0x01 0b0000001: I2C write/read address is 0x02/0x03 ... ... 0b1001000: I2C write/read address is 0x90/0x91 0b1001010: I2C write/read address is 0x94/0x95 0b1001100: I2C write/read address is 0x98/0x99 0b1101000: I2C write/read address is 0xD0/0xD1 0b1101010: I2C write/read address is 0xD4/0xD5 0b1101100: I2C write/read address is 0xD8/0xD9 0b0101000: I2C write/read address is 0x50/0x51 0b0101010: I2C write/read address is 0x54/0x55 ... ... 0b1111111: I2C write/read address is 0xFE/0xFF
CFG_BLOCK	0	Configuration Block When set, all registers become non-writable (read-only). Only blocks writeable registers from being written. This bit is used to freeze the chip configuration. After set, this bit becomes not writeable. To reset the register to "Not blocked," the part must be powered down or power cycled.	0b0: Not blocked 0b1: Blocked

REG1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		DIS_LOC_CC[1:0]		–	–	–	–
Reset	0b11		0b00		–	–	–	–
Access Type			Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LOC_CC	5:4	Disables control channel connection to I2C Ports 1 and 0 Bit 4 controls Port 0. Bit 5 controls Port 1. See bit 2 for control of control channel Port 2.	0bx0: Port 0 Rx/SDA and Tx/SCL connected to control channel 0bx1: Port 0 Rx/SDA and Tx/SCL disconnected from control channel 0b0x: Port 1 Rx1/SDA1 and Tx1/SCL1 connected to control channel 0b1x: Port 1 Rx1/SDA1 and Tx1/SCL1 disconnected from control channel

REG3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	DIS_REM_CC_D[1:0]		DIS_REM_CC_C[1:0]		DIS_REM_CC_B[1:0]		DIS_REM_CC_A[1:0]	
Reset	0b10		0b10		0b10		0b10	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_REM_CC_D	7:6	Disable GMSL2 remote control channel link from each CC port to Link D Bit 0 disables the connection from port 0. Bit 1 disables the connection from port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_C	5:4	Disable GMSL2 remote control channel link from each CC port to Link C Bit 0 disables the connection from port 0. Bit 1 disables the connection from port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_B	3:2	Disable GMSL2 remote control channel link from each CC port to Link B Bit 0 disables the connection from port 0. Bit 1 disables the connection from port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled
DIS_REM_CC_A	1:0	Disable GMSL2 remote control channel link from each CC port to Link A Bit 0 disables the connection from port 0. Bit 1 disables the connection from port 1.	0b0: Remote control channel enabled 0b1: Remote control channel disabled

REG4 (0x4)

Video channel - GMSL2 Video pipe access

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VID_EN_3	VID_EN_2	VID_EN_1	VID_EN_0
Reset	–	–	–	–	0b1	0b1	0b1	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VID_EN_3	3	VID_EN3 Video Enable - Video switch used to access Pipe 3 video flow	0b0: Video transmit Channel 3 disabled 0b1: Video transmit Channel 3 enabled
VID_EN_2	2	VID_EN2 Video Enable - Video switch used to access Pipe 2 video flow	0b0: Video transmit Channel 2 disabled 0b1: Video transmit Channel 2 enabled
VID_EN_1	1	VID_EN1 Video Enable - Video switch used to access Pipe 1 video flow	0b0: Video transmit Channel 1 disabled 0b1: Video transmit Channel 1 enabled
VID_EN_0	0	VID_EN0 Video Enable - Video switch used to access Pipe 0 video flow	0b0: Video transmit Channel 0 disabled 0b1: Video transmit Channel 0 enabled

REG5 (0x5)

LOCK and ERRB enable and configuration

BIT	7	6	5	4	3	2	1	0
Field	LOCK_EN	ERRB_EN	LOCK_CFG	ERRB_LOCK_OEN	ERRB_MST_RST	–	–	RSVD
Reset	0x1	0x1	0b0	0b0		–	–	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read	–	–	

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_EN	7	Enable LOCK output	0b0: LOCK output disabled 0b1: LOCK output enabled
ERRB_EN	6	Enables ERRB output to GPIO	0b0: ERRB output disabled 0b1: ERRB output enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK_CFG	5	Configures LOCK pin behavior. See the LOCK_POUT register field for additional information.	0b0: GMSL2 link locked 0b1: GMSL2 link locked and MIPI output started
ERRB_LOCK_OEN	4	Enable output of lock through the ERRB pin. 1'b0 - Disable 1'b1 - Enable When enabled, if any one of the enabled GMSL links is not locked, the status is reflected on the ERRB pin that is asserted low.	0x0: Disable 0x1: Enable
ERRB_MST_RST	3	Master ERRB output reset. Write 1 to clear all the inputs to the ERRB generation logic. This bit self-clears. Note: This does not clear the error condition(s) that resulted from assertion of the ERRB output. The user must address and fix the cause for the error condition(s) before asserting this master reset.	0x0: Disabled 0x1: Enabled - returns to 0 after assertion

REG6 (0x6)

BIT	7	6	5	4	3	2	1	0
Field	GMSL2_D	GMSL2_C	GMSL2_B	GMSL2_A	LINK_EN_D	LINK_EN_C	LINK_EN_B	LINK_EN_A
Reset	0b1	0b1	0b1	0b1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GMSL2_D	7	GMSL1/GMSL2 Selection for Link D Bit is set according to the latched CFG1/ MFP6 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_C	6	GMSL1/GMSL2 Selection for Link C Bit is set according to the latched CFG1/ MFP6 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_B	5	GMSL1/GMSL2 Selection for Link B Bit is set according to the latched CFG1/ MFP6 pin value at power-up	0b0: GMSL1 0b1: GMSL2
GMSL2_A	4	GMSL1/GMSL2 Selection for Link A Bit is set according to the latched CFG1/ MFP6 pin value at power-up	0b0: GMSL1 0b1: GMSL2
LINK_EN_D	3	Enables Link D	0b0: DisableLink D 0b1: Enable Link D
LINK_EN_C	2	Enables Link C	0b0: Disable Link C 0b1: Enable Link C
LINK_EN_B	1	Enables Link B	0b0: Disable Link B 0b1: Enable Link B
LINK_EN_A	0	Enables Link A	0b0: Disable Link A 0b1: Enable Link A

REG7 (0x7)

BIT	7	6	5	4	3	2	1	0
Field	CC_CROSSOVER_SEL[3:0]				RSVD[3:0]			
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CROSSOVER_SEL	7:4	Control Channel Port Crossover Selector The primary microcontroller must be connected to I2C Port 0. The secondary microcontroller(s) should be connected to I2C Port 1. Typically, most serializers have only a single control channel (CC) I2C port which, by default, is connected across the GMSL2 link to the GM24 I2C Port 0. The crossover bits are used to allow the secondary microcontroller to connect Port 1 to access the CC in the serializer; otherwise, it is not possible for the microcontroller on Port 1 to program the serializer. Bits in this register select whether control channel port crossover is disabled or enabled between Port 0 and Port 1 Each of the links is controlled by a bit in the bitfield. The description of each link's bits are as follows: Link A Bit[4]: 0—No Crossover 1—Enable Crossover between Port 0 and Port 1 Link B Bit[5]: 0—No Crossover 1—Enable Crossover between Port 0 and Port 1 Link C Bit[6] 0—No Crossover 1—Enable Crossover between Port 0 and Port 1 Link D Bit[7]: 0—No Crossover 1—Enable Crossover between Port 0 and Port 1	0bXXX0XXX0: Link A—No Crossover 0bXXX1XXX0: Link A—Enable Crossover between Port 0 and Port 1 0bXXX0XXX1: Link A—Enable Crossover between Port 0 and Port 1 0bXX0XXX0X: Link B—No Crossover 0bXX1XXX0X: Link B—Enable Crossover between Port 0 and Port 1 0bXX0XXX1X: Link B—Enable Crossover between Port 0 and Port 1 0bX0XXX0XX: Link C—No Crossover 0bX1XXX0XX: Link C—Enable Crossover between Port 0 and Port 1 0bX0XXX1XX: Link C—Enable Crossover between Port 0 and Port 1 0b0XXX0XXX: Link D—No Crossover 0b1XXX0XXX: Link D—Enable Crossover between Port 0 and Port 1 0b0XXX1XXX: Link D—Enable Crossover between Port 0 and Port 1

CTRL12 (0xA)

GMSL Link Lock status

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_B	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_B	3	GMSL2 Link Locked - Link B Only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

CTRL13 (0xB)

GMSL Link Lock status

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_C	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_C	3	GMSL2 Link Locked - Link C Only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

CTRL14 (0xC)

GMSL Link Lock status

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	–	–	LOCKED_D	–	–	–
Reset	0b0	0b0	–	–	0b0	–	–	–
Access Type			–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_D	3	GMSL2 Link Locked - Link D Only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked

REG13 (0xD)

BIT	7	6	5	4	3	2	1	0
Field	DEV_ID[7:0]							
Reset	0xA2							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_ID	7:0	Device Identifier	0xA2: MAX96724 0xA3: MAX96724F 0xA4: MAX96724R

REG26 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYB[1:0]		RX_RATE_PHYB[1:0]		TX_RATE_PHYA[1:0]		RX_RATE_PHYA[1:0]	
Reset	0x0		0x2		0x0		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_RATE_PHYB	7:6	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYB	5:4	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1/MFP6 pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved
TX_RATE_PHYA	3:2	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYA	1:0	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1/MFP6 pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

REG27 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	TX_RATE_PHYD[1:0]		RX_RATE_PHYD[1:0]		TX_RATE_PHYC[1:0]		RX_RATE_PHYC[1:0]	
Reset	0x0		0x2		0x0		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_RATE_PHYD	7:6	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved
RX_RATE_PHYD	5:4	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1/MFP6 pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved
TX_RATE_PHYC	3:2	Transmitter Rate (when changed, becomes active after next link reset)	0b00: 187.5Mbps 0b01: Reserved 0b10: Reserved 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
RX_RATE_PHYC	1:0	Receiver Rate (when changed, becomes active after next link reset) Default value is set by CFG1/MFP6 pin at power-up.	0b00: Reserved 0b01: 3Gbps 0b10: 6Gbps 0b11: Reserved

PWR0 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_STATUS[2:0]			CMP_STATUS[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_STATUS	7:5	Power manager switched 1V supply comparator status bits.	0bXX1: Latched high when VDDA_sw < 0.82V 0bX1X: Latched high when VDD_sw < 0.82V 0b1XX: Reserved
CMP_STATUS	4:0	Power manager comparator status bits.	0bXXXX0: Latched low when V_{DD18} < 1.617V 0bXXX0X: Latched low when switched V_{DDIO} supply < 1.617V 0bXX0XX: Latched low when CAPVDD < 0.82V 0bX0XXX: Reserved 0b0XXXX: Reserved

PWR1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RESET_ALL	RSVD[5:0]					
Reset	0b0	0b0	0x0					
Access Type		Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_ALL	6	Device Reset Writing 1 to this bit resets the device. All blocks and registers are reset to defaults. This is equivalent to toggling the PWDNB pin. The bit is cleared when written.	0b0: No action 0b1: Activate chip reset

CTRL1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	RESET_LINK_D	RESET_LINK_C	RESET_LINK_B	RESET_LINK_A	RESET_ONESHOT_D	RESET_ONESHOT_C	RESET_ONESHOT_B	RESET_ONESHOT_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESET_LINK_D	7	Link D Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_C	6	Link C Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_B	5	Link B Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_LINK_A	4	Link A Reset Resets whole data path (keep register settings). Write 1 to activate reset, write 0 to release reset.	0b0: Release link reset 0b1: Activate link reset
RESET_ONESHOT_D	3	Link D One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONESHOT_C	2	Link C One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONESHOT_B	1	Link B One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path
RESET_ONESHOT_A	0	Link A One-Shot Reset Resets whole data path (keep register settings) one shot. Write 1 to activate reset, bit self-clears and automatically releases reset.	0b0: No action 0b1: Reset data path

CTRL3 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD[1:0]		LOCKED_A	ERROR	CMU_LOCKED	LOCK_PIN
Reset	0b0	0b0	0x1		0b0	0b0	0b0	0x0
Access Type					Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_A	3	GMSL2 link lock (bidirectional)—Link A only	0b0: GMSL2 link not locked 0b1: GMSL2 link locked
ERROR	2	Reflects error status (inverse of ERRB pin value)	0b0: ERRB not asserted (ERRB pin = 1) 0b1: ERRB asserted (ERRB pin = 0)
CMU_LOCKED	1	Clock Multiplier Unit (CMU) lock	0b0: CMU not locked 0b1: CMU locked
LOCK_PIN	0	Reflects LOCK pin output. See the LOCK_EN, LOCK_CFG, and ERRB_LOCK register fields for additional information.	0x0: 1 or more enabled GMSL links are not locked 0x1: All enabled GMSL links are locked

CTRL11 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	CXTP_D	RSVD	CXTP_C	RSVD	CXTP_B	RSVD	CXTP_A
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type		Write, Read		Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CXTP_D	6	Coax/Twisted-Pair Cable Select for Link D Bit is set according to the latched CFG1/ MFP6 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_C	4	Coax/Twisted-Pair Cable Select for Link C Bit is set according to the latched CFG1/ MFP6 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_B	2	Coax/Twisted-Pair Cable Select for Link B Bit is set according to the latched CFG1/ MFP6 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive
CXTP_A	0	Coax/Twisted-Pair Cable Select for Link A Bit is set according to the latched CFG1 pin value at power-up.	0b0: Shielded twisted-pair drive 0b1: Coax drive

INTR2 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DEC_ERR_OEN_D	DEC_ERR_OEN_C	DEC_ERR_OEN_B	DEC_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_OEN_D	3	Enables reporting of decoding errors (DEC_ERR_FLAG_D—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_D) at ERRB pin
DEC_ERR_OEN_C	2	Enables reporting of decoding errors (DEC_ERR_FLAG_C—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_C) at ERRB pin
DEC_ERR_OEN_B	1	Enables reporting of decoding errors (DEC_ERR_FLAG_B—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_B) at ERRB pin
DEC_ERR_OEN_A	0	Enables reporting of decoding errors (DEC_ERR_FLAG_A—0x26) at ERRB pin.	0b0: Disable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin 0b1: Enable reporting of decoding errors (DEC_ERR_FLAG_A) at ERRB pin

INTR3 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	DEC_ERR_FLAG_D	DEC_ERR_FLAG_C	DEC_ERR_FLAG_B	DEC_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_FLAG_D	3	Decoding error flag for Link D, asserted when DEC_ERR_D ≥ DEC_ERR_THR. To clear this flag, read register DEC_ERR_D	0b0: DEC_ERR_D < DEC_ERR_THR 0b1: DEC_ERR_D ≥ DEC_ERR_THR
DEC_ERR_FLAG_C	2	Decoding error flag for Link C, asserted when DEC_ERR_C ≥ DEC_ERR_THR. To clear this flag, read register DEC_ERR_C	0b0: DEC_ERR_C < DEC_ERR_THR 0b1: DEC_ERR_C ≥ DEC_ERR_THR
DEC_ERR_FLAG_B	1	Decoding error flag for Link B, asserted when DEC_ERR_B ≥ DEC_ERR_THR. To clear this flag, read register DEC_ERR_B	0b0: DEC_ERR_B < DEC_ERR_THR 0b1: DEC_ERR_B ≥ DEC_ERR_THR
DEC_ERR_FLAG_A	0	Decoding error flag for Link A, asserted when DEC_ERR_A ≥ DEC_ERR_THR. To clear this flag, read register DEC_ERR_A	0b0: DEC_ERR_A < DEC_ERR_THR 0b1: DEC_ERR_A ≥ DEC_ERR_THR

INTR4 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_OEN_D	EOM_ERR_OEN_C	EOM_ERR_OEN_B	EOM_ERR_OEN_A	RSVD	LFLT_INT_OEN	–	–
Reset	0b1	0b1	0b1	0b1	0b0	0x1	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_OEN_D	7	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_D—0x28) for Link D at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_D) for Link D at ERRB pin
EOM_ERR_OEN_C	6	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_C—0x28) for Link C at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_C) for Link C at ERRB pin
EOM_ERR_OEN_B	5	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_B—0x28) for Link B at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_B) for Link B at ERRB pin
EOM_ERR_OEN_A	4	Enables reporting of eye-opening monitor error (EOM_ERR_FLAG_A0x28) for Link A at ERRB pin.	0b0: Disable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin 0b1: Enable reporting of eye-opening monitor error (EOM_ERR_FLAG_A) for Link A at ERRB pin
LFLT_INT_OEN	2	Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin	0b0: Disable reporting of line fault interrupt (LFLT_INT) at ERRB pin 0b1: Enable reporting of line fault interrupt (LFLT_INT) at ERRB pin

INTR5 (0x28)

BIT	7	6	5	4	3	2	1	0
Field	EOM_ERR_FLAG_D	EOM_ERR_FLAG_C	EOM_ERR_FLAG_B	EOM_ERR_FLAG_A	RSVD	LFLT_INT	–	–
Reset	0b0	0b0	0b0	0b0	0x0	0b0	–	–
Access Type	Read Only	Read Only	Read Only	Read Only		Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_D	7	Link D Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link D.	0b0: Eye-opening is above configured threshold for Link D 0b1: Eye-opening is below configured threshold for Link D
EOM_ERR_FLAG_C	6	Link C Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link C.	0b0: Eye-opening is above configured threshold for Link C 0b1: Eye-opening is below configured threshold for Link C
EOM_ERR_FLAG_B	5	Link B Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link B.	0b0: Eye-opening is above configured threshold for Link B 0b1: Eye-opening is below configured threshold for Link B

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_ERR_FLAG_A	4	Link A Eye-opening Threshold Status Indicates whether or not eye-opening is below configured threshold for Link A.	0b0: Eye-opening is above configured threshold for Link A 0b1: Eye-opening is below configured threshold for Link A
LFLT_INT	2	Line Fault Interrupt Asserted when any one of the line fault monitors indicates a fault status. When enabled, this interrupt will be enabled onto the ERRB pin. See register LFLT_INT_OEN See the LF_0, LF_1, LF_2, LF_3, and LFLT_INT_FLAG register fields. Note: This bit is sticky and will only be cleared when the LFLT_INT_FLAG is read. The individual line fault interrupt outputs maybe masked. See the MASK_LF0, MASK_LF1, MASK_LF2, and MASK_LF3 registers.	0x0: no Line Fault interrupt asserted 0x1: Line Fault Interrupt asserted

INTR6 (0x29)

BIT	7	6	5	4	3	2	1	0
Field	G1_D_ERR_OEN	G1_C_ERR_OEN	G1_B_ERR_OEN	G1_A_ERR_OEN	LCRC_ERR_OEN	VPRBS_ERR_OEN	REM_ERR_OEN	FSYNC_ERR_OEN
Reset	0x1	0x1	0x1	0x1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_OEN	7	Enables reporting of GMSL1 Link D errors (G1_D_ERR_FLAG) at ERRB pin. This controls a composite output to the ERRB pin. Individual error flag outputs to the ERRB pin are controlled by the following registers for Link D: DET_ERRB_OEN (DER_ERR_FLAG) EOM_ERRB_OEN (EOM_ERR_FLAG) LINE_CRC_ERRB_OEN (LINE_CRC_ERR_FLAG) UNDERBST_DET_ERRB_OEN (UNDERBST_DET_FLAG) MAX_RT_I2C_ERRB_OEN (MAX_RT_I2C_ERR_FLAG) MAX_RT_GPI_ERRB_OEN (MAX_RT_GPI_ERR_FLAG) CC_CRC_ERRB_OEN (CC_CRC_ERR_FLAG) PRBS_ERRB_OEN (PRBS_ERR_FLAG)	0b0: Disable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link D error reporting (G1_D_ERR_FLAG) at ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
G1_C_ERR_OEN	6	Enables reporting of GMSL1 Link C errors (G1_C_ERR_FLAG) at ERRB pin. This controls a composite output to the ERRB pin. Individual error flag outputs to the ERRB pin are controlled by the following registers for Link C: DET_ERRB_OEN (DER_ERR_FLAG) EOM_ERRB_OEN (EOM_ERR_FLAG) LINE_CRC_ERRB_OEN (LINE_CRC_ERR_FLAG) UNDERBST_DET_ERRB_OEN (UNDERBST_DET_FLAG) MAX_RT_I2C_ERRB_OEN (MAX_RT_I2C_ERR_FLAG) MAX_RT_GPI_ERRB_OEN (MAX_RT_GPI_ERR_FLAG) CC_CRC_ERRB_OEN (CC_CRC_ERR_FLAG) PRBS_ERRB_OEN (PRBS_ERR_FLAG)	0b0: Disable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link C error reporting (G1_C_ERR_FLAG) at ERRB pin
G1_B_ERR_OEN	5	Enables reporting of GMSL1 Link B errors (G1_B_ERR_FLAG) at ERRB pin. This controls a composite output to the ERRB pin. Individual error flag outputs to the ERRB pin are controlled by the following registers for Link B: DET_ERRB_OEN (DER_ERR_FLAG) EOM_ERRB_OEN (EOM_ERR_FLAG) LINE_CRC_ERRB_OEN (LINE_CRC_ERR_FLAG) UNDERBST_DET_ERRB_OEN (UNDERBST_DET_FLAG) MAX_RT_I2C_ERRB_OEN (MAX_RT_I2C_ERR_FLAG) MAX_RT_GPI_ERRB_OEN (MAX_RT_GPI_ERR_FLAG) CC_CRC_ERRB_OEN (CC_CRC_ERR_FLAG) PRBS_ERRB_OEN (PRBS_ERR_FLAG)	0b0: Disable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link B error reporting (G1_B_ERR_FLAG) at ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
G1_A_ERR_OEN	4	Enables reporting of GMSL1 Link A errors (G1_A_ERR_FLAG) at ERRB pin. This controls a composite output to the ERRB pin. Individual error flag outputs to the ERRB pin are controlled by the following registers for Link A: DET_ERRB_OEN (DER_ERR_FLAG) EOM_ERRB_OEN (EOM_ERR_FLAG) LINE_CRC_ERRB_OEN (LINE_CRC_ERR_FLAG) UNDERBST_DET_ERRB_OEN (UNDERBST_DET_FLAG) MAX_RT_I2C_ERRB_OEN (MAX_RT_I2C_ERR_FLAG) MAX_RT_GPI_ERRB_OEN (MAX_RT_GPI_ERR_FLAG) CC_CRC_ERRB_OEN (CC_CRC_ERR_FLAG) PRBS_ERRB_OEN (PRBS_ERR_FLAG)	0b0: Disable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin 0b1: Enable GMSL1 Link A error reporting (G1_A_ERR_FLAG) at ERRB pin
LCRC_ERR_OEN	3	Enables reporting of video line CRC errors (LCRC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin 0b1: Enable video line CRC error reporting (LCRC_ERR_FLAG) at ERRB pin
VPRBS_ERR_OEN	2	Enables reporting of video PRBS errors (VPRBS_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin 0b1: Enable video PRBS error reporting (VPRBS_ERR_FLAG) at ERRB pin
REM_ERR_OEN	1	Enables reporting of remote error status (REM_ERR—0x2A) at ERRB pin.	0b0: Disable remote error status (REM_ERR) reporting at ERRB pin 0b1: Enable remote error status (REM_ERR) reporting at ERRB pin
FSYNC_ERR_OEN	0	Enables reporting of frame sync errors (FSYNC_ERR_FLAG—0x2A) at ERRB pin.	0b0: Disable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin 0b1: Enable frame sync error reporting (FSYNC_ERR_FLAG) at ERRB pin

INTR7 (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	G1_D_ERR_FLAG	G1_C_ERR_FLAG	G1_B_ERR_FLAG	G1_A_ERR_FLAG	LCRC_ERR_FLAG	VPRBS_ERR_FLAG	REM_ERR_FLAG	FSYNC_ERR_FLAG
Reset	0x0	0x0	0x0	0x0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
G1_D_ERR_FLAG	7	GMSL1 Link D Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error is detected. When PRBS test is not enabled, this flag is asserted when any of these conditions is true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xC0E)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication has been exceeded. 6. A CRC error is detected in PKTCC communication.	0b0: No error detected 0b1: Error detected
G1_C_ERR_FLAG	6	GMSL1 Link C Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error is detected. When PRBS test is not enabled, this flag is asserted when any of these conditions are true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xCOE)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication is exceeded. 6. A CRC error is detected in PKTCC communication.	0b0: No error detected 0b1: Error detected

BITFIELD	BITS	DESCRIPTION	DECODE
G1_B_ERR_FLAG	5	GMSL1 Link B Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error is detected. When PRBS test is not enabled, this flag is asserted when any of these conditions are true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xCOE)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication is exceeded. 6. A CRC error is detected in PKTCC communication.	0b0: No error detected 0b1: Error detected
G1_A_ERR_FLAG	4	GMSL1 Link A Error Flag When PRBS test is enabled, this bit is asserted if at least one PRBS error is detected. When PRBS test is not enabled, this flag is asserted when any of these conditions are true: 1. The number of detected decoding errors is greater than the detected error threshold (DET_ERR (0xB15) > DET_THR (0xCOE)). 2. The measured eye-opening is less than or equal to the eye-opening threshold (EOM_EYE_WIDTH (0xC1C) ≤ EOM_MIN_THR_G1 (0xB13)). 3. The adaptive EQ has detected an under boost. 4. A video line CRC error is detected. 5. The maximum retransmission count in PKTCC communication is exceeded. 6. A CRC error is detected in PKTCC communication.	0b0: No error detected 0b1: Error detected

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR_FLAG	3	Video Line CRC Error Flag Assert when a video line CRC error is detected.	0b0: No video line CRC error detected 0b1: Video line CRC error detected
VPRBS_ERR_FLAG	2	Video PRBS Error Flag Asserted when VPRBS_ERR (0x1D8) > 0.	0b0: VPRBS_ERR ≤ 0 0b1: VPRBS_ERR > 0
REM_ERR_FLAG	1	Receives remote side error status (inverse of remote side ERRB pin level).	0b0: No remote side error status received 0b1: Remote side error status received
FSYNC_ERR_FLAG	0	Frame Sync Error Flag Asserted when FSYNC_ERR_CNT (0x4B0) ≥ FSYNC_ERR_THR (0x4B1).	0b0: FSYNC_ERR_CNT < FSYNC_ERR_THR 0b1: FSYNC_ERR_CNT ≥ FSYNC_ERR_THR

INTR8 (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_OEN_D	IDLE_ERR_OEN_C	IDLE_ERR_OEN_B	IDLE_ERR_OEN_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_OEN_D	3	Enables reporting of idle word errors (IDLE_ERR_FLAG_D) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_D) at ERRB pin
IDLE_ERR_OEN_C	2	Enables reporting of idle word errors (IDLE_ERR_FLAG_C) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_C) at ERRB pin
IDLE_ERR_OEN_B	1	Enables reporting of idle word errors (IDLE_ERR_FLAG_B) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_B) at ERRB pin
IDLE_ERR_OEN_A	0	Enables reporting of idle word errors (IDLE_ERR_FLAG_A) at ERRB pin.	0b0: Disable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin 0b1: Enable idle word error reporting (IDLE_ERR_FLAG_A) at ERRB pin

INTR9 (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	IDLE_ERR_FLAG_D	IDLE_ERR_FLAG_C	IDLE_ERR_FLAG_B	IDLE_ERR_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type					Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_FLAG_D	3	Idle Word Error Flag D Asserted when IDLE_ERR_D (0x3C) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_D < DEC_ERR_THR 0b1: IDLE_ERR_D ≥ DEC_ERR_THR
IDLE_ERR_FLAG_C	2	Idle Word Error Flag C Asserted when IDLE_ERR_C (0x3B) ≥ DEC_ERR_THR.	0b0: IDLE_ERR_C < DEC_ERR_THR 0b1: IDLE_ERR_C ≥ DEC_ERR_THR
IDLE_ERR_FLAG_B	1	Idle Word Error Flag B Asserted when IDLE_ERR_B (x3A0 ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_B < DEC_ERR_THR 0b1: IDLE_ERR_B ≥ DEC_ERR_THR
IDLE_ERR_FLAG_A	0	Idle Word Error Flag A Asserted when IDLE_ERR_A (0x39) ≥ DEC_ERR_THR (0x23).	0b0: IDLE_ERR_A < DEC_ERR_THR 0b1: IDLE_ERR_A ≥ DEC_ERR_THR

INTR10 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	RT_CNT_OEN_D	RT_CNT_OEN_C	RT_CNT_OEN_B	RT_CNT_OEN_A	MAX_RT_OEN_D	MAX_RT_OEN_C	MAX_RT_OEN_B	MAX_RT_OEN_A
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_OEN_D	7	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_D) at ERRB pin
RT_CNT_OEN_C	6	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_C) at ERRB pin
RT_CNT_OEN_B	5	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_B) at ERRB pin
RT_CNT_OEN_A	4	Enables reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ retransmission event flag (RT_CNT_FLAG_A) at ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_OEN_D	3	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_D) at ERRB pin
MAX_RT_OEN_C	2	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_C) at ERRB pin
MAX_RT_OEN_B	1	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_B) at ERRB pin
MAX_RT_OEN_A	0	Enables reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A—0x2E) at ERRB pin.	0b0: Disable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin 0b1: Enable reporting of combined ARQ maximum retransmission limit error flag (MAX_RT_FLAG_A) at ERRB pin

INTR11 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	RT_CNT_FLAG_D	RT_CNT_FLAG_C	RT_CNT_FLAG_B	RT_CNT_FLAG_A	MAX_RT_FLAG_D	MAX_RT_FLAG_C	MAX_RT_FLAG_B	MAX_RT_FLAG_A
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG_D	7	Combined ARQ Retransmission Event Flag D Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_D (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FLAG_C	6	Combined ARQ Retransmission Event Flag C Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_C (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
RT_CNT_FLAG_B	5	Combined ARQ Retransmission Event Flag B Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_B (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT_FLAG_A	4	Combined ARQ Retransmission Event Flag A Asserted when any of the selected channels have done at least one ARQ retransmission. Selection is done by each channel's RT_CNT_OEN_A (0x2D) register bit.	0b0: None of the selected channels have done at least one ARQ retransmission 0b1: One or more of the selected channels has done at least one ARQ retransmission
MAX_RT_FLAG_D	3	Combined ARQ Maximum Retransmission Limit Error Flag D Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_D (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_C	2	Combined ARQ Maximum Retransmission Limit Error Flag C Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_C (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_B	1	Combined ARQ Maximum Retransmission Limit Error Flag B Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_B (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit
MAX_RT_FLAG_A	0	Combined ARQ Maximum Retransmission Limit Error Flag A Asserted when any of the selected channel's ARQ retransmission limit is reached. Selection is done by each channel's MAX_RT_ERR_OEN_A (0x2D) register bit.	0b0: None of the selected channels have reached the maximum retry limit 0b1: One or more of the selected channels has reached the maximum retry limit

INTR12 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	ERR_TX_EN	–	–	ERR_TX_ID[4:0]				
Reset	0b1	–	–	0x1F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_TX_EN	7	Transmits local error status (inverse of ERRB pin level) to remote side through GPIO channel.	0b0: Do not transmit local error status to remote side through GPIO channel 0b1: Transmit local error status to remote side through GPIO channel
ERR_TX_ID	4:0	GPIO ID used for transmitting ERR_TX.	0bXXXXX: GPIO ID used for transmitting ERR_TX

INTR13 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_A	ERR_RX_RECVED_A	–	ERR_RX_ID_A[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_A	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link A.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link A 0b1: Receive remote error status through GPIO channel for GMSL2 Link A
ERR_RX_RECVED_A	6	Received ERR_RX value for Link A	0b0: ERR_RX value for Link A received 0b1: ERR_RX value for Link A not received
ERR_RX_ID_A	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link A.	0bXXXXX: GPIO ID used for receiving ERR_RX Link A

INTR14 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_B	ERR_RX_RECVED_B	–	ERR_RX_ID_B[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_B	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link B.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link B 0b1: Receive remote error status through GPIO channel for GMSL2 Link B
ERR_RX_RECVED_B	6	Received ERR_RX value for link B	0x0: ERR_RX value for Link B received 0x1: ERR_RX value for Link B not received
ERR_RX_ID_B	4:0	GPIO ID used for receiving ERR_RX for GMSL2 Link B.	0bXXXXX: GPIO ID used for receiving ERR_RX Link B

INTR15 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_C	ERR_RX_RECVED_C	–	ERR_RX_ID_C[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_C	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link C.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link C 0b1: Receive remote error status through GPIO channel for GMSL2 Link C

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_RECVED_C	6	Received ERR_RX value for Link C	0x0: ERR_RX value for Link C received 0x1: ERR_RX value for Link C not received
ERR_RX_ID_C	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link C	0bXXXXX: GPIO ID used for receiving ERR_RX link C

INTR16 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	ERR_RX_EN_D	ERR_RX_RECVED_D	–	ERR_RX_ID_D[4:0]				
Reset	0b1	0b1	–	0x1F				
Access Type	Write, Read	Write, Read	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_RX_EN_D	7	Receives remote error status (inverse of ERRB pin level) through GPIO channel for GMSL2 Link D.	0b0: Do not receive remote error status through GPIO channel for GMSL2 Link D 0b1: Receive remote error status through GPIO channel for GMSL2 Link D
ERR_RX_RECVED_D	6	Received ERR_RX value for Link D	0x0: ERR_RX value for Link D received 0x1: ERR_RX value for Link D not received
ERR_RX_ID_D	4:0	GPIO ID used for receiving ERR_RX for GMSL2 link D	0bXXXXX: GPIO ID used for receiving ERR_RX link D

CNT0 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_A	7:0	The number of decoding (disparity) errors detected at Link A Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link A decoding errors detected

CNT1 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_B	7:0	The number of decoding (disparity) errors detected at Link B Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link B decoding errors detected

CNT2 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_C	7:0	The number of decoding (disparity) errors detected at Link C Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link C decoding errors detected

CNT3 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	DEC_ERR_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
DEC_ERR_D	7:0	The number of decoding (disparity) errors detected at Link D Reset after reading or with the rising edge of LOCK.	0xXX: Number of Link D decoding errors detected

CNT4 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_A[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_A	7:0	The number of idle word errors detected at Link A Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT5 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_B[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_B	7:0	The number of idle word errors detected at Link B Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT6 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_C[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_C	7:0	The number of idle word errors detected at Link C Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

CNT7 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	IDLE_ERR_D[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
IDLE_ERR_D	7:0	Number of idle word errors detected at Link D Reset after reading or with the rising edge of LOCK.	0xXX: Number of idle word errors detected

VID_PXL_CRC_ERR_VIDEOMASK_OEN (0x44)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_MASKED_3_OEN	VIDEO_MASKED_2_OEN	VIDEO_MASKED_1_OEN	VIDEO_MASKED_0_OEN	VID_PXL_CRC_ERR_OEN_D	VID_PXL_CRC_ERR_OEN_C	VID_PXL_CRC_ERR_OEN_B	VID_PXL_CRC_ERR_OEN_A
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_MASKED_3_OEN	7	Enable Video Masked 3 status on ERRB	0x0: Video Masked 3 status disabled on ERRB pin 0x1: Video Masked 3 status enabled on ERRB pin
VIDEO_MASKED_2_OEN	6	Enable Video Masked 2 status on ERRB	0x0: Video Masked 2 status disabled on ERRB pin 0x1: Video Masked 2 status enabled on ERRB pin
VIDEO_MASKED_1_OEN	5	Enable Video Masked 1 status on ERRB	0x0: Video Masked 1 status disabled on ERRB pin 0x1: Video Masked 1 status enabled on ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_MASKED_0_OEN	4	Enable Video Masked 0 status on ERRB	0x0: Video Masked 0 status disabled on ERRB pin 0x1: Video Masked 0 status enabled on ERRB pin
VID_PXL_CRC_ERR_OEN_D	3	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_C	2	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_B	1	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output
VID_PXL_CRC_ERR_OEN_A	0	Video Pixel CRC Error Counter Interrupt Output Enable	0b0: Disable video pixel CRC error counter interrupt output 0b1: Enable video pixel CRC error counter interrupt output

VID_PXL_CRC_VIDEOMASK_INT_FLAG (0x45)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_MASKED_3_FLAG	VIDEO_MASKED_2_FLAG	VIDEO_MASKED_1_FLAG	VIDEO_MASKED_0_FLAG	VID_PXL_CRC_ERR_D	VID_PXL_CRC_ERR_C	VID_PXL_CRC_ERR_B	VID_PXL_CRC_ERR_A
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_MASKED_3_FLAG	7	Sticky status value for Video Masked 3. Flag will be set if any of Video Pipes 0-3 apart of 4WxH or Wx4H synchronous aggregation of Controller 3 lose video lock. See video_masked registers in MIPI_TX_x registers to determine which Video Pipe was masked.	0x0: Video Pipe 3 video output has not been masked 0x1: Video Pipe 3 video output has been masked
VIDEO_MASKED_2_FLAG	6	Sticky status value for Video Masked 2. Flag will be set if any of Video Pipes 0-3 apart of 4WxH or Wx4H synchronous aggregation of Controller 2 lose video lock. See video_masked registers in MIPI_TX_x registers to determine which Video Pipe was masked.	0x0: Video Pipe 2 video output has not been masked 0x1: Video Pipe 2 video output has been masked
VIDEO_MASKED_1_FLAG	5	Sticky status value for Video Masked 1. Flag will be set if any of Video Pipes 0-3 apart of 4WxH or Wx4H synchronous aggregation of Controller 1 lose video lock. See video_masked registers in MIPI_TX_x registers to determine which Video Pipe was masked.	0x0: Video Pipe 1 video output has not been masked 0x1: Video Pipe 1 video output has been masked

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_MASKED_0_FLAG	4	Sticky status value for Video Masked 0. Flag will be set if any of Video Pipes 0-3 apart of 4WxH or Wx4H synchronous aggregation of Controller 0 lose video lock. See video_masked registers in MIPI_TX_x registers to determine which Video Pipe was masked.	0x0: Video Pipe 0 video output has not been masked 0x1: Video Pipe 0 video output has been masked
VID_PXL_CRC_ERR_D	3	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_C	2	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_B	1	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected
VID_PXL_CRC_ERR_A	0	Video Pixel CRC Error Counter Interrupt	0b0: No video pixel CRC error counter interrupt detected 0b1: Video pixel CRC error counter interrupt detected

PWR_STATUS_OEN (0x48)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_INT_OEN	RSVD	–	RSVD	–	–	RSVD[1:0]	
Reset	0x1	0x1	–	0x0	–	–	0x1	
Access Type	Write, Read		–		–	–		

BITFIELD	BITS	DESCRIPTION
VDDBAD_INT_OEN	7	Enable reporting of VDDBAD interrupt (VDDBAD_INT_FLAG) at ERRB pin

PWR_STATUS_OV_FLAG (0x49)

BIT	7	6	5	4	3	2	1	0
Field	VDDBAD_INT_FLAG	RSVD	RSVD	RSVD	CMP_STATUS_VDD_OV	CMP_STATUS_VDD12_OV	CMP_STATUS_vddio_ov	CMP_STATUS_VDD18_OV
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All				Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VDDBAD_INT_FLAG	7	Combined VDDBAD indicator	
CMP_STATUS_VDD_OV	3	VDD Comparator Status	0x0: VDD operating in normal range 0x1: VDD measured above overvoltage comparator threshold

BITFIELD	BITS	DESCRIPTION	DECODE
CMP_STATUS_VDD12_OV	2		0x0: VTERM operating in normal range 0x1: VTERM measured above overvoltage comparator threshold
CMP_STATUS_vddio_ov	1		0x0: VDDIO operating in normal range 0x1: VDDIO measured above overvoltage comparator threshold
CMP_STATUS_VDD18_OV	0		0x0: VDD18 operating in normal range 0x1: VDD18 measured above overvoltage comparator threshold

VDDCMP_MASK (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_OEN	–	CMP_VTERM_MASK	VDDCMP_MASK[4:0]				
Reset	0x1	–	0x1	0x07				
Access Type	Write, Read	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
VDDCMP_INT_OEN	7	Enables reporting of V_{DD} comparator interrupt (VDDCMP_INT_FLAG) at ERRB pin. See registers VDDCMP_MASK, CMP_STATUS, and VDDCMP_INT_FLAG
CMP_VTERM_MASK	5	Enable V_{TERM} voltage comparator status to drive VDDCMP_INT_FLAG error flag and ERRB pin output. See CMP_VTERM_STATUS register. Program to zero to mask status contribution to VDDCMP_INT_FLAG and ERRB pin. Program to one to enable status contribution to VDDCMP_INT_FLAG and ERRB pin.
VDDCMP_MASK	4:0	Select which voltage comparator status bits are masked from contributing to the VDDCMP_INT_FLAG error flag and ERRB pin. See the CMP_STATUS register field. Programming a bit to zero will mask the corresponding bit in the CMP_STATUS register field and prevent it from contributing to the VDDCMP_INT_FLAG. Note that this does not mask the CMP_STATUS register field; it only masks the contribution to the VDDCMP_INT_FLAG and ERRB pin output. 0 - Mask corresponding CMP_STATUS bit contribution to VDDCMP_INT_FLAG and ERRB 1 - Enable corresponding CMP_STATUS bit contribution to VDDCMP_INT_FLAG and ERRB See the VDDCMP_INT_FLAG and VDDCMP_INT_OEN register fields.

VDDCMP_STATUS_FLAG (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	VDDCMP_INT_FLAG	–	CMP_VTERM_STATUS	–	–	–	–	–
Reset	0x0	–	0x0	–	–	–	–	–
Access Type	Read Clears All	–	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
VDDCMP_INT_FLAG	7	Combined V_{DD} comparator output. See CMP_STATUS and VDDCMP_MASK registers.
CMP_VTERM_STATUS	5	Power manager V_{TERM} comparator status. Latched low when switched V_{TERM} supply < 1V. Cleared when the CMP_STATUS word (register 0x12) is read and the switched V_{TERM} supply is > 1V.

DEV_REV (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DEV_REV[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
DEV_REV	3:0	Device Revision	0x0: Revision number

EFUSE_CTRL (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	–	EFUSE_CRC_ERR_RST_OS	EFUSE_CRC_ERR_RST	EFUSE_CRC_ERR_OEN	–	–	–	–
Reset	–	0b0	0b0	0b1	–	–	–	–
Access Type	–	Write Clears All, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EFUSE_CRC_ERR_RST_OS	6	Resets EFUSE CRC Error output. Write 1 to reset the EFUSE CRC Error output. This register is self clearing.	0x0: normal operation 0x1: Reset eFuse CRC Error Output (self-clearing)
EFUSE_CRC_ERR_RST	5	Resets EFUSE CRC Error output. Write 1 to reset the EFUSE CRC Error output. Write 0 to clear the reset request. This register is not self clearing.	0x0: clear eFuse CRC Error Output Reset 0x1: Reset eFuse CRC Error Output (NOT self-clearing)
EFUSE_CRC_ERR_OEN	4	Enable reporting efuse CRC at ERRB pin	0x0: Efuse CRC error report not enabled at ERRB pin 0x1: Efuse CRC error report enabled at ERRB pin

EFUSE_CRC_ERR (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	EFUSE_CRC_ERR	–	–	–	–
Reset	–	–	–		–	–	–	–
Access Type	–	–	–	Read Only	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
EFUSE_CRC_ERR	4		0x0: Efuse CRC error not reported at ERRB pin 0x1: Efuse CRC error observed at ERRB pin

CFGH_VIDEO_CRC0 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_A_B[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_A_B	7:0	Received Packet CRC Enable for Ports A and B Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet. Bit 0: RX_CRC_EN_A_VIDEO_X Bit 1: RX_CRC_EN_A_VIDEO_Y Bit 2: RX_CRC_EN_A_VIDEO_Z Bit 3: RX_CRC_EN_A_VIDEO_U Bit 4: RX_CRC_EN_B_VIDEO_X Bit 5: RX_CRC_EN_B_VIDEO_Y Bit 6: RX_CRC_EN_B_VIDEO_Z Bit 7: RX_CRC_EN_B_VIDEO_U	0bXXXXXXX0: No CRC on received packets—RX_CRC_EN_A_VIDEO_X 0bXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_A_VIDEO_X 0bXXXXXX0X: No CRC on received packets—RX_CRC_EN_A_VIDEO_Y 0bXXXXXX1X: Received packets have CRC and checking is enabled— RX_CRC_EN_A_VIDEO_Y … … … 0b0XXXXXXX: No CRC on received packets—RX_CRC_EN_B_VIDEO_U 0b1XXXXXXX: Received packets have CRC and checking is enabled— RX_CRC_EN_B_VIDEO_U

CFGH_VIDEO_CRC1 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	RX_CRC_EN_C_D[7:0]							
Reset	0b0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_C_D	7:0	Received Packet CRC Enable for Ports C and D Each bit enables CRC for one pipe within a GMSL link as described below. Setting a given bit indicates that packets received at the corresponding port/pipe have appended CRC and CRC checking must be performed at each packet. Bit 0: RX_CRC_EN_C_VIDEO_X Bit 1: RX_CRC_EN_C_VIDEO_Y Bit 2: RX_CRC_EN_C_VIDEO_Z Bit 3: RX_CRC_EN_C_VIDEO_U Bit 4: RX_CRC_EN_D_VIDEO_X Bit 5: RX_CRC_EN_D_VIDEO_Y Bit 6: RX_CRC_EN_D_VIDEO_Z Bit 7: RX_CRC_EN_D_VIDEO_U	0bXXXXXXX0: No CRC on received packets—RX_CRC_EN_C_VIDEO_X 0bXXXXXXX1: Received packets have CRC and checking is enabled—RX_CRC_EN_C_VIDEO_X 0bXXXXXX0X: No CRC on received packets—RX_CRC_EN_C_VIDEO_Y 0bXXXXXX1X: Received packets have CRC and checking is enabled— RX_CRC_EN_C_VIDEO_Y ... ... 0b0XXXXXXX: No CRC on received packets—RX_CRC_EN_D_VIDEO_U 0b1XXXXXXX: Received packets have CRC and checking is enabled— RX_CRC_EN_D_VIDEO_U

TR0 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/10 as a percentage of total link bandwidth.	0bXXXXXX: Channel base-bandwidth value

TR2 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x76)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR2 (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR3 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

TR0 (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/ 10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmit limit. ARQ will stop retransmission after reaching the limit for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—0xA7) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0xA7) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT—0xA6) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached

BITFIELD	BITS	DESCRIPTION	DECODE
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0xAE)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_B	6:4	Maximum retransmit limit. ARQ will stop retransmission after reaching the limit for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B—0xAF) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0xAF) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xAF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B—0xAE) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0xB6)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_C	6:4	Maximum retransmit limit. ARQ will stop retransmission after reaching the limit for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0xB7) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0xB7) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xB7)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C—0xB6) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

TR0 (0xB8)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		RSVD[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port.	0b0: Transmit CRC disabled 0b1: Transmit CRC enabled
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Receive CRC disabled 0b1: Receive CRC enabled
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests.	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority

TR1 (0xB9)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor.	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0xBB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0xBC)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Receives packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0xBE)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_D	6:4	Maximum retransmit limit. ARQ will stop retransmission after reaching the limit for a single packet.	0bXXX: Maximum retransmit limit
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D—0xBF) for this channel at ERRB pin	0b0: ARQ maximum retransmit limit errors reporting at ERRB pin disabled 0b1: ARQ maximum retransmit limit errors reporting at ERRB pin enabled
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0xBF) of this channel is greater than 0.	0b0: ARQ retransmission count reporting at ERRB pin disabled 0b1: ARQ retransmission count reporting at ERRB pin enabled

ARQ2 (0xBF)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D—0xBE) for one packet in this channel.	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel.	0bXXXXXXX: Count of retransmissions for this channel

I2C_7 (0xC7)

BIT	7	6	5	4	3	2	1	0
Field	I2C_REGSLV_1_TIMED_OUT	I2C_INTREG_SLV_1_TO[2:0]			I2C_REGSLV_0_TIMED_OUT	I2C_INTREG_SLV_0_TO[2:0]		
Reset	0x0	0x6			0x0	0x6		
Access Type	Read Only	Write, Read			Read Only	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_REGSLV_1_TIMED_OUT	7	Internal I^2C-to-register slave for Port 1 has timed out while waiting for the master or the internal register access FSM.	0b0: Internal I^2C-to-register slave for Port 1 has not timed out 0b1: Internal I^2C-to-register slave for Port 1 has timed out
I2C_INTREG_SLV_1_TO	6:4	I^2C-to-Internal Register Slave 1 Timeout Setting Internal register I^2C Slave 1 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves I^2C Port 1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled
I2C_REGSLV_0_TIMED_OUT	3	Internal I^2C-to-register slave for Port 0 has timed out while waiting for the master or the internal register access FSM.	0b0: Internal I^2C-to-register slave for Port 0 has not timed out 0b1: Internal I^2C-to-register slave for Port 0 has timed out
I2C_INTREG_SLV_0_TO	2:0	I^2C-to-Internal Register Slave 0 Timeout Setting Internal register I^2C Slave 0 times out after the configured duration if it does not receive any response from the external master or internal register FSM. This slave serves I^2C Port 0.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

REG0 (0xE0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PU_LF3	PU_LF2	PU_LF1	PU_LF0
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PU_LF3	3	Power up Line Fault monitor 3	0b0: Line fault monitor 3 disabled 0b1: Line fault monitor 3 enabled
PU_LF2	2	Power up Line Fault monitor 2	0b0: Line fault monitor 2 disabled 0b1: Line fault monitor 2 enabled
PU_LF1	1	Power up Line Fault monitor 1	0b0: Line fault monitor 1 disabled 0b1: Line fault monitor 1 enabled
PU_LF0	0	Power up Line Fault monitor 0	0b0: Line fault monitor 0 disabled 0b1: Line fault monitor 0 enabled

REG1 (0xE1)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_1[2:0]			–	LF_0[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_1	6:4	Line Fault status of wire connected to LMN1 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short
LF_0	2:0	Line Fault status of wire connected to LMN0 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

REG2 (0xE2)

BIT	7	6	5	4	3	2	1	0
Field	–	LF_3[2:0]			–	LF_2[2:0]		
Reset	–	0x2			–	0x2		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
LF_3	6:4	Line Fault status of wire connected to LMN3 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

BITFIELD	BITS	DESCRIPTION	DECODE
LF_2	2:0	Line Fault status of wire connected to LMN2 pin	0b000: Short to battery 0b001: Short to GND 0b010: Normal Operation 0b011: Line Open 0b1XX: Line-to-line short

REG5 (0xE5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	LFLT_INT_FLAG[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Clears All			

BITFIELD	BITS	DESCRIPTION	DECODE
LFLT_INT_FLAG	3:0	Line-Fault Error Flag Indicators	0x0: Gets set to 1 when (!mask_lf0 && pu_lf0 && (LF_0 != 3'b010)). Read clears 0x1: Gets set to 1 when (!mask_lf1 && pu_lf1 && (LF_1 != 3'b010)). Read clears 0x2: Gets set to 1 when (!mask_lf2 && pu_lf2 && (LF_2 != 3'b010)). Read clears 0x3: Gets set to 1 when (!mask_lf3 && pu_lf3 && (LF_3 != 3'b010)). Read clears

REG6 (0xE6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MASK_LF3	MASK_LF2	MASK_LF1	MASK_LF0
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MASK_LF3	3	Mask Line Fault monitor 3 Interrupt	0b0: Line fault monitor 3 interrupt enabled 0b1: Line fault monitor 3 interrupt masked
MASK_LF2	2	Mask Line Fault monitor 2 Interrupt	0b0: Line fault monitor 2 interrupt enabled 0b1: Line fault monitor 2 interrupt masked
MASK_LF1	1	Mask Line Fault monitor 1 Interrupt	0b0: Line fault monitor 1 interrupt enabled 0b1: Line fault monitor 1 interrupt masked
MASK_LF0	0	Mask Line Fault monitor 0 Interrupt	0b0: Line fault monitor 0 interrupt enabled 0b1: Line fault monitor 0 interrupt masked

VIDEO_PIPE_SEL_0 (0xF0)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_1[3:0]				VIDEO_PIPE_SEL_0[3:0]			
Reset	0x6				0x2			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_1	7:4	Video Pipe 1 Input Selection Control Bits [7:6]: GMSL2 Phy Link selection for Pipe 1 Bits [5:4]: Input Pipe selection for Pipe 1	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_0	3:0	Video Pipe 0 Input Selection Control Bits [3:2]: GMSL2 Phy Link selection for Pipe 0 Bits [1:0]: Input Pipe selection for Pipe 0	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_SEL_1 (0xF1)

BIT	7	6	5	4	3	2	1	0
Field	VIDEO_PIPE_SEL_3[3:0]				VIDEO_PIPE_SEL_2[3:0]			
Reset	0xe				0xa			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
VIDEO_PIPE_SEL_3	7:4	Video Pipe 3 Selection Bits [7:6]: GMSL2 Phy Link selection for Pipe 3 Bits [5:4]: Input Pipe selection for Pipe 3	Bits [7:6] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [5:4] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U
VIDEO_PIPE_SEL_2	3:0	Video Pipe 2 Selection Bits [3:2]: GMSL2 Phy Link selection for Pipe 2 Bits [1:0]: Input Pipe selection for Pipe 2	Bits [3:2] 0b00: GMSL2 PHY A 0b01: GMSL2 PHY B 0b10: GMSL2 PHY C 0b11: GMSL2 PHY D Bits [1:0] 0b00: Pipe X 0b01: Pipe Y 0b10: Pipe Z 0b11: Pipe U

VIDEO_PIPE_EN (0xF4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	STREAM_SEL_ALL	VIDEO_PIPE_EN[3:0]			
Reset	–	–	–	0x1	0xF			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
STREAM_SEL_ALL	4	When set to a 1, overrides VIDEO_PIPE_SEL_*[1:0] select bits such that all X,Y,Z, and U streams are selected, not just one. When cleared to 0, VIDEO_PIPE_SEL_0[1:0] will select which stream to pass to pipe 0.	0x0: Legacy (MAX96712) mode 0x1: Select all streams (X,Y,Z and/or U)
VIDEO_PIPE_EN	3:0	Video Pipe Enable Register	0bXXXXXXX0: Disable Pipe 0 0bXXXXXXX1: Enable Pipe 0 0bXXXXXX0X: Disable Pipe 1 0bXXXXXX1X: Enable Pipe 1 0bXXXXX0XX: Disable Pipe 2 0bXXXXX1XX: Enable Pipe 2 0bXXXX0XXX: Disable Pipe 3 0bXXXX1XXX: Enable Pipe 3

HVD_GPIO_CTRL_EN (0xFA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HVD_OUT_EN[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
HVD_OUT_EN	3:0	This register field controls which (if any) of the VSYNC/HSYNC/DE GPIO are enabled. Desired output signals are selected using the HVD_HS_SEL*, HVD_VS_SEL*, HVD_DE_SEL*, and HVD_OUT_SEL registers When Bit 0 = 1 Enables HDV GPIO on MFP1 When Bit 1 = 1 Enables HDV GPIO on MFP3 When Bit 2 = 1 Enables HDV GPIO on MFP7 When Bit 3 = 1 Enables HDV GPIO on MFP8	0x0: Disable all HVD GPIO 0x1: Enable only HVD GPIO on MFP1, all others disabled 0x2: Enable only HVD GPIO on MFP3, all others disabled 0x3: Enable HVD GPIO on MFP1 and MFP3, all others disabled 0x4: Enable only HVD GPIO on MFP7, all others disabled 0x5: Enable HVD GPIO on MFP1 and MFP7, all others disabled 0x6: Enable HVD GPIO on MFP3 and MFP7, all others disabled 0x7: Enable HVD GPIO on MFP1, MFP3, and MFP7, all others disabled 0x8: Enable only HVD GPIO on MFP8, all others disabled 0x9: Enable HVD GPIO on MFP1 and MFP8 0xA: Enable HVD GPIO on MFP3 and MFP8, all others disabled 0xB: Enable HVD GPIO on MFP1, MFP3 and MFP8, all others disabled 0xC: Enable HVD GPIO on MFP7 and MFP8, all others disabled 0xD: Enable HVD GPIO on MFP1, MFP7 and MFP8, all others disabled 0xE: Enable HVD GPIO on MFP3, MFP7, and MFP8, all others disabled 0xF: Enable HVD GPIO on MFP1, MFP3, MFP7, and MFP8, all others disabled

HVD_GPIO_CTRL_HS (0xFB)

BIT	7	6	5	4	3	2	1	0
Field	HVD_HS_SEL3[1:0]		HVD_HS_SEL2[1:0]		HVD_HS_SEL1[1:0]		HVD_HS_SEL0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
HVD_HS_SEL3	7:6	Selects which Video Pipe HS Sync to Output on MFP8 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - HS Sync for Video Pipe 0 2'b01 - HS Sync for Video Pipe 1 2'b10 - HS Sync for Video Pipe 2 2'b11 - HS Sync for Video Pipe 3
HVD_HS_SEL2	5:4	Selects which Video Pipe HS Sync to Output on MFP7 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - HS Sync for Video Pipe 0 2'b01 - HS Sync for Video Pipe 1 2'b10 - HS Sync for Video Pipe 2 2'b11 - HS Sync for Video Pipe 3

BITFIELD	BITS	DESCRIPTION
HVD_HS_SEL1	3:2	Selects which Video Pipe HS Sync to Output on MFP3 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - HS Sync for Video Pipe 0 2'b01 - HS Sync for Video Pipe 1 2'b10 - HS Sync for Video Pipe 2 2'b11 - HS Sync for Video Pipe 3
HVD_HS_SEL0	1:0	Selects which Video Pipe HS Sync to Output on MFP1 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - HS Sync for Video Pipe 0 2'b01 - HS Sync for Video Pipe 1 2'b10 - HS Sync for Video Pipe 2 2'b11 - HS Sync for Video Pipe 3

HVD_GPIO_CTRL_VS (0xFC)

BIT	7	6	5	4	3	2	1	0
Field	HVD_VS_SEL3[1:0]		HVD_VS_SEL2[1:0]		HVD_VS_SEL1[1:0]		HVD_VS_SEL0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
HVD_VS_SEL3	7:6	Selects which Video Pipe VS Sync to Output on MFP8 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - VS Sync for Video Pipe 0 2'b01 - VS Sync for Video Pipe 1 2'b10 - VS Sync for Video Pipe 2 2'b11 - VS Sync for Video Pipe 3
HVD_VS_SEL2	5:4	Selects which Video Pipe VS Sync to Output on MFP7 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - VS Sync for Video Pipe 0 2'b01 - VS Sync for Video Pipe 1 2'b10 - VS Sync for Video Pipe 2 2'b11 - VS Sync for Video Pipe 3
HVD_VS_SEL1	3:2	Selects which Video Pipe VS Sync to Output on MFP3 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - VS Sync for Video Pipe 0 2'b01 - VS Sync for Video Pipe 1 2'b10 - VS Sync for Video Pipe 2 2'b11 - VS Sync for Video Pipe 3
HVD_VS_SEL0	1:0	Selects which Video Pipe VS Sync to Output on MFP1 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - VS Sync for Video Pipe 0 2'b01 - VS Sync for Video Pipe 1 2'b10 - VS Sync for Video Pipe 2 2'b11 - VS Sync for Video Pipe 3

HVD_GPIO_CTRL_DE (0xFD)

BIT	7	6	5	4	3	2	1	0
Field	HVD_DE_SEL3[1:0]		HVD_DE_SEL2[1:0]		HVD_DE_SEL1[1:0]		HVD_DE_SEL0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
HVD_DE_SEL3	7:6	Selects which Video Pipe DE to Output on MFP8 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - DE Sync for Video Pipe 0 2'b01 - DE Sync for Video Pipe 1 2'b10 - DE Sync for Video Pipe 2 2'b11 - DE Sync for Video Pipe 3
HVD_DE_SEL2	5:4	Selects which Video Pipe DE to Output on MFP7 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - DE Sync for Video Pipe 0 2'b01 - DE Sync for Video Pipe 1 2'b10 - DE Sync for Video Pipe 2 2'b11 - DE Sync for Video Pipe 3
HVD_DE_SEL1	3:2	Selects which Video Pipe DE to Output on MFP3 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - DE Sync for Video Pipe 0 2'b01 - DE Sync for Video Pipe 1 2'b10 - DE Sync for Video Pipe 2 2'b11 - DE Sync for Video Pipe 3
HVD_DE_SEL0	1:0	Selects which Video Pipe DE to Output on MFP1 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - DE Sync for Video Pipe 0 2'b01 - DE Sync for Video Pipe 1 2'b10 - DE Sync for Video Pipe 2 2'b11 - DE Sync for Video Pipe 3

HVD_GPIO_CTRL_SEL (0xFE)

BIT	7	6	5	4	3	2	1	0
Field	HVD_OUT_SEL3[1:0]		HVD_OUT_SEL2[1:0]		HVD_OUT_SEL1[1:0]		HVD_OUT_SEL0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
HVD_OUT_SEL3	7:6	Selects Signal type, VSYNC, HSYNC, or DE to be output on MFP8. Using the HVD_HS_SEL*, HVD_VS_SEL*, and HVD_DE_SEL* registers, users can select one of any of the video pipe HSYNC, VSYNC, or DE signals to be output on MFP8. 2'b00 - Output HSYNC selected by HVD_HS_SEL3 on MFP8 2'b01 - Output VSYNC selected by HVD_VS_SEL3 on MFP8 2'b10 - Output DE selected by HVD_DE_SEL3 on MFP8 2'b11 - Output TX Start selected by HVD_ST_SEL3 on MFP8

BITFIELD	BITS	DESCRIPTION
HVD_OUT_SEL2	5:4	Selects Signal type, VSYNC, HSYNC, or DE to be output on MFP7. Using the HVD_HS_SEL*, HVD_VS_SEL*, and HVD_DE_SEL* registers, users can select one of any of the video pipe HSYNC, VSYNC, or DE signals to be output on MFP7. 2'b00 - Output HSYNC selected by HVD_HS_SEL2 on MFP7 2'b01 - Output VSYNC selected by HVD_VS_SEL2 on MFP7 2'b10 - Output DE selected by HVD_DE_SEL2 on MFP7 2'b11 - Output TX Start selected by HVD_ST_SEL2 on MFP7
HVD_OUT_SEL1	3:2	Selects Signal type, VSYNC, HSYNC, or DE to be output on MFP3. Using the HVD_HS_SEL*, HVD_VS_SEL*, and HVD_DE_SEL* registers, users can select one of any of the video pipe HSYNC, VSYNC, or DE signals to be output on MFP3. 2'b00 - Output HSYNC selected by HVD_HS_SEL1 on MFP3 2'b01 - Output VSYNC selected by HVD_VS_SEL1 on MFP3 2'b10 - Output DE selected by HVD_DE_SEL1 on MFP3 2'b11 - Output TX Start selected by HVD_ST_SEL1 on MFP3
HVD_OUT_SEL0	1:0	Selects Signal type, VSYNC, HSYNC, or DE to be output on MFP1. Using the HVD_HS_SEL*, HVD_VS_SEL*, and HVD_DE_SEL* registers, users can select one of any of the video pipe HSYNC, VSYNC, or DE signals to be output on MFP1. 2'b00 - Output HSYNC selected by HVD_HS_SEL0 on MFP1 2'b01 - Output VSYNC selected by HVD_VS_SEL0 on MFP1 2'b10 - Output DE selected by HVD_DE_SEL0 on MFP1 2'b11 - Output TX Start selected by HVD_ST_SEL0 on MFP1

HVD_GPIO_CTRL_ST (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	HVD_ST_SEL3[1:0]		HVD_ST_SEL2[1:0]		HVD_ST_SEL1[1:0]		HVD_ST_SEL0[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
HVD_ST_SEL3	7:6	Selects which Video Pipe TX Start to Output on MFP8 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - TX Start for Video Pipe 0 2'b01 - TX Start for Video Pipe 1 2'b10 - TX Start for Video Pipe 2 2'b11 - TX Start for Video Pipe 3
HVD_ST_SEL2	5:4	Selects which Video Pipe TX Start to Output on MFP7 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - TX Start for Video Pipe 0 2'b01 - TX Start for Video Pipe 1 2'b10 - TX Start for Video Pipe 2 2'b11 - TX Start for Video Pipe 3
HVD_ST_SEL1	3:2	Selects which Video Pipe TX Start to Output on MFP3 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - TX Start for Video Pipe 0 2'b01 - TX Start for Video Pipe 1 2'b10 - TX Start for Video Pipe 2 2'b11 - TX Start for Video Pipe 3

BITFIELD	BITS	DESCRIPTION
HVD_ST_SEL0	1:0	Selects which Video Pipe TX Start to Output on MFP1 Note: Must also program HVD_OUT_EN and HVD_OUT_SEL 2'b00 - TX Start for Video Pipe 0 2'b01 - TX Start for Video Pipe 1 2'b10 - TX Start for Video Pipe 2 2'b11 - TX Start for Video Pipe 3

VIDEO_RX0 (0x100, 0x112, 0x124, 0x136)

BIT	7	6	5	4	3	2	1	0
Field	LCRC_ERR	RSVD	RSVD	SEQ_MISS_EN	RSVD	RSVD	LINE_CRC_EN	DIS_PKT_DET
Reset	0x0	0b0	0b1	0b1	0b0	0b0	0b1	0b0
Access Type	Read Clears All			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LCRC_ERR	7	Video Line CRC Error Flag Asserted when a video line CRC error is detected	0b0: No video line CRC error detected 0b1: Video line CRC error detected
SEQ_MISS_EN	4	Video sequence miss detection enable	0b0: Disable Video Sequence Miss Detection 0b1: Video Sequence Miss Detection Enabled (Default)
LINE_CRC_EN	1	Video Line CRC Enable	0b0: Disable video line CRC 0b1: Enable video line CRC
DIS_PKT_DET	0	Disable Packet Detector If the video is restarted with a different BPP when the packet detector is disabled, toggle this register or the video receive enable register to make sure the video link restarts.	0b0: Enable packet detect (default) 0b1: Disable packet detect

VIDEO_RX6 (0x106, 0x118, 0x12A, 0x13C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[2:0]			VID_SEQ_ERR_OEN	LIM_HEART	–	RSVD	RSVD
Reset	0x0			0b1	0b0	–	0b1	0b0
Access Type				Write, Read	Write, Read	–		

BITFIELD	BITS	DESCRIPTION	DECODE
VID_SEQ_ERR_OEN	4	Enables reflection of Video Sequencing Error onto the ERRB pin. Refer to the VID_SEQ_ERR register field.	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LIM_HEART	3	If enabled, there is a configurable timeout using VRX_PKT_DET.TIMEOUT_x (default is 10ms) to detect loss of video lock. If disabled, there is a 100us timeout to detect loss of video lock. If Heartbeat is disabled (LIM_HEART = 1 on Serializer), set VRX_PKT_DET.TIMEOUT_x from 1 to 127ms, as per requirement. Use together with SEQ_MISS_EN and DIS_PKT_DET registers in deserializer. Embedded data should use the Heartbeat to ensure loss of video lock timeout does not occur.	0x0 0x1: See Description

VIDEO_RX8 (0x108, 0x11A, 0x12C, 0x13E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	VID_LOCK	VID_PKT_DET	VID_SEQ_ERR	RSVD[3:0]			
Reset	0b0	0b0	0b0	0b0	0x2			
Access Type		Read Only	Read Only	Read Clears All				

BITFIELD	BITS	DESCRIPTION	DECODE
VID_LOCK	6	Video pipeline locked	0b0: Video pipeline not locked 0b1: Video pipeline locked
VID_PKT_DET	5	Video Rx sufficient packet throughput detection.	0b0: Insufficient packet throughput 0b1: Sufficient packet throughput
VID_SEQ_ERR	4	Video Rx sequence error detection.	0b0: No video Rx sequence error detected 0b1: Video Rx sequence error detected

LIM_HEART_TIMEOUT_0 (0x160)

BIT	7	6	5	4	3	2	1	0
Field	–	LIM_HEART_TIMEOUT_0[6:0]						
Reset	–	0xA						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
LIM_HEART_TIMEOUT_0	6:0	Video Pipe 0 Packet Detection Timeout used when LIM_HEART=1. Timeout can be configured from 1 to 127 in milliseconds. bits [6:0]: Timeout count (in ms) Note: Value of 0 will also default to 1ms.

LIM_HEART_TIMEOUT_1 (0x161)

BIT	7	6	5	4	3	2	1	0
Field	–	LIM_HEART_TIMEOUT_1[6:0]						
Reset	–	0xA						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
LIM_HEART_TIMEOUT_1	6:0	Video Pipe 1 Packet Detection Timeout used when LIM_HEART=1. Timeout can be configured from 1 to 127 in milliseconds. bits [6:0]: Timeout count (in ms) Note: Value of 0 will also default to 1ms.

LIM_HEART_TIMEOUT_2 (0x162)

BIT	7	6	5	4	3	2	1	0
Field	–	LIM_HEART_TIMEOUT_2[6:0]						
Reset	–	0xA						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
LIM_HEART_TIMEOUT_2	6:0	Video Pipe 2 Packet Detection Timeout used when LIM_HEART=1. Timeout can be configured from 1 to 127 in milliseconds. bits [6:0]: Timeout count (in ms) Note: Value of 0 will also default to 1ms.

LIM_HEART_TIMEOUT_3 (0x163)

BIT	7	6	5	4	3	2	1	0
Field	–	LIM_HEART_TIMEOUT_3[6:0]						
Reset	–	0xA						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION
LIM_HEART_TIMEOUT_3	6:0	Video Pipe 3 Packet Detection Timeout used when LIM_HEART=1. Timeout can be configured from 1 to 127 in milliseconds. bits [6:0]: Timeout count (in ms) Note: Value of 0 will also default to 1ms.

CROSS_HS (0x1D8, 0x1F8, 0x218, 0x238)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_HS_I	CROSS_HS_F	CROSS_HS[4:0]				
Reset	–	0x0	0x0	0x18				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_HS_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_HS_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_HS	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

CROSS_VS (0x1D9, 0x1F9, 0x219, 0x239)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_VS_I	CROSS_VS_F	CROSS_VS[4:0]				
Reset	–	0x0	0x0	0x19				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_VS_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_VS_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_VS	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

CROSS_DE (0x1DA, 0x1FA, 0x21A, 0x23A)

BIT	7	6	5	4	3	2	1	0
Field	–	CROSS_DE_I	CROSS_DE_F	CROSS_DE[4:0]				
Reset	–	0x0	0x0	0x1A				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
CROSS_DE_I	6	Inverts CrossX	0b0: Do not invert bit 0b1: Invert bit
CROSS_DE_F	5	Forces CrossX to 0 before inversion	0b0: Do not force bit to zero 0b1: Force bit to zero
CROSS_DE	4:0	Maps selected internal signal to Cross X	0bXXXXX: Incoming bit position

PRBS_ERR (0x1DB, 0x1FB, 0x21B, 0x23B)

BIT	7	6	5	4	3	2	1	0
Field	VPRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VPRBS_ERR	7:0	Video PRBS error counter, clears on read	0xXX: Number of video PRBS errors since last read

VPRBS (0x1DC, 0x1FC, 0x21C, 0x23C)

BIT	7	6	5	4	3	2	1	0
Field	PATGEN_CLK_SRC	VPRBS_CHECK	VPRBS_FAIL	VPRBS24_GENCHK_EN	VPRBS7_GENCHK_EN	VPRBS9_GENCHK_EN	DIS_GLITCH_FILT	VIDEO_LOCK
Reset	0x1	0b0	0b0	0b0	0b0	0b0	0x0	0b0
Access Type	Write, Read	Read Only	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
PATGEN_CLK_SRC	7	Pattern generator clock source for video PRBS7, PRBS9, PRBS24, checkerboard, and gradient patterns. 0 = 150MHz, 1 = 375MHz (default).	0b0: 150MHz 0b1: 375MHz (default)
VPRBS_CHECK	6	Indicates when PRBS checker has synchronized and is checking received PRBS data.	0: PRBS Checker has not started checking 1: PRBS Checker started checking
VPRBS_FAIL	5	Indicates when PRBS checker could not synchronize and PRBS test failed.	0: PRBS Checker synchronized and test passed 1: PRBS Checker could not synchronize and test failed
VPRBS24_GENCHK_EN	4	Enables video PRBS24 generator/checker	0b0: Video PRBS24 generator/checker disabled 0b1: Video PRBS24 generator/checker enabled
VPRBS7_GENCHK_EN	3	Enables video PRBS7 generator/checker	0b0: Video PRBS7 generator/checker disabled 0b1: Video PRBS7 generator/checker enabled
VPRBS9_GENCHK_EN	2	Enables video PRBS9 generator/checker	0b0: Video PRBS9 generator/checker disabled 0b1: Video PRBS9 generator/checker enabled
DIS_GLITCH_FILT	1	Disables HS, VS, and DE glitch filtering	0b0: Glitch filter enabled 0b1: Glitch filter disabled
VIDEO_LOCK	0	Video channel is locked and outputting valid video data	0b0: Video channel is not locked 0b1: Video channel is locked

POLARITY_A_L (0x2E0)

BIT	7	6	5	4	3	2	1	0
Field	POLARITY_A_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_A_L	7:0	Packet GPIO[7:0] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

POLARITY_B_L (0x2E1)

BIT	7	6	5	4	3	2	1	0
Field	POLARITY_B_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_B_L	7:0	Packet GPIO[7:0] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

POLARITY_C_L (0x2E2)

BIT	7	6	5	4	3	2	1	0
Field	POLARITY_C_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_C_L	7:0	Packet GPIO[7:0] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

POLARITY_D_L (0x2E3)

BIT	7	6	5	4	3	2	1	0
Field	POLARITY_D_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_D_L	7:0	Packet GPIO[7:0] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

POLARITY_AB_H (0x2E4)

BIT	7	6	5	4	3	2	1	0
Field	–	POLARITY_B_H[2:0]			–	POLARITY_A_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_B_H	6:4	Packet GPIO[10:8] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_A_H	2:0	Packet GPIO[10:8] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

POLARITY_CD_H (0x2E5)

BIT	7	6	5	4	3	2	1	0
Field	–	POLARITY_D_H[2:0]			–	POLARITY_C_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
POLARITY_D_H	6:4	Packet GPIO[10:8] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)
POLARITY_C_H	2:0	Packet GPIO[10:8] RX Aggregation Polarity/ Inversion Function	0x0: Acitve Low (True State, default) 0x1: Active High (Invert State)

ENABLE_A_L (0x2E6)

BIT	7	6	5	4	3	2	1	0
Field	ENABLE_A_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_A_L	7:0	Packet GPIO[7:0] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

ENABLE_B_L (0x2E7)

BIT	7	6	5	4	3	2	1	0
Field	ENABLE_B_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_B_L	7:0	Packet GPIO[7:0] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

ENABLE_C_L (0x2E8)

BIT	7	6	5	4	3	2	1	0
Field	ENABLE_C_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_C_L	7:0	Packet GPIO[7:0] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

ENABLE_D_L (0x2E9)

BIT	7	6	5	4	3	2	1	0
Field	ENABLE_D_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_D_L	7:0	Packet GPIO[7:0] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

ENABLE_AB_H (0x2EA)

BIT	7	6	5	4	3	2	1	0
Field	–	ENABLE_B_H[2:0]			–	ENABLE_A_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_B_H	6:4	Packet GPIO[10:8] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)
ENABLE_A_H	2:0	Packet GPIO[10:8] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

ENABLE_CD_H (0x2EB)

BIT	7	6	5	4	3	2	1	0
Field	–	ENABLE_D_H[2:0]			–	ENABLE_C_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ENABLE_D_H	6:4	Packet GPIO[10:8] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)
ENABLE_C_H	2:0	Packet GPIO[10:8] RX Aggregation Enable	0x0: Disabled (GPIO RX data bit set high to aggregator or AND function, default) 0x1: Enabled (GPIO RX data bit passed to aggregator or AND function)

READ_A_L (0x2EC)

BIT	7	6	5	4	3	2	1	0
Field	READ_A_L[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
READ_A_L	7:0	Packet GPIO[7:0] RX Aggregation Read State

READ_B_L (0x2ED)

BIT	7	6	5	4	3	2	1	0
Field	READ_B_L[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
READ_B_L	7:0	Packet GPIO[7:0] RX Aggregation Read State

READ_C_L (0x2EE)

BIT	7	6	5	4	3	2	1	0
Field	READ_C_L[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
READ_C_L	7:0	Packet GPIO[7:0] RX Aggregation Read State

READ_D_L (0x2EF)

BIT	7	6	5	4	3	2	1	0
Field	READ_D_L[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
READ_D_L	7:0	Packet GPIO[7:0] RX Aggregation Read State

READ_AB_H (0x2F0)

BIT	7	6	5	4	3	2	1	0
Field	–	READ_B_H[2:0]			–	READ_A_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION
READ_B_H	6:4	Packet GPIO[10:8] RX Aggregation Read State
READ_A_H	2:0	Packet GPIO[10:8] RX Aggregation Read State

READ_CD_H (0x2F1)

BIT	7	6	5	4	3	2	1	0
Field	–	READ_D_H[2:0]			–	READ_C_H[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Read Only			–	Read Only		

BITFIELD	BITS	DESCRIPTION
READ_D_H	6:4	Packet GPIO[10:8] RX Aggregation Read State
READ_C_H	2:0	Packet GPIO[10:8] RX Aggregation Read State

OUTPUT (0x2F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OUTPUT_INVERT	OUTPUT_ENABLE	DESTINATION	READ_FLAG
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
OUTPUT_INVERT	3	Packet GPIO RX Aggregation Output Invert	0x0: Aggregation Output True 0x1: Aggregation Output Inverted
OUTPUT_ENABLE	2	Packet GPIO RX Aggregation Output Enable to ERRB Pin	0x0: Disabled (default) 0x1: Enabled
DESTINATION	1	Packet GPIO RX Aggregation Output destination or output enable to MFP6	0x0: Disabled to MFP6 0x1: Enabled to MFP6

BITFIELD	BITS	DESCRIPTION	DECODE
READ_FLAG	0	Packet GPIO RX Aggregation Output, Active Low	0x0: Aggregation Error 0x1: Aggregation No Error

GPIO_A (0x300)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x301)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x00				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x302)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x00				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x300) and PULL_UPDN_SEL (0x301) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x303)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x304)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x01				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x305)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x01				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x303) and PULL_UPDN_SEL (0x304) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x306)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x307)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x02				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x308)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x02				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x306) and PULL_UPDN_SEL (0x307) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x309)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x30A)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x03				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x30B)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x03				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x309) and PULL_UPDN_SEL (0x30A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x30C)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x30D)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x04				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x30E)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x04				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x30C) and PULL_UPDN_SEL (0x30D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x310)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x311)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x05				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x312)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x05				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x310) and PULL_UPDN_SEL (0x311) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x313)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x314)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x0		0b1	0x06				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration by default MFP6 does not have a pull down selection like the other MFPs.	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x315)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x06				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x313) and PULL_UPDN_SEL (0x314) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x316)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x317)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x07				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x318)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x07				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x316) and PULL_UPDN_SEL (0x317) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x319)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x31A)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x08				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x31B)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x08				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x319) and PULL_UPDN_SEL (0x31A) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x31C)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x31D)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x09				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x31E)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x09				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x31C) and PULL_UPDN_SEL (0x31D) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_A (0x320)

BIT	7	6	5	4	3	2	1	0
Field	RES_CFG	RSVD	TX_COMP_EN	GPIO_OUT	GPIO_IN	GPIO_RX_EN	GPIO_TX_EN	GPIO_OUT_DIS
Reset	0b1	0x0	0x0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RES_CFG	7	Resistor pullup/pulldown strength	0b0: 40kΩ 0b1: 1MΩ
TX_COMP_EN	5	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_OUT	4	GPIO pin output drive value when GPIO_RX_EN = 0	0b0: This GPIO pin output is driven to 0 0b1: This GPIO pin output is driven to 1
GPIO_IN	3	GPIO pin input level	0b0: This GPIO pin value is 0 0b1: This GPIO pin value is 1
GPIO_RX_EN	2	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_TX_EN	1	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_OUT_DIS	0	Enable/disable GPIO output driver	0b0: Output driver enabled 0b1: Output driver disabled

GPIO_B (0x321)

BIT	7	6	5	4	3	2	1	0
Field	PULL_UPDN_SEL[1:0]		OUT_TYPE	GPIO_TX_ID[4:0]				
Reset	0x2		0b1	0x0A				
Access Type	Write, Read		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
PULL_UPDN_SEL	7:6	Buffer pullup/pulldown configuration	0b00: None 0b01: Pullup 0b10: Pulldown 0b11: Reserved
OUT_TYPE	5	Driver type selection	0b0: Open-drain 0b1: Push-pull
GPIO_TX_ID	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x322)

BIT	7	6	5	4	3	2	1	0
Field	OVR_RES_CFG	GPIO_RECVED	RSVD	GPIO_RX_ID[4:0]				
Reset	0x0	0b1	0b0	0x0A				
Access Type	Write, Read	Write, Read		Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
OVR_RES_CFG	7	Override non-GPIO port function IO setting. When set, RES_CFG (0x320) and PULL_UPDN_SEL (0x321) are effective when pin is configured as non-GPIO. When cleared, non-GPIO pin function determines IO type.	0b0: Non-GPIO function determines IO type when alternate function is selected 0b1: RES_CFG and PULL_UPDN_SEL determine IO type for non-GPIO configuration
GPIO_RECVED	6	Received GPIO value	
GPIO_RX_ID	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x337)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x338)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x33A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x33B)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x33D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x33E)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x341)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x342)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x344)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x345)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x347)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x348)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x34A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x34B)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x34D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x34E)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x351)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x352)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x354)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x355)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x357)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_B	GPIO_TX_EN_B	GPIO_TX_ID_B[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_B	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_B	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_B	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x358)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_B	GPIO_RX_EN_B	GPIO_RX_ID_B[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_B	6	Received GPIO value	
GPIO_RX_EN_B	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_B	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x36D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x36E)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x371)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x372)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x374)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x375)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x377)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x378)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x37A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x37B)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x37D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x37E)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x381)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x382)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x384)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x385)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x387)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x388)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x38A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x38B)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x38D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_C	GPIO_TX_EN_C	GPIO_TX_ID_C[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_C	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_C	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_C	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x38E)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_C	GPIO_RX_EN_C	GPIO_RX_ID_C[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_C	6	Received GPIO value	
GPIO_RX_EN_C	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_C	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3A4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x00				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3A5)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x00				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3A7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x01				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3A8)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x01				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3AA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x02				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3AB)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x02				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3AD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x03				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3AE)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x03				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x04				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B2)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x04				
Access Type	–		Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x05				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B5)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x05				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3B7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x06				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3B8)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x06				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3BA)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x07				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3BB)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x07				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3BD)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x08				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3BE)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x08				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3C1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x09				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3C2)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x09				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

GPIO_B (0x3C4)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	TX_COMP_EN_D	GPIO_TX_EN_D	GPIO_TX_ID_D[4:0]				
Reset	0x0	0x0	0b0	0x0a				
Access Type		Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TX_COMP_EN_D	6	Jitter minimization compensation enable	0b0: Jitter compensation disabled 0b1: Jitter compensation enabled
GPIO_TX_EN_D	5	GPIO Tx source control	0b0: This GPIO source disabled for GMSL2 transmission 0b1: This GPIO source enabled for GMSL2 transmission
GPIO_TX_ID_D	4:0	GPIO ID for pin while transmitting	0bXXXXX: This GPIO transmit ID

GPIO_C (0x3C5)

BIT	7	6	5	4	3	2	1	0
Field	–	GPIO_RECVED_D	GPIO_RX_EN_D	GPIO_RX_ID_D[4:0]				
Reset	–	0b1	0b0	0x0a				
Access Type	–	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_RECVED_D	6	Received GPIO value	
GPIO_RX_EN_D	5	GPIO out source control	0b0: This GPIO source disabled for GMSL2 reception 0b1: This GPIO source enabled for GMSL2 reception
GPIO_RX_ID_D	4:0	GPIO ID for pin while receiving	0bXXXXX: This GPIO receive ID

BACKTOP1 (0x400)

BIT	7	6	5	4	3	2	1	0
Field	CSIPLL3_LOCK	CSIPLL2_LOCK	CSIPLL1_LOCK	CSIPLL0_LOCK	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Read Only	Read Only	Read Only	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL3_LOCK	7	CSIPLL1 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL2_LOCK	6	CSIPLL0 lock	0b0: CSI2 0 PLL not locked 0b1: CSI2 0 PLL locked
CSIPLL1_LOCK	5	CSIPLL1 lock	0b0: PLL not locked 0b1: PLL locked
CSIPLL0_LOCK	4	CSIPLL0 lock	0b0: CSI2 0 PLL not locked 0b1: CSI2 0 PLL locked

BACKTOP2 (0x401)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC0_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC0_L	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 0 enabled 0xXXXXXX1X: Virtual Channel 1 enabled 0xXXXXX1XX: Virtual Channel 2 enabled 0xXXXX1XXX: Virtual Channel 3 enabled 0xXXX1XXXX: Virtual Channel 4 enabled 0xXX1XXXXX: Virtual Channel 5 enabled 0xX1XXXXXX: Virtual Channel 6 enabled 0x1XXXXXXX: Virtual Channel 7 enabled

BACKTOP3 (0x402)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC0_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC0_H	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 8 enabled 0xXXXXXX1X: Virtual Channel 9 enabled 0xXXXXX1XX: Virtual Channel 10 enabled 0xXXXX1XXX: Virtual Channel 11 enabled 0xXXX1XXXX: Virtual Channel 12 enabled 0xXX1XXXXX: Virtual Channel 13 enabled 0xX1XXXXXX: Virtual Channel 14 enabled 0x1XXXXXXX: Virtual Channel 15 enabled

BACKTOP4 (0x403)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC1_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC1_L	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 0 enabled 0xXXXXXX1X: Virtual Channel 1 enabled 0xXXXXX1XX: Virtual Channel 2 enabled 0xXXXX1XXX: Virtual Channel 3 enabled 0xXXX1XXXX: Virtual Channel 4 enabled 0xXX1XXXXX: Virtual Channel 5 enabled 0xX1XXXXXX: Virtual Channel 6 enabled 0x1XXXXXXX: Virtual Channel 7 enabled

BACKTOP5 (0x404)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC1_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC1_H	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 8 enabled 0xXXXXXX1X: Virtual Channel 9 enabled 0xXXXXX1XX: Virtual Channel 10 enabled 0xXXXX1XXX: Virtual Channel 11 enabled 0xXXX1XXXX: Virtual Channel 12 enabled 0xXX1XXXXX: Virtual Channel 13 enabled 0xX1XXXXXX: Virtual Channel 14 enabled 0x1XXXXXXX: Virtual Channel 15 enabled

BACKTOP6 (0x405)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC2_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC2_L	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 0 enabled 0xXXXXXX1X: Virtual Channel 1 enabled 0xXXXXX1XX: Virtual Channel 2 enabled 0xXXXX1XXX: Virtual Channel 3 enabled 0xXXX1XXXX: Virtual Channel 4 enabled 0xXX1XXXXX: Virtual Channel 5 enabled 0xX1XXXXXX: Virtual Channel 6 enabled 0x1XXXXXXX: Virtual Channel 7 enabled

BACKTOP7 (0x406)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC2_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC2_H	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 8 enabled 0xXXXXXX1X: Virtual Channel 9 enabled 0xXXXXX1XX: Virtual Channel 10 enabled 0xXXXX1XXX: Virtual Channel 11 enabled 0xXXX1XXXX: Virtual Channel 12 enabled 0xXX1XXXXX: Virtual Channel 13 enabled 0xX1XXXXXX: Virtual Channel 14 enabled 0x1XXXXXXX: Virtual Channel 15 enabled

BACKTOP8 (0x407)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC3_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC3_L	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 0 enabled 0xXXXXXX1X: Virtual Channel 1 enabled 0xXXXXX1XX: Virtual Channel 2 enabled 0xXXXX1XXX: Virtual Channel 3 enabled 0xXXX1XXXX: Virtual Channel 4 enabled 0xXX1XXXXX: Virtual Channel 5 enabled 0xX1XXXXXX: Virtual Channel 6 enabled 0x1XXXXXXX: Virtual Channel 7 enabled

BACKTOP9 (0x408)

BIT	7	6	5	4	3	2	1	0
Field	VS_VC3_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_VC3_H	7:0	Override Frame Start-End short packet VC enable. Each bit corresponds to a Virtual Channel number enable	0x0: Default behavior 0xXXXXXXX1: Virtual Channel 8 enabled 0xXXXXXX1X: Virtual Channel 9 enabled 0xXXXXX1XX: Virtual Channel 10 enabled 0xXXXX1XXX: Virtual Channel 11 enabled 0xXXX1XXXX: Virtual Channel 12 enabled 0xXX1XXXXX: Virtual Channel 13 enabled 0xX1XXXXXX: Virtual Channel 14 enabled 0x1XXXXXXX: Virtual Channel 15 enabled

BACKTOP10 (0x409)

BIT	7	6	5	4	3	2	1	0
Field	DE_SEL3	DE_SEL2	DE_SEL1	DE_SEL0	RSVD	RSVD	RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DE_SEL3	7	Use HS for creation of long packets instead of DE	0x0: Use DE for creation of long packets 0x1: Use HS for creation of long packets
DE_SEL2	6	Use HS for creation of long packets instead of DE	0x0: Use DE for creation of long packets 0x1: Use HS for creation of long packets
DE_SEL1	5	Use HS for creation of long packets instead of DE	0x0: Use DE for creation of long packets 0x1: Use HS for creation of long packets
DE_SEL0	4	Use HS for creation of long packets instead of DE	0x0: Use DE for creation of long packets 0x1: Use HS for creation of long packets

BACKTOP11 (0x40A)

BIT	7	6	5	4	3	2	1	0
Field	cmd_overflow3	cmd_overflow2	cmd_overflow1	cmd_overflow0	LMO_3	LMO_2	LMO_1	LMO_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
cmd_overflow3	7	Pipe 3 command FIFO overflow. Cleared on read. See the CMD_OVFL_3_ERRB_OEN register to enable output of this status on ERRB pin.	0b0: No overflow 0b1: Overflow
cmd_overflow2	6	Pipe 2 command FIFO overflow. Cleared on read. See the CMD_OVFL_2_ERRB_OEN register to enable output of this status on ERRB pin.	0b0: No overflow 0b1: Overflow
cmd_overflow1	5	Pipe 1 command FIFO overflow. Cleared on read. See the CMD_OVFL_1_ERRB_OEN register to enable output of this status on ERRB pin.	0b0: No overflow 0b1: Overflow
cmd_overflow0	4	Pipe 0 command FIFO overflow. Cleared on read. See the CMD_OVFL_0_ERRB_OEN register to enable output of this status on ERRB pin.	0b0: No overflow 0b1: Overflow
LMO_3	3	Pipe 3 line memory overflow sticky register. Cleared on read.	0b0: No overflow 0b1: Overflow
LMO_2	2	Pipe 2 line memory overflow sticky register. Cleared on read.	0b0: No overflow 0b1: Overflow
LMO_1	1	Pipe 1 line memory overflow sticky register. Cleared on read.	0b0: No overflow 0b1: Overflow
LMO_0	0	Pipe 0 line memory overflow sticky register. Cleared on read. See LMO_0_ERRB_EN to enable output of this status to the ERRB pin	0b0: No overflow 0b1: Overflow

BACKTOP12 (0x40B)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_0[4:0]					–	CSI_OUT_EN	RSVD
Reset	0x00					–	0b1	0b0
Access Type	Write, Read					–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_0	7:3	Pipe 0 BPP software-override: Software-override video data BPP.	0x8: Data types = 0x2A, 0x10-12, 0x31-37 0xA: Data types = 0x2B 0xC: Data types = 0x2C 0xE: Data types = 0x2D 0x10: Data types = 0x22, 0x1E, 0x2E 0x12: Data types = 0x23 0x14: Data types = 0x1F, 0x2F 0x18: Data types = 0x24, 0x30 All other values: Reserved
CSI_OUT_EN	1	Enables MIPI CSI output	0b0: CSI output disabled 0x1: CSI output enabled

BACKTOP13 (0x40C)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_1[3:0]				soft_vc_0[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_1	7:4	Pipe 1 VC software-override	0xX: Software-defined virtual channel for Pipe 1
soft_vc_0	3:0	Pipe 0 VC software-override	0xX: Software-defined virtual channel for Pipe 0

BACKTOP14 (0x40D)

BIT	7	6	5	4	3	2	1	0
Field	soft_vc_3[3:0]				soft_vc_2[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_vc_3	7:4	Pipe 3 VC software-override	0xX: Software-defined virtual channel for Pipe 3
soft_vc_2	3:0	Pipe 2 VC software-override	0xX: Software-defined virtual channel for Pipe 2

BACKTOP15 (0x40E)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_1_h[1:0]		soft_dt_0[5:0]					
Reset	0x0		0x00					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_1_h	7:6	Pipe 1 DT (high bits) software-override bitfield. Works together with soft_dt_1_l in BACKTOP16 register (0x40F).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_0	5:0	Pipe 0 DT software-override.	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP16 (0x40F)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_2_h[3:0]				soft_dt_1_l[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_2_h	7:4	Pipe 2 DT (high bits) software-override bitfield. Works together with soft_dt_2_l in BACKTOP17 register (0x410).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_1_l	3:0	Pipe 1 DT (low bits) software-override bitfield. Works together with soft_dt_1_h in BACKTOP16 register (0x40E).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP17 (0x410)

BIT	7	6	5	4	3	2	1	0
Field	soft_dt_3[5:0]						soft_dt_2_l[1:0]	
Reset	0x00						0x0	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_dt_3	7:2	Pipe 3 DT software-override	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8
soft_dt_2_l	1:0	Pipe 2 DT (low bits) software-override. Works together with soft_dt_2_h in BACKTOP16 register (0x40F).	0x10: GENERIC8 0x11: GENERIC8 0x12: EMBEDDED 0x1E: YUV422 8-bit 0x1F: YUV422 10-bit 0x22: RGB565 0x23: RGB666 0x24: RGB888 0x2A: RAW8 0x2B: RAW10 0x2C: RAW12 0x2D: RAW14 0x2E: RAW16 0x2F: RAW20 0x30: YUV422 12-bit 0x31: UDP8 0x32: UDP8 0x33: UDP8 0x34: UDP8 0x35: UDP8 0x36: UDP8 0x37: UDP8

BACKTOP18 (0x411)

BIT	7	6	5	4	3	2	1	0
Field	soft_bpp_2_h[2:0]			soft_bpp_1[4:0]				
Reset	0x0			0x00				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_2_h	7:5	Pipe 2 BPP (high bits) software-override bitfield: Works together with soft_bpp_2_l in BACKTOP19 register (0x412).	0bXX: High bits of software-defined BPP for Pipe 2
soft_bpp_1	4:0	Pipe 1 BPP software-override bitfield: Software override video data BPP.	0x8: Data types = 0x2A, 0x10-12, 0x31-37 0xA: Data types = 0x2B 0xC: Data types = 0x2C 0xE: Data types = 0x2D 0x10: Data types = 0x22, 0x1E, 0x2E 0x12: Data types = 0x23 0x14: Data types = 0x1F, 0x2F 0x18: Data types = 0x24, 0x30

BACKTOP19 (0x412)

BIT	7	6	5	4	3	2	1	0
Field	–	soft_bpp_3[4:0]					soft_bpp_2_l[1:0]	
Reset	–	0x00					0x0	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
soft_bpp_3	6:2	Pipe 3 BPP software-override bitfield: Software override video data BPP.	0x8: Data types = 0x2A, 0x10-12, 0x31-37 0xA: Data types = 0x2B 0xC: Data types = 0x2C 0xE: Data types = 0x2D 0x10: Data types = 0x22, 0x1E, 0x2E 0x12: Data types = 0x23 0x14: Data types = 0x1F, 0x2F 0x18: Data types = 0x24, 0x30 0bXX: New BPP for Pipe 4
soft_bpp_2_l	1:0	Pipe 2 BPP software-override register: Software override video data BPP (low bits). Works together with soft_bpp_2_h in BACKTOP18 register (0x412).	0bXX: Low bits of software-defined BPP for Pipe 2

BACKTOP20 (0x413)

BIT	7	6	5	4	3	2	1	0
Field	phy0_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY0 frequency fine tuning	0xXX: PHY frequency fine tuning override low byte

BACKTOP21 (0x414)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl3	bpp8dbl2	bpp8dbl1	bpp8dbl0	phy0_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl3	7	Pipe 3 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl2	6	Pipe 2 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl1	5	Pipe 1 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
bpp8dbl0	4	Pipe 0 BPP8 double-pixel register: BPP = 8 processed as 16-bit color	0b0: Disable process BPP = 8 as 16-bit color 0b1: Enable process BPP = 8 as 16-bit color
phy0_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY0 frequency fine tuning	0xX: PHY0 frequency fine tuning override high nibble

BACKTOP22 (0x415)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_1	override_bpp_vc_dt_0	phy0_csi_tx_dpll_fb_fraction_predef_en	phy0_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_1	7	Pipe 1 software-override enable bitfield Note: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • RRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC _#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0b0: Disable 0b1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_0	6	Pipe 0 software-override enable bitfield Note: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0b0: Disable 0b1: Enable
phy0_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY0 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy0_csi_tx_dpll_predef_freq	4:0	MIPI PHY0 DPLL frequency bitfield. Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half, data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL, 456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP23 (0x416)

BIT	7	6	5	4	3	2	1	0
Field	phy1_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY1 frequency fine tuning	0xXX: PHY1 frequency fine tuning override low byte

BACKTOP24 (0x417)

BIT	7	6	5	4	3	2	1	0
Field	bpp8dbl3_mode	bpp8dbl2_mode	bpp8dbl1_mode	bpp8dbl0_mode	phy1_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0b0	0b0	0b0	0b0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl3_mode	7	Pipe 3 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl2_mode	6	Pipe 2 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected

BITFIELD	BITS	DESCRIPTION	DECODE
bpp8dbl1_mode	5	Pipe 1 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp8dbl0_mode	4	Pipe 0 BPP8 double-pixel mode register: 8-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
phy1_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY1 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

BACKTOP25 (0x418)

BIT	7	6	5	4	3	2	1	0
Field	override_bpp_vc_dt_3	override_bpp_vc_dt_2	phy1_csi_tx_dpll_fb_fraction_predef_en	phy1_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
override_bpp_vc_dt_3	7	Pipe 3 software-override enable bitfield Note: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0b0: Disable 0b1: Enable
override_bpp_vc_dt_2	6	Pipe 2 software-override enable bitfield Note: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0b0: Disable 0b1: Enable
phy1_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY1 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_csi_tx_dpll_predef_freq	4:0	MIPI PHY1 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP26 (0x419)

BIT	7	6	5	4	3	2	1	0
Field	phy2_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY2 frequency fine tuning	0xXX: PHY1 frequency fine tuning override low byte

BACKTOP27 (0x41A)

BIT	7	6	5	4	3	2	1	0
Field	yuv_8_10_mux_mode3	yuv_8_10_mux_mode2	yuv_8_10_mux_mode1	yuv_8_10_mux_mode0	phy2_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
yuv_8_10_mux_mode3	7	Pipe 3 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode2	6	Pipe 2 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode1	5	Pipe 1 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
yuv_8_10_mux_mode0	4	Pipe 0 YUV422 8-bit and 10-bit mux	0b0: Disable 8-/10-bit mux 0b1: Enable 8-/10-bit mux
phy2_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY2 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

BACKTOP28 (0x41B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy2_csi_tx_dpll_fb_fraction_predef_en	phy2_csi_tx_dpll_predef_freq[4:0]				
Reset	–	–	0b1	0x0F				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
phy2_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY2 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy2_csi_tx_dpll_predef_freq	4:0	MIPI PHY2 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP29 (0x41C)

BIT	7	6	5	4	3	2	1	0
Field	phy3_csi_tx_dpll_fb_fraction_in_l[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_l	7:0	Low byte of software-override value for CSI PHY3 frequency fine tuning	0xXX: PHY1 frequency fine tuning override low byte

BACKTOP30 (0x41D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	bpp10dbl3_mode	bpp10dbl3	phy3_csi_tx_dpll_fb_fraction_in_h[3:0]			
Reset	–	–	0b0	0b0	0x0			
Access Type	–	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl3_mode	5	Pipe 3 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl3	4	Pipe 3 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_csi_tx_dpll_fb_fraction_in_h	3:0	High nibble of software-override value for CSI PHY3 frequency fine tuning	0xX: PHY1 frequency fine tuning override high nibble

BACKTOP31 (0x41E)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl2_mode	bpp10dbl2	phy3_csi_tx_dpll_fb_fraction_predef_en	phy3_csi_tx_dpll_predef_freq[4:0]				
Reset	0b0	0b0	0b1	0x0F				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl2_mode	7	Pipe 2 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl2	6	Pipe 2 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
phy3_csi_tx_dpll_fb_fraction_predef_en	5	MIPI PHY3 software-override disable for frequency fine tuning	0b0: Enable software override for frequency fine tuning 0b1: Disable software override for frequency fine tuning
phy3_csi_tx_dpll_predef_freq	4:0	MIPI PHY3 DPLL frequency bitfield: Set DPLL frequency on multiple of 100MHz. DPHY: Clock frequency is half; data rate is equivalent bps/lane. CPHY: 2.28bits/symbol.	DPHY data rate/lane 0x02: 200MHz DPLL, 200Mbps/lane ... 0x19: 2500MHz DPLL, 2.5Gbps/lane CPHY data rate/trio 0x02: 200MHz DPLL,456Mbps/lane ... 0x19: 2500MHz DPLL, 5.7Gbps/lane

BACKTOP32 (0x41F)

BIT	7	6	5	4	3	2	1	0
Field	bpp10dbl1_mode	bpp10dbl1	bpp10dbl0_mode	bpp10dbl0	bpp12dbl3	bpp12dbl2	bpp12dbl1	bpp12dbl0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
bpp10dbl1_mode	7	Pipe 1 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl1	6	Pipe 1 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color
bpp10dbl0_mode	5	Pipe 0 BPP10 double-pixel mode register: 10-bit alternate bit mapping to rams	0b0: Alternative bit mapping not selected 0b1: Alternative bit mapping selected
bpp10dbl0	4	Pipe 0 BPP10 double-pixel register: BPP = 10 processed as 20-bit color	0b0: Disable process BPP = 10 as 20-bit color 0b1: Enable process BPP = 10 as 20-bit color

BITFIELD	BITS	DESCRIPTION	DECODE
bpp12dbl3	3	Pipe 3 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl2	2	Pipe 2 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color
bpp12dbl1	1	Pipe 1 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BP P= 12 as 24-bit color
bpp12dbl0	0	Pipe 0 BPP12 double-pixel register: BPP = 12 processed as 24-bit color	0b0: Disable process BPP = 12 as 24-bit color 0b1: Enable process BPP = 12 as 24-bit color

BACKTOP1 (0x420)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_EN[3:0]				–	–	RSVD[1:0]	
Reset	0b0000				–	–	0x01	
Access Type	Write, Read				–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_EN	7:4	Enable the ERRB packet to each video pipe.	0bxxx0: Disable ERRB packet out to video pipe 0 0bxxx1: Enable ERRB packet out to video pipe 0 0bxx0x: Disable ERRB packet out to video pipe 1 0bxx1x: Enable ERRB packet out to video pipe 1 0bx0xx: Disable ERRB packet out to video pipe 2 0bx1xx: Enable ERRB packet out to video pipe 2 0b0xxx: Disable ERRB packet out to video pipe 3 0b1xxx: Enable ERRB packet out to video pipe 3

BACKTOP2 (0x421)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_Insert_Mode_4[1:0]		ERRB_PKT_Insert_Mode_3[1:0]		ERRB_PKT_Insert_Mode_2[1:0]		ERRB_PKT_Insert_Mode_1[1:0]	
Reset	0b01		0b01		0b01		0b01	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_Insert_Mode_4	7:6	Specify where the ERRB packet is inserted. Specify if ERRB_PKT comes out before or after the "Frame Start/End short packet". Used in conjuction with ERRB_PKT_EDGE_SEL which is used to select Frame Start or Frame End.	0b00: No insertion 0b01: ERRB packet inserted before the Frame Start/End Packet 0b10: ERRB packet inserted after the Frame Start/End Packet 0b11: Reserved
ERRB_PKT_Insert_Mode_3	5:4	Specify where the ERRB packet is inserted. Specify if ERRB_PKT comes out before or after the "Frame Start/End short packet". Used in conjuction with ERRB_PKT_EDGE_SEL which is used to select Frame Start or Frame End.	0b00: No insertion 0b01: ERRB packet inserted before the Frame Start/End Packet 0b10: ERRB packet inserted after the Frame Start/End Packet 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_Insert_Mode_2	3:2	Specify where the ERRB packet is inserted. Specify if ERRB_PKT comes out before or after the "Frame Start/End short packet". Used in conjuction with ERRB_PKT_EDGE_SEL which is used to select Frame Start or Frame End.	0b00: No insertion 0b01: ERRB packet inserted before the Frame Start/End Packet 0b10: ERRB packet inserted after the Frame Start/End Packet 0b11: Reserved
ERRB_PKT_Insert_Mode_1	1:0	Specify where the ERRB packet is inserted. Specify if ERRB_PKT comes out before or after the "Frame Start/End short packet". Used in conjuction with ERRB_PKT_EDGE_SEL which is used to select Frame Start or Frame End.	0b00: No insertion 0b01: ERRB packet inserted before the Frame Start/End Packet 0b10: ERRB packet inserted after the Frame Start/End Packet 0b11: Reserved

BACKTOP3 (0x422)

BIT	7	6	5	4	3	2	1	0
Field	–	ERRB_PKT_EDGE_SEL_4	–	ERRB_PKT_EDGE_SEL_3	–	ERRB_PKT_EDGE_SEL_2	–	ERRB_PKT_EDGE_SEL_1
Reset	–		–		–		–	
Access Type	–	Write, Read	–	Write, Read	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_EDGE_SEL_4	6	0 = ERRB_PKT comes out at Frame End 1 = ERRB_PKT comes out at Frame Start	0x0: 0 = ERRB_PKT comes out at Frame End 0x1: 1 = ERRB_PKT comes out at Frame Start
ERRB_PKT_EDGE_SEL_3	4	0 = ERRB_PKT comes out at Frame End 1 = ERRB_PKT comes out at Frame Start	0x0: 0 = ERRB_PKT comes out at Frame End 0x1: 1 = ERRB_PKT comes out at Frame Start
ERRB_PKT_EDGE_SEL_2	2	0 = ERRB_PKT comes out at Frame End 1 = ERRB_PKT comes out at Frame Start	0x0: 0 = ERRB_PKT comes out at Frame End 0x1: 1 = ERRB_PKT comes out at Frame Start
ERRB_PKT_EDGE_SEL_1	0	0 = ERRB_PKT comes out at Frame End 1 = ERRB_PKT comes out at Frame Start	0x0: 0 = ERRB_PKT comes out at Frame End 0x1: 1 = ERRB_PKT comes out at Frame Start

BACKTOP4 (0x423)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_DBL_MODE_1	–	ERRB_PKT_DT_1[5:0]					
Reset	0x0	–	0x12					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_DBL_MODE_1	7	0 = Double mode disabled 1 = Double mode enabled For pixel mode only. Double mode allows the ERRB packet to be packed more efficiently into memory. Must be used for data types with bpp > 16 and pixels per line count over 2700. Note: Double mode can only be used if the word count of the incoming video is an even number.	0x0: Double mode disabled 0x1: Double mode enabled
ERRB_PKT_DT_1	5:0	Specify the data type for ERRB packet, 0x12 or 0x31-37	0xxX: Data type of ERRB packet

BACKTOP5 (0x424)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_DBL_MODE_2	–	ERRB_PKT_DT_2[5:0]					
Reset	0x0	–	0x12					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_DBL_MODE_2	7	0 = Double mode disabled 1 = Double mode enabled For pixel mode only. Double mode allows the ERRB packet to be packed more efficiently into memory. Must be used for data types with bpp > 16 and pixels per line count over 2700. Note: Double mode can only be used if the word count of the incoming video is an even number.	0x0: Double mode disabled 0x1: Double mode enabled
ERRB_PKT_DT_2	5:0	Specify the data type for ERRB packet, 0x12 or 0x31-37	0xxX: Data type of ERRB packet

BACKTOP6 (0x425)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_DBL_MODE_3	–	ERRB_PKT_DT_3[5:0]					
Reset	0x0	–	0x12					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_DBL_MODE_3	7	0 = Double mode disabled 1 = Double mode enabled For pixel mode only. Double mode allows the ERRB packet to be packed more efficiently into memory. Must be used for data types with bpp > 16 and pixels per line count over 2700. Note: Double mode can only be used if the word count of the incoming video is an even number.	0x0: Double mode disabled 0x1: Double mode enabled
ERRB_PKT_DT_3	5:0	Specify the data type for ERRB packet, 0x12 or 0x31-37	0xxX: Data type of ERRB packet

BACKTOP7 (0x426)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_DBL_MODE_4	–	ERRB_PKT_DT_4[5:0]					
Reset	0x0	–	0x12					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_DBL_MODE_4	7	0 = Double mode disabled 1 = Double mode enabled For pixel mode only. Double mode allows the ERRB packet to be packed more efficiently into memory. Must be used for data types with bpp > 16 and pixels per line count over 2700. Note: Double mode can only be used if the word count of the incoming video is an even number.	0x0: Double mode disabled 0x1: Double mode enabled
ERRB_PKT_DT_4	5:0	Specify the data type for ERRB packet, 0x12 or 0x31-37	0xxX: Data type of ERRB packet

BACKTOP8 (0x427)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_VC_OVRD_EN_1	–	–	ERRB_PKT_VC_OVRD_1[4:0]				
Reset	0x0	–	–	0xF				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_OVRD_EN_1	7	0 = Pick random VC from video source in pipe 1 as the VC for ERRB packets 1 = Use VC specified in ERRB_PKT_VC_OVRD_1 register as the VC for ERRB packets Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#,OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Pick random VC from video source in pipe 0 as the VC for ERRB packets 0x1: Use VC specified in ERRB_PKT_VC_OVRD_0 register as the VC for ERRB packets
ERRB_PKT_VC_OVRD_1	4:0	Specify Virtual Channel number for ERRB Packet when ERRB_PKT_VC_OVRD_EN is set	0xX: Virtual channel number of ERRB packet

BACKTOP9 (0x428)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_VC_OVRD_EN_2	–	–	ERRB_PKT_VC_OVRD_2[4:0]				
Reset	0x0	–	–	0xF				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_OVRD_EN_2	7	0 = Pick random VC from video source in pipe 2 as the VC for ERRB packets 1 = Use VC specified in ERRB_PKT_VC_OVRD_2 register as the VC for ERRB packets Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#,OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Pick random VC from video source in pipe 1 as the VC for ERRB packets 0x1: Use VC specified in ERRB_PKT_VC_OVRD_1 register as the VC for ERRB packets
ERRB_PKT_VC_OVRD_2	4:0	Specify Virtual Channel number for ERRB Packet when ERRB_PKT_VC_OVRD_EN is set	0xX: Virtual channel number of ERRB packet

BACKTOP10 (0x429)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_VC_OVRD_EN_3	–	–	ERRB_PKT_VC_OVRD_3[4:0]				
Reset	0x0	–	–	0xF				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_OVRD_EN_3	7	0 = Pick random VC from video source in pipe 3 as the VC for ERRB packets 1 = Use VC specified in ERRB_PKT_VC_OVRD_3 register as the VC for ERRB packets Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#,OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Pick random VC from video source in pipe 2 as the VC for ERRB packets 0x1: Use VC specified in ERRB_PKT_VC_OVRD_2 register as the VC for ERRB packets
ERRB_PKT_VC_OVRD_3	4:0	Specify Virtual Channel number for ERRB Packet when ERRB_PKT_VC_OVRD_EN is set	0xX: Virtual channel number of ERRB packet

BACKTOP11 (0x42A)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_VC_OVRD_EN_4	–	–	ERRB_PKT_VC_OVRD_4[4:0]				
Reset	0x0	–	–	0xF				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_OVRD_EN_4	7	0 = Pick random VC from video source in pipe 4 as the VC for ERRB packets 1 = Use VC specified in ERRB_PKT_VC_OVRD_4 register as the VC for ERRB packets Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#,OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Pick random VC from video source in pipe 3 as the VC for ERRB packets 0x1: Use VC specified in ERRB_PKT_VC_OVRD_3 register as the VC for ERRB packets
ERRB_PKT_VC_OVRD_4	4:0	Specify Virtual Channel number for ERRB Packet when ERRB_PKT_VC_OVRD_EN is set	0xX: Virtual channel number of ERRB packet

BACKTOP12 (0x42B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERRB_PKT_VC_1[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_1	4:0	Virtual Channel number used by ERRB Packet	0xX: Virtual channel number of ERRB packet

BACKTOP13 (0x42C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERRB_PKT_VC_2[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_2	4:0	Virtual Channel number used by ERRB Packet	0xX: Virtual channel number of ERRB packet

BACKTOP14 (0x42D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERRB_PKT_VC_3[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_3	4:0	Virtual Channel number used by ERRB Packet	0xX: Virtual channel number of ERRB packet

BACKTOP15 (0x42E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERRB_PKT_VC_4[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_VC_4	4:0	Virtual Channel number used by ERRB Packet	0xX: Virtual channel number of ERRB packet

BACKTOP22 (0x435)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	n_vs_block[3:0]			
Reset	–	–	–	–	0x1			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
n_vs_block	3:0	Frame block: Block the first 1-15 frames after video lock	0x0: All frames out 0x1: Block the first frame ... ... 0xF: Block the first 15 frames

BACKTOP23 (0x436)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	dis_vs3	dis_vs2	dis_vs1	dis_vs0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
dis_vs3	3	Pipe 3 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs2	2	Pipe 2 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out
dis_vs1	1	Pipe 1 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out

BITFIELD	BITS	DESCRIPTION	DECODE
dis_vs0	0	Pipe 0 disable VS: Disable the transmission of VS to MIPI output.	0b0: Enable VS out 0b1: Disable VS out

BACKTOP24 (0x437)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_OVRD_EN_4	ERRB_PKT_WC_OVRD_EN_3	ERRB_PKT_WC_OVRD_EN_2	ERRB_PKT_WC_OVRD_EN_1	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ERRB_PKT_WC_OVRD_EN_4	7	0 = Pick random word count from video source in pipe 4 as the word count for ERRB packets 1 = Use word count specified in ERRB_PKT_WC_4_H/L register as the word count for ERRB packets	0x0 0x1: See Description
ERRB_PKT_WC_OVRD_EN_3	6	0 = Pick random word count from video source in pipe 3 as the word count for ERRB packets 1 = Use word count specified in ERRB_PKT_WC_3_H/L register as the word count for ERRB packets	0x0 0x1: See Description
ERRB_PKT_WC_OVRD_EN_2	5	0 = Pick random word count from video source in pipe 2 as the word count for ERRB packets 1 = Use word count specified in ERRB_PKT_WC_2_H/L register as the word count for ERRB packets	0x0 0x1: See Description
ERRB_PKT_WC_OVRD_EN_1	4	0 = Pick random word count from video source in pipe 1 as the word count for ERRB packets 1 = Use word count specified in ERRB_PKT_WC_1_H/L register as the word count for ERRB packets	0x0 0x1: See Description

BACKTOP25 (0x438)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_1_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_1_H	7:0	If ERRB_PKT_WC_OVRD_EN_1 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP26 (0x439)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_1_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_1_L	7:0	If ERRB_PKT_WC_OVRD_EN_1 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP27 (0x43A)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_2_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_2_H	7:0	If ERRB_PKT_WC_OVRD_EN_2 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP28 (0x43B)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_2_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_2_L	7:0	If ERRB_PKT_WC_OVRD_EN_2 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP29 (0x43C)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_3_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_3_H	7:0	If ERRB_PKT_WC_OVRD_EN_3 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP30 (0x43D)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_3_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_3_L	7:0	If ERRB_PKT_WC_OVRD_EN_3 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP31 (0x43E)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_4_H[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_4_H	7:0	If ERRB_PKT_WC_OVRD_EN_4 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP32 (0x43F)

BIT	7	6	5	4	3	2	1	0
Field	ERRB_PKT_WC_4_L[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
ERRB_PKT_WC_4_L	7:0	If ERRB_PKT_WC_OVRD_EN_4 is set, this register sets the word count for ERRB packet. When not in WC override mode, this register reads back detected word count from incoming video used for ERRB packet.

BACKTOP33 (0x440)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	FIFO_EMPTY_3	FIFO_EMPTY_2	FIFO_EMPTY_1	FIFO_EMPTY_0
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
FIFO_EMPTY_3	3	Pipe 3 FIFO empty
FIFO_EMPTY_2	2	Pipe 2 FIFO empty

BITFIELD	BITS	DESCRIPTION
FIFO_EMPTY_1	1	Pipe 1 FIFO empty
FIFO_EMPTY_0	0	Pipe 0 FIFO empty

BACKTOP1_HDR_ERR (0x442)

BIT	7	6	5	4	3	2	1	0
Field	TUN_HDR_ERR_FLAG_0_OEN	TUN_HDR_ERR_FLAG_0	TUN_HDR_CRC_ERR_3_FLAG_0	TUN_HDR_CRC_ERR_2_FLAG_0	TUN_HDR_CRC_ERR_1_FLAG_0	TUN_HDR_CRC_ERR_0_FLAG_0	TUN_HDR_ECC_ERR_FLAG_0	TUN_HDR_ECC_FLAG_0
Reset	0b1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_HDR_ERR_FLAG_0_OEN	7	Pipe 0 tunneling mode header error flag going to ERRB pin output enable.	0b0: Disable reporting of header error flag (TUN_HDR_ERR_FLAG_1) at ERRB pin 0b1: Enable reporting of header error flag (TUN_HDR_ERR_FLAG_1) at ERRB pin
TUN_HDR_ERR_FLAG_0	6	Pipe 0 tunneling mode header error flag going to ERRB pin. This error flag takes 2-bit ECC error (bit 1 of same register) when in DPHY mode, logic AND of CPHY header 1 and 2 (bits 2 and 3 in same register) in 1-lane CPHY mode, and logic AND of CPHY header 1, 2, 3 and 4 (bits 2, 3, 4 and 5 in same register) in 2-lane CPHY mode. This flag is sticky (i.e., clear on read).	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_3_FLAG_0	5	Pipe 0 tunneling mode CPHY fourth header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_2_FLAG_0	4	Pipe 0 tunneling mode CPHY third header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_1_FLAG_0	3	Pipe 0 tunneling mode CPHY second header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_0_FLAG_0	2	Pipe 0 tunneling mode CPHY first header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_ERR_FLAG_0	1	Pipe 0 tunneling mode DPHY header 2-bit (uncorrectable) ECC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_FLAG_0	0	Pipe 0 tunneling mode DPHY header 1-bit (correctable) ECC error flag	0x0: no error detected 0x1: Error Detected

BACKTOP2_HDR_ERR (0x443)

BIT	7	6	5	4	3	2	1	0
Field	TUN_HDR_ERR_FLAG_1_OEN	TUN_HDR_ERR_FLAG_1	TUN_HDR_CRC_ERR_3_FLAG_1	TUN_HDR_CRC_ERR_2_FLAG_1	TUN_HDR_CRC_ERR_1_FLAG_1	TUN_HDR_CRC_ERR_0_FLAG_1	TUN_HDR_ECC_ERR_FLAG_1	TUN_HDR_ECC_FLAG_1
Reset	0b1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_HDR_ERR_FLAG_1_OEN	7	Pipe 1 tunneling mode header error flag going to ERRB pin output enable.	0b0: Disable reporting of header error flag (TUN_HDR_ERR_FLAG_2) at ERRB pin 0b1: Enable reporting of header error flag (TUN_HDR_ERR_FLAG_2) at ERRB pin
TUN_HDR_ERR_FLAG_1	6	Pipe 1 tunneling mode header error flag going to ERRB pin. This error flag takes 2-bit ECC error (bit 1 of same register) when in DPHY mode, logic AND of CPHY header 1 and 2 (bits 2 and 3 in same register) in 1-lane CPHY mode, and logic AND of CPHY header 1, 2, 3 and 4 (bits 2, 3, 4 and 5 in same register) in 2-lane CPHY mode. This flag is sticky (i.e., clear on read).	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_3_FLAG_1	5	Pipe 1 tunneling mode CPHY fourth header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_2_FLAG_1	4	Pipe 1 tunneling mode CPHY third header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_1_FLAG_1	3	Pipe 1 tunneling mode CPHY second header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_0_FLAG_1	2	Pipe 1 tunneling mode CPHY first header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_ERR_FLAG_1	1	Pipe 1 tunneling mode DPHY header 2-bit (uncorrectable) ECC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_FLAG_1	0	Pipe 1 tunneling mode DPHY header 1-bit (correctable) ECC error flag	0x0: no error detected 0x1: Error Detected

BACKTOP3_HDR_ERR (0x444)

BIT	7	6	5	4	3	2	1	0
Field	TUN_HDR_ERR_FLAG_2_OEN	TUN_HDR_ERR_FLAG_2	TUN_HDR_CRC_ERR_3_FLAG_2	TUN_HDR_CRC_ERR_2_FLAG_2	TUN_HDR_CRC_ERR_1_FLAG_2	TUN_HDR_CRC_ERR_0_FLAG_2	TUN_HDR_ECC_ERR_FLAG_2	TUN_HDR_ECC_FLAG_2
Reset	0b1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_HDR_ERR_FLAG_2_OEN	7	Pipe 2 tunneling mode header error flag going to ERRB pin output enable.	0b0: Disable reporting of header error flag (TUN_HDR_ERR_FLAG_3) at ERRB pin 0b1: Enable reporting of header error flag (TUN_HDR_ERR_FLAG_3) at ERRB pin
TUN_HDR_ERR_FLAG_2	6	Pipe 2 tunneling mode header error flag going to ERRB pin. This error flag takes 2-bit ECC error (bit 1 of same register) when in DPHY mode, logic AND of CPHY header 1 and 2 (bits 2 and 3 in same register) in 1-lane CPHY mode, and logic AND of CPHY header 1, 2, 3 and 4 (bits 2, 3, 4 and 5 in same register) in 2-lane CPHY mode. This flag is sticky (i.e., clear on read).	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_3_FLAG_2	5	Pipe 2 tunneling mode CPHY fourth header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_2_FLAG_2	4	Pipe 2 tunneling mode CPHY third header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_1_FLAG_2	3	Pipe 2 tunneling mode CPHY second header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_0_FLAG_2	2	Pipe 2 tunneling mode CPHY first header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_ERR_FLAG_2	1	Pipe 2 tunneling mode DPHY header 2-bit (uncorrectable) ECC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_FLAG_2	0	Pipe 2 tunneling mode DPHY header 1-bit (correctable) ECC error flag	0x0: no error detected 0x1: Error Detected

BACKTOP4_HDR_ERR (0x445)

BIT	7	6	5	4	3	2	1	0
Field	TUN_HDR_ERR_FLAG_3_OEN	TUN_HDR_ERR_FLAG_3	TUN_HDR_CRC_ERR_3_FLAG_3	TUN_HDR_CRC_ERR_2_FLAG_3	TUN_HDR_CRC_ERR_1_FLAG_3	TUN_HDR_CRC_ERR_0_FLAG_3	TUN_HDR_ECC_ERR_FLAG_3	TUN_HDR_ECC_FLAG_3
Reset	0b1	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_HDR_ERR_FLAG_3_OEN	7	Pipe 3 tunneling mode header error flag going to ERRB pin output enable.	0b0: Disable reporting of header error flag (TUN_HDR_ERR_FLAG_4) at ERRB pin 0b1: Enable reporting of header error flag (TUN_HDR_ERR_FLAG_4) at ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_HDR_ERR_FLAG_3	6	Pipe 3 tunneling mode header error flag going to ERRB pin. This error flag takes 2-bit ECC error (bit 1 of same register) when in DPHY mode, logic AND of CPHY header 1 and 2 (bits 2 and 3 in same register) in 1-lane CPHY mode, and logic AND of CPHY header 1, 2, 3 and 4 (bits 2, 3, 4 and 5 in same register) in 2-lane CPHY mode. This flag is sticky (i.e., clear on read).	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_3_FLAG_3	5	Pipe 3 tunneling mode CPHY fourth header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_2_FLAG_3	4	Pipe 3 tunneling mode CPHY third header CRC error flag. Obsolete when SER is in 1-lane CPHY mode.	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_1_FLAG_3	3	Pipe 3 tunneling mode CPHY second header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_CRC_ERR_0_FLAG_3	2	Pipe 3 tunneling mode CPHY first header CRC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_ERR_FLAG_3	1	Pipe 3 tunneling mode DPHY header 2-bit (uncorrectable) ECC error flag	0x0: no error detected 0x1: Error Detected
TUN_HDR_ECC_FLAG_3	0	Pipe 3 tunneling mode DPHY header 1-bit (correctable) ECC error flag	0x0: no error detected 0x1: Error Detected

BACKTOP39 (0x446)

BIT	7	6	5	4	3	2	1	0
Field	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP3_LINE_LEN_OVRD	BKTP2_LINE_LEN_OVRD	BKTP1_LINE_LEN_OVRD	BKTP0_LINE_LEN_OVRD
Reset	0x1	0x1	0x1	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
BKTP3_LINE_LEN_OVRD	7	Enable use of timeout timer for video masking. By default, the timer is set to wait 1/8th of a line. The time for a line is autodetected. Use BKTPx_VM_TIMEOUT_DIV to select between 1, 1/2, 1/4, or 1/8th of a line. Use BKTPx_VM_TIMEOUT_OVRD and BKTPx_VM_TIMEOUT registers to override timeout value in 3ns increments.	0x0: Disabled 0x1: Enabled
BKTP3_LINE_LEN_OVRD	6	Enable use of timeout timer for video masking	0x0: Disabled 0x1: Enabled
BKTP3_LINE_LEN_OVRD	5	Enable use of timeout timer for video masking	0x0: Disabled 0x1: Enabled
BKTP3_LINE_LEN_OVRD	4	Enable use of timeout timer for video masking	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
BKTP3_LINE_LEN_OVRD	3	Enable use of BKTPx_VM_TIMEOUT_H/L registers to assert video timeout masking in synchronous aggregation mode.	0x0: Disabled 0x1: Enabled
BKTP2_LINE_LEN_OVRD	2	Enable use of BKTPx_VM_TIMEOUT_H/L registers to assert video timeout masking in synchronous aggregation mode.	0x0: Disabled 0x1: Enabled
BKTP1_LINE_LEN_OVRD	1	Enable use of BKTPx_VM_TIMEOUT_H/L registers to assert video timeout masking in synchronous aggregation mode.	0x0: Disabled 0x1: Enabled
BKTP0_LINE_LEN_OVRD	0	Enable use of BKTPx_VM_TIMEOUT_H/L registers to assert video timeout masking in synchronous aggregation mode.	0x0: Disabled 0x1: Enabled

BACKTOP40 (0x447)

BIT	7	6	5	4	3	2	1	0
Field	BKTP0_LINE_LEN_H[7:0]							
Reset	0x7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP0_LINE_LEN_H	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP41 (0x448)

BIT	7	6	5	4	3	2	1	0
Field	BKTP0_LINE_LEN_L[7:0]							
Reset	0x53							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP0_LINE_LEN_L	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP42 (0x449)

BIT	7	6	5	4	3	2	1	0
Field	BKTP1_LINE_LEN_H[7:0]							
Reset	0x7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP1_LINE_LEN_H	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP43 (0x44A)

BIT	7	6	5	4	3	2	1	0
Field	BKTP1_LINE_LEN_L[7:0]							
Reset	0x53							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP1_LINE_LEN_L	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP44 (0x44B)

BIT	7	6	5	4	3	2	1	0
Field	BKTP2_LINE_LEN_H[7:0]							
Reset	0x7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP2_LINE_LEN_H	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP45 (0x44C)

BIT	7	6	5	4	3	2	1	0
Field	BKTP2_LINE_LEN_L[7:0]							
Reset	0x53							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP2_LINE_LEN_L	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP46 (0x44D)

BIT	7	6	5	4	3	2	1	0
Field	BKTP3_LINE_LEN_H[7:0]							
Reset	0x7							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP3_LINE_LEN_H	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP47 (0x44E)

BIT	7	6	5	4	3	2	1	0
Field	BKTP3_LINE_LEN_L[7:0]							
Reset	0x53							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
BKTP3_LINE_LEN_L	7:0	Used to assert video timeout masking in tunneling mode in synchronous aggregation (Wx4H) mode. If video is detected in other aggregated pipes and current pipe does not receive video in the specified timeout time, current pipe will be masked until video resumes at the beginning of a frame. Value specified in this register is in 2.67ns increments.

BACKTOP48 (0x44F)

BIT	7	6	5	4	3	2	1	0
Field	BKTP4_VM_TIMEOUT_DIV[1:0]		BKTP3_VM_TIMEOUT_DIV[1:0]		BKTP2_VM_TIMEOUT_DIV[1:0]		BKTP1_VM_TIMEOUT_DIV[1:0]	
Reset	0x3		0x3		0x3		0x3	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
BKTP4_VM_TIMEOUT_DIV	7:6	Selects between 1, 3/4, 1/2, or 1/4 of a line.	0x0: 1/4 of a line 0x1: 1/2 of a line 0x2: 3/4 of a line 0x3: 1 line
BKTP3_VM_TIMEOUT_DIV	5:4	Selects between 1, 3/4, 1/2, or 1/4 of a line.	0x0: 1/4 of a line 0x1: 1/2 of a line 0x2: 3/4 of a line 0x3: 1 line
BKTP2_VM_TIMEOUT_DIV	3:2	Selects between 1, 3/4, 1/2, or 1/4 of a line.	0x0: 1/4 of a line 0x1: 1/2 of a line 0x2: 3/4 of a line 0x3: 1 line

BITFIELD	BITS	DESCRIPTION	DECODE
BKTP1_VM_TIMEOUT_DIV	1:0	Selects between 1, 3/4, 1/2, or 1/4 of a line.	0x0: 1/4 of a line 0x1: 1/2 of a line 0x2: 3/4 of a line 0x3: 1 line

BACKTOP_EMBED0 (0x450)

BIT	7	6	5	4	3	2	1	0
Field	EMBED_LL_EN_BKTP0	–	EMBED_LL_NUM_BKTP0 [1:0]		EMBED_FL_EN_BKTP0	–	EMBED_FL_NUM_BKTP0 [1:0]	
Reset	0b0	–	0b0		0b0	–	0b0	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EMBED_LL_EN_BKTP0	7	Enable conversion of last few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP0 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_LL_NUM_BKTP0	5:4	When the embedded packet type is enabled to be located in the last few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP0 only. See the EMBED_LL_EN_BKTP0 register bit. 2'b00 - Use Last Line 2'b01- Use Second from Last Line 2'b10 - Use Third from Last Line 2'b11 - Use Fourth from Last Line	0x0 0x1: See Description
EMBED_FL_EN_BKTP0	3	Enable conversion of first few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP0 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_FL_NUM_BKTP0	1:0	When the embedded packet type is enabled to be located in the first few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP0 only. See the EMBED_FL_EN_BKTP0 register bit. 2'b00- Use first line. 2'b01- Use second line. 2'b10- Use third line 2'b11- Use fourth line	0x0 0x1: See Description

BACKTOP_EMBED1 (0x451)

BIT	7	6	5	4	3	2	1	0
Field	EMBED_LL_EN_BKTP1	–	EMBED_LL_NUM_BKTP1 [1:0]		EMBED_FL_EN_BKTP1	–	EMBED_FL_NUM_BKTP1 [1:0]	
Reset	0b0	–	0b0		0b0	–	0b0	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EMBED_LL_EN_BKTP1	7	Enable conversion of last few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP1 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_LL_NUM_BKTP1	5:4	When the embedded packet type is enabled to be located in the last few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP1 only. See the EMBED_LL_EN_BKTP1 register bit. 2'b00 - Use Last Line 2'b01- Use Second from Last Line 2'b10 - Use Third from Last Line 2'b11 - Use Fourth from Last Line	0x0 0x1: See Description
EMBED_FL_EN_BKTP1	3	Enable conversion of first few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP1 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_FL_NUM_BKTP1	1:0	When the embedded packet type is enabled to be located in the first few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP1 only. See the EMBED_FL_EN_BKTP1 register bit. 2'b00- Use first line. 2'b01- Use second line. 2'b10- Use third line 2'b11- Use fourth line	0x0 0x1: See Description

BACKTOP_EMBED2 (0x452)

BIT	7	6	5	4	3	2	1	0
Field	EMBED_LL_EN_BKTP2	–	EMBED_LL_NUM_BKTP2 [1:0]		EMBED_FL_EN_BKTP2	–	EMBED_FL_NUM_BKTP2 [1:0]	
Reset	0b0	–	0b0		0b0	–	0b0	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EMBED_LL_EN_BKTP2	7	Enable conversion of last few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP2 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_LL_NUM_BKTP2	5:4	When the embedded packet type is enabled to be located in the last few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP2 only. See the EMBED_LL_EN_BKTP2 register bit. 2'b00 - Use Last Line 2'b01- Use Second from Last Line 2'b10 - Use Third from Last Line 2'b11 - Use Fourth from Last Line	0x0 0x1: See Description
EMBED_FL_EN_BKTP2	3	Enable conversion of first few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP02only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_FL_NUM_BKTP2	1:0	When the embedded packet type is enabled to be located in the first few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP2 only. See the EMBED_FL_EN_BKTP2 register bit. 2'b00- Use first line. 2'b01- Use second line. 2'b10- Use third line 2'b11- Use fourth line	0x0 0x1: See Description

BACKTOP_EMBED3 (0x453)

BIT	7	6	5	4	3	2	1	0
Field	EMBED_LL_EN_BKTP3	–	EMBED_LL_NUM_BKTP3[1:0]		EMBED_FL_EN_BKTP3	–	EMBED_FL_NUM_BKTP3[1:0]	
Reset	0b0	–	0b0		0b0	–	0b0	
Access Type	Write, Read	–	Write, Read		Write, Read	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
EMBED_LL_EN_BKTP3	7	Enable conversion of last few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP3 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
EMBED_LL_NUM_BKTP3	5:4	When the embedded packet type is enabled to be located in the last few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP3 only. See the EMBED_LL_EN_BKTP3 register bit. 2'b00 - Use Last Line 2'b01- Use Second from Last Line 2'b10 - Use Third from Last Line 2'b11 - Use Fourth from Last Line	0x0 0x1: See Description
EMBED_FL_EN_BKTP3	3	Enable conversion of first few pixel lines of each frame into MIPI embedded data type. Applies to MIPI BACKTOP3 only. 0: Disable 1: Enable	0x0: Disabled 0x1: Enabled
EMBED_FL_NUM_BKTP3	1:0	When the embedded packet type is enabled to be located in the first few lines of each frame, this register field sets the line number to be used for the converted embedded data type. Applies to MIPI BACKTOP3 only. See the EMBED_FL_EN_BKTP3 register bit. 2'b00- Use first line. 2'b01- Use second line. 2'b10- Use third line. 2'b11- Use fourth line.	0x0 0x1: See Description

CMD_LMO_ERRB_EN (0x454)

BIT	7	6	5	4	3	2	1	0
Field	CMD_OVFL_3_ERRB_OEN	CMD_OVFL_2_ERRB_OEN	CMD_OVFL_1_ERRB_OEN	CMD_OVFL_0_ERRB_OEN	LMO_3_ERRB_OEN	LMO_2_ERRB_OEN	LMO_1_ERRB_OEN	LMO_0_ERRB_OEN
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CMD_OVFL_3_ERRB_OEN	7	Enable Pipe 3 command FIFO overflow Status on ERRB output	0x0: Disabled 0x1: Enabled
CMD_OVFL_2_ERRB_OEN	6	Enable Pipe 2 command FIFO overflow Status on ERRB output	0x0: Disabled 0x1: Enabled
CMD_OVFL_1_ERRB_OEN	5	Enable Pipe 1 command FIFO overflow Status on ERRB output	0x0: Disabled 0x1: Enabled
CMD_OVFL_0_ERRB_OEN	4	Enable Pipe 0 command FIFO overflow Status on ERRB output	0x0: Disabled 0x1: Enabled
LMO_3_ERRB_OEN	3	Enable Pipe 3 line memory overflow status on ERRB output. See the LMO_3_ERRB_EN to enable output of this status to the ERRB pin	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
LMO_2_ERRB_OEN	2	Enable Pipe 2 line memory overflow status on ERRB output. See the LMO_2_ERRB_EN to enable output of this status to the ERRB pin	0x0: Disabled 0x1: Enabled
LMO_1_ERRB_OEN	1	Enable Pipe 1 line memory overflow status on ERRB output See the LMO_1_ERRB_EN to enable output of this status to the ERRB pin	0x0: Disabled 0x1: Enabled
LMO_0_ERRB_OEN	0	Enable Pipe 0 line memory overflow status on ERRB output.	0x0: Disabled 0x1: Enabled

DPLL_ERRB_OEN (0x455)

BIT	7	6	5	4	3	2	1	0
Field	CSIPLL3_LOL_STICKY_FLAG	CSIPLL2_LOL_STICKY_FLAG	CSIPLL1_LOL_STICKY_FLAG	CSIPLL0_LOL_STICKY_FLAG	CSI_DPLL3_ERRB_OEN	CSI_DPLL2_ERRB_OEN	CSI_DPLL1_ERRB_OEN	CSI_DPLL0_ERRB_OEN
Reset	0x0	0x0	0x0	0x0	0b1	0b1	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL3_LOL_STICKY_FLAG	7	CSIPLL3 Loss of lock ERRB Flag. This flag is the sticky bit output for the CSIPLL3 Loss of Lock and is directly associated with the CSIPLL3_LOCK register bit. The CSIPLL3_LOCK status data is live data, however, this bit is intended to catch a loss of lock event and will maintain that information until this register bit is cleared. This register bit is cleared upon reading. This register information is also reflected onto the ERRB pin unless otherwise disabled from doing so. See the CSI_DPLL3_ERRB_OEN register.	0x0: no error detected 0x1: Error Detected
CSIPLL2_LOL_STICKY_FLAG	6	CSIPLL2 Loss of Lock ERRB Flag. This flag is the sticky bit output for the CSIPLL2 Loss of Lock and is directly associated with the CSIPLL2_LOCK register bit. The CSIPLL2_LOCK status data is live data; however, this bit is intended to catch a loss of lock event and will maintain that information until this register bit is cleared. This register bit is cleared upon reading. This register information is also reflected onto the ERRB pin unless otherwise disabled from doing so. See the CSI_DPLL2_ERRB_OEN register.	0x0: no error detected 0x1: Error Detected

BITFIELD	BITS	DESCRIPTION	DECODE
CSIPLL1_LOL_STICKY_FLAG	5	CSIPLL1 Loss of Lock ERRB Flag. This flag is the sticky bit output for the CSIPLL1 Loss of Lock and is directly associated with the CSIPLL1_LOCK register bit. The CSIPLL1_LOCK status data is live data; however, this bit is intended to catch a loss of lock event and will maintain that information until this register bit is cleared. This register bit is cleared upon reading. This register information is also reflected onto the ERRB pin unless otherwise disabled from doing so. See the CSI_DPLL1_ERRB_OEN register.	0x0: no error detected 0x1: Error Detected
CSIPLL0_LOL_STICKY_FLAG	4	CSIPLL0 Loss of Lock ERRB Flag. This flag is the sticky bit output for the CSIPLL0 Loss of Lock and is directly associated with the CSIPLL0_LOCK register bit. The CSIPLL0_LOCK status data is live data; however, this bit is intended to catch a loss of lock event and will maintain that information until this register bit is cleared. This register bit is cleared upon reading. This register information is also reflected onto the ERRB pin unless otherwise disabled from doing so. See the CSI_DPLL0_ERRB_OEN register.	0x0: no error detected 0x1: Error Detected
CSI_DPLL3_ERRB_OEN	3	Enable CSI DPLL 3 Loss of Lock status on ERRB output. See the CSIPLL3_LOCK status output register bit and the CSIPLL3_LOL_STICKY_FLAG register bit.	0x0: Disabled 0x1: Enabled
CSI_DPLL2_ERRB_OEN	2	Enable CSI DPLL 2 Loss of Lock status on ERRB output. See the CSIPLL2_LOCK status output register bit and the CSIPLL2_LOL_STICKY_FLAG register bit.	0x0: Disabled 0x1: Enabled
CSI_DPLL1_ERRB_OEN	1	Enable CSI DPLL 1 Loss of Lock status on ERRB output. See the CSIPLL1_LOCK status output register bit and the CSIPLL1_LOL_STICKY_FLAG register bit.	0x0: Disabled 0x1: Enabled
CSI_DPLL0_ERRB_OEN	0	Enable CSI DPLL 0 Loss of Lock status on ERRB output. See the CSIPLL0_LOCK status output register bit and the CSIPLL0_LOL_STICKY_FLAG register bit.	0x0: Disabled 0x1: Enabled

BACKTOP_OVERRIDE_BPP_DT (0x456)

BIT	7	6	5	4	3	2	1	0
Field	OVERRIDE_VC_3	OVERRIDE_VC_2	OVERRIDE_VC_1	OVERRIDE_VC_0	OVERRIDE_BPP_DT_3	OVERRIDE_BPP_DT_2	OVERRIDE_BPP_DT_1	OVERRIDE_BPP_DT_0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OVERRIDE_VC_3	7	This register allows software override of VC only, similar to override_bpp_vc_dt_#. Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Disable 0x1: Enable
OVERRIDE_VC_2	6	This register allows software override of VC only, similar to override_bpp_vc_dt_#. Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Disable 0x1: Enable
OVERRIDE_VC_1	5	This register allows software override of VC only, similar to override_bpp_vc_dt_#. Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
OVERRIDE_VC_0	4	This register allows software override of VC only, similar to override_bpp_vc_dt_#. Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over the OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Disable 0x1: Enable
OVERRIDE_BPP_DT_3	3	This register allows software override of BPP and DT only, similar to override_bpp_vc_dt_#.	0x0: Disable 0x1: Enable
OVERRIDE_BPP_DT_2	2	This register allows software override of BPP and DT only, similar to override_bpp_vc_dt_#.	0x0: Disable 0x1: Enable
OVERRIDE_BPP_DT_1	1	This register allows software override of BPP and DT only, similar to override_bpp_vc_dt_#.	0x0: Disable 0x1: Enable
OVERRIDE_BPP_DT_0	0	This register allows software override of BPP and DT only, similar to override_bpp_vc_dt_#.	0x0: Disable 0x1: Enable

BACKTOP_OVERRIDE_VC (0x457)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	OVERRIDE_VC_BITS_2_AND_3
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
OVERRIDE_VC_BITS_2_AND_3	0	Override VC [3:2] such that VCs for each pipe start with 4'h0, 4'h4,4'h8, and 4'hC respectively. VC bits [1:0] are still passed through. Notes: • Control registers, override_bpp_vc_dt_# and/or OVERRIDE_VC_# have priority over this OVERRIDE_VC_BITS_2_AND_3 register. • ERRB_PKT_VC_OVRD_EN has priority over override_bpp_vc_dt_#, OVERRIDE_VC_#, and/or OVERRIDE_VC_BITS_2_AND_3 for errb_pkts	0x0: Disable 0x1: Enable

SRAM_LCRC_ERR (0x458)

BIT	7	6	5	4	3	2	1	0
Field	SRAM_LCRC_ERR_OEN_3	SRAM_LCRC_ERR_OEN_2	SRAM_LCRC_ERR_OEN_1	SRAM_LCRC_ERR_OEN_0	SRAM_LCRC_ERR_3	SRAM_LCRC_ERR_2	SRAM_LCRC_ERR_1	SRAM_LCRC_ERR_0
Reset	0x1	0x1	0x1	0x1	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
SRAM_LCRC_ERR_OEN_3	7	SRAM Line CRC Error Ouput Enable.
SRAM_LCRC_ERR_OEN_2	6	SRAM Line CRC Error Ouput Enable.
SRAM_LCRC_ERR_OEN_1	5	SRAM Line CRC Error Ouput Enable.
SRAM_LCRC_ERR_OEN_0	4	SRAM Line CRC Error Ouput Enable.
SRAM_LCRC_ERR_3	3	SRAM Line CRC Error Detection. Compares CRC value of data written to the Video Line SRAM vs CRC value of data read out of the Video Line SRAM.
SRAM_LCRC_ERR_2	2	SRAM Line CRC Error Detection. Compares CRC value of data written to the Video Line SRAM vs CRC value of data read out of the Video Line SRAM.
SRAM_LCRC_ERR_1	1	SRAM Line CRC Error Detection. Compares CRC value of data written to the Video Line SRAM vs CRC value of data read out of the Video Line SRAM.
SRAM_LCRC_ERR_0	0	SRAM Line CRC Error Detection. Compares CRC value of data written to the Video Line SRAM vs CRC value of data read out of the Video Line SRAM.

SRAM_LCRC_EN (0x459)

BIT	7	6	5	4	3	2	1	0
Field	SRAM_LCRC_TUN_CHK_DIS_3	SRAM_LCRC_TUN_CHK_DIS_2	SRAM_LCRC_TUN_CHK_DIS_1	SRAM_LCRC_TUN_CHK_DIS_0	SRAM_LCRC_PIXEL_CHK_DIS_3	SRAM_LCRC_PIXEL_CHK_DIS_2	SRAM_LCRC_PIXEL_CHK_DIS_1	SRAM_LCRC_PIXEL_CHK_DIS_0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SRAM_LCRC_TUN_CHK_DIS_3	7	SRAM Line CRC Tunnel Mode Check Disable
SRAM_LCRC_TUN_CHK_DIS_2	6	SRAM Line CRC Tunnel Mode Check Disable
SRAM_LCRC_TUN_CHK_DIS_1	5	SRAM Line CRC Tunnel Mode Check Disable
SRAM_LCRC_TUN_CHK_DIS_0	4	SRAM Line CRC Tunnel Mode Check Disable
SRAM_LCRC_PIXEL_CHK_DIS_3	3	SRAM Line CRC Pixel Mode Check Disable
SRAM_LCRC_PIXEL_CHK_DIS_2	2	SRAM Line CRC Pixel Mode Check Disable

BITFIELD	BITS	DESCRIPTION
SRAM_LCRC_PIXEL_CHK_DIS_1	1	SRAM Line CRC Pixel Mode Check Disable
SRAM_LCRC_PIXEL_CHK_DIS_0	0	SRAM Line CRC Pixel Mode Check Disable

SRAM_LCRC_RESET (0x45A)

BIT	7	6	5	4	3	2	1	0
Field	INIT_SRAM_LCRC_ERR_DIS_3	INIT_SRAM_LCRC_ERR_DIS_2	INIT_SRAM_LCRC_ERR_DIS_1	INIT_SRAM_LCRC_ERR_DIS_0	SRAM_LCRC_MATCH_RESET_3	SRAM_LCRC_MATCH_RESET_2	SRAM_LCRC_MATCH_RESET_1	SRAM_LCRC_MATCH_RESET_0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
INIT_SRAM_LCRC_ERR_DIS_3	7	Initial SRAM Line CRC Error Disable. Disables requirement for SRAM Line CRC Match within first 3 lines written to memory.
INIT_SRAM_LCRC_ERR_DIS_2	6	Initial SRAM Line CRC Error Disable. Disables requirement for SRAM Line CRC Match within first 3 lines written to memory.
INIT_SRAM_LCRC_ERR_DIS_1	5	Initial SRAM Line CRC Error Disable. Disables requirement for SRAM Line CRC Match within first 3 lines written to memory.
INIT_SRAM_LCRC_ERR_DIS_0	4	Initial SRAM Line CRC Error Disable. Disables requirement for SRAM Line CRC Match within first 3 lines written to memory.
SRAM_LCRC_MATCH_RESET_3	3	SRAM Line CRC Match Reset. Setting this bit to a logic 1 will reset internal register such that if another LCRC Match does not occur within 3 video lines, an SRAM LCRC Error will occur. Orthogonal Safety Check. Self-clearing register.
SRAM_LCRC_MATCH_RESET_2	2	SRAM Line CRC Match Reset. Setting this bit to a logic 1 will reset internal register such that if another LCRC Match does not occur within 3 video lines, an SRAM LCRC Error will occur. Orthogonal Safety Check. Self-clearing register.
SRAM_LCRC_MATCH_RESET_1	1	SRAM Line CRC Match Reset. Setting this bit to a logic 1 will reset internal register such that if another LCRC Match does not occur within 3 video lines, an SRAM LCRC Error will occur. Orthogonal Safety Check. Self-clearing register.
SRAM_LCRC_MATCH_RESET_0	0	SRAM Line CRC Match Reset. Setting this bit to a logic 1 will reset internal register such that if another LCRC Match does not occur within 3 video lines, an SRAM LCRC Error will occur. Orthogonal Safety Check. Self-clearing register.

BKTOP_ERR_INJ_1 (0x480)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SRAM_LCRC_ERR_INJ_DIS_3	SRAM_LCRC_ERR_INJ_DIS_2	SRAM_LCRC_ERR_INJ_DIS_1	SRAM_LCRC_ERR_INJ_DIS_0
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SRAM_LCRC_ERR_INJ_DIS_3	3	SRAM Line CRC Error Injection Disable
SRAM_LCRC_ERR_INJ_DIS_2	2	SRAM Line CRC Error Injection Disable
SRAM_LCRC_ERR_INJ_DIS_1	1	SRAM Line CRC Error Injection Disable
SRAM_LCRC_ERR_INJ_DIS_0	0	SRAM Line CRC Error Injection Disable

MEM_ERR_INJ_1BIT (0x481)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEM_ERR_INJ_1BIT_BKTP4	MEM_ERR_INJ_1BIT_BKTP3	MEM_ERR_INJ_1BIT_BKTP2	MEM_ERR_INJ_1BIT_BKTP1
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ERR_INJ_1BIT_BKTP4	3	Inject one 1-bit error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one-time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_1BIT_BKTP3	2	Inject one 1-bit error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_1BIT_BKTP2	1	Inject one 1-bit error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_1BIT_BKTP1	0	Inject one 1-bit error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error

MEM_ERR_INJ_2BIT (0x482)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEM_ERR_INJ_2BIT_BKTP4	MEM_ERR_INJ_2BIT_BKTP3	MEM_ERR_INJ_2BIT_BKTP2	MEM_ERR_INJ_2BIT_BKTP1
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ERR_INJ_2BIT_BKTP4	3	Inject 2-bits of error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_2BIT_BKTP3	2	Inject 2-bits of error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_2BIT_BKTP2	1	Inject 2-bits of error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error
MEM_ERR_INJ_2BIT_BKTP1	0	Inject 2-bits of error into each word (MEM_ERR_INJ_WORD_LOC and MEM_ERR_INJ_WORD2_LOC) when word locations are enabled. Errors are injected one time into the packet number specified in MEM_ERR_INJ_PKT_NUM.	0x0: Normal operation 0x1: Inject error

MEM_ERR_INJ_WORD_LOC_EN (0x483)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MEM_ERR_INJ_WORD_LOC_2_EN	MEM_ERR_INJ_WORD_LOC_1_EN
Reset	–	–	–	–	–	–	0x0	0x1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MEM_ERR_INJ_WORD_LOC_2_EN	1	Enables second memory error injection word location	0x0: Injection Disabled 0x1: Injection Enabled
MEM_ERR_INJ_WORD_LOC_1_EN	0	Enables memory error injection word location	0x0: Injection Disabled 0x1: Injection Enabled

MEM_ERR_INJ_WORD_LOC_1 (0x484)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ERR_INJ_WORD_LOC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MEM_ERR_INJ_WORD_LOC_1	7:0	Set word (24-bits) count location to inject 1-bit or 2-bit errors. Errors are injected on bit locations specified by MEM_ERR_INJ_BIT_LOC and MEM_ERR_INJ_BIT2_LOC. In pixel mode, errors can only be injected into pixel data. In tunnel mode:

	Inject Header Error	Inject Pixel Error
DPHY	< 2	≥ 2
CPHY 1-lane	< 4	≥ 4
CPHY 2-lanes	< 8	≥ 8

MEM_ERR_INJ_WORD_LOC_2 (0x485)

BIT	7	6	5	4	3	2	1	0
Field	MEM_ERR_INJ_WORD_LOC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
MEM_ERR_INJ_WORD_LOC_2	7:0	Set second word (24-bits) count location to inject 1-bit or 2-bit errors. Errors are injected on bit locations specified in MEM_ERR_INJ_BIT_LOC and MEM_ERR_INJ_BIT2_LOC. In pixel mode, errors can only be injected into pixel data. In tunnel mode:

	Inject Header Error	Inject Pixel Error
DPHY	< 2	≥ 2
CPHY 1-lane	< 4	≥ 4
CPHY 2-lanes	< 8	≥ 8

Enabling word2_loc can result in a total of 4-bits of errors injected.

MEM_ERR_INJ_PKT_NUM (0x486)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEM_ERR_INJ_PKT_NUM[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
MEM_ERR_INJ_PKT_NUM	3:0	Sets the packet to inject 1-bit or 2-bit errors. Packet is counted from the next frame-start packet after MEM_ERR_INJ_1/2_BIT_BKTPx is set .

MEM_ERR_INJ_BIT1_LOC (0x487)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEM_ERR_INJ_BIT1_LOC[4:0]				
Reset	–	–	–	0x03				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
MEM_ERR_INJ_BIT1_LOC	4:0	Specify bit location to inject 1-bit error on a 24-bit bus. Min = 0, Max = 23. If set to more than 23, no error will be injected. Bit and Bit 2 locations are used by both word locations.

MEM_ERR_INJ_BIT2_LOC (0x488)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEM_ERR_INJ_BIT2_LOC[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
MEM_ERR_INJ_BIT2_LOC	4:0	Specify second bit location to inject 2-bit error on a 24-bit bus. Min = 0, Max = 23. If set to more than 23, no error will be injected. Bit and bit 2 locations are used by both word locations.

FSYNC_0 (0x4A0)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	FSYNC_OUT_PIN	EN_VS_GEN	FSYNC_MODE[1:0]		FSYNC_METH[1:0]	
Reset	0x0	0x0	0b0	0x0	0x3		0x0	
Access Type			Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_OUT_PIN	5	Selects pin to output frame sync signal (effective only when FSYNC_METH = 01)	0b0: MFP0 0b1: MFP7
EN_VS_GEN	4	Selects whether or not VS is generated internally by the frame sync generator (not effective when FSYNC_MODE = 11)	0b0: VS is not generated internally by the frame sync generator 0b1: VS is generated internally by the frame sync generator

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_MODE	3:2	Frame Synchronization Mode	0b00: Frame sync generation is on. GPIO is not used as FSYNC input or output 0b01: Frame sync generation is on. GPIO is used as FSYNC output and drives a slave device 0b10: Frame sync generation is off. GPIO is used as FSYNC input driven by a master device for GMSL1 links. Any enabled GPIO input can be used as FSYNC input for GMSL2 links. 0b11: Frame sync generation is off. GPIO is not used as FSYNC input or output
FSYNC_METH	1:0	Frame Synchronization Method	0b00: Manual 0b01: Semi-auto 0b10: Auto 0b11: Reserved

FSYNC_1 (0x4A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		RSVD[1:0]		FSYNC_PER_DIV[3:0]			
Reset	0x0		0x0		0x0			
Access Type					Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PER_DIV	3:0	Frame sync transmission period in terms of VSYNC periods	0x0: 1 0x1: 2 0x2: 3 0x3: 6 0x4: 8 0x5: 10 0x6: 12 0x7: 16 0x8: 20 0x9: 24 0xA: 32 0xB: 48 0xC: 64 0xD: 80 0xE: 96 0xF: 128

FSYNC_2 (0x4A2)

BIT	7	6	5	4	3	2	1	0
Field	MST_LINK_SEL[2:0]			K_VAL_SIGN	K_VAL[3:0]			
Reset	0x4			0x0	0x1			
Access Type	Write, Read			Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
MST_LINK_SEL	7:5	Master link select for frame sync generation	0b000: Video 0 0b001: Video 1 0b010: Video 2 0b011: Video 3 0b100: Auto select 0b101: Auto select 0b110: Auto select 0b111: Auto select
K_VAL_SIGN	4	Sign bit of K_VAL	0b0: K_VAL is positive 0b1: K_VAL is negative
K_VAL	3:0	Desired frame sync margin with respect to either the VSYNC of the slowest link in automatic mode or the VSYNC of the master link in semi-automatic mode.	0x0: 0.85µs 0x1: 1.71µs 0x2: 2.56µs 0x3: 3.41µs 0x4: 4.27µs 0x5: 5.12µs 0x6: 5.97µs 0x7: 6.83µs 0x8: 8.53µs 0x9: 10.24µs 0xA: 11.95µs 0xB: 13.65µs 0xC: 17.07µs 0xD: 20.48µs 0xE: 23.89µs 0xF: 27.31µs

FSYNC_3 (0x4A3)

BIT	7	6	5	4	3	2	1	0
Field	P_VAL_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_L	7:0	Low byte of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the master link in semi-automatic mode	0bXXXXXXXX: Low byte of desired frame sync margin

FSYNC_4 (0x4A4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	P_VAL_SIGN	P_VAL_H[4:0]				
Reset	–	–	0x0	0x00				
Access Type	–	–	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_SIGN	5	Sign bit of P_VAL	0b0: P_VAL is positive 0b1: P_VAL is negative

BITFIELD	BITS	DESCRIPTION	DECODE
P_VAL_H	4:0	High bits of desired frame sync margin in terms of PCLK cycles with respect to the VSYNC of the slowest link in automatic mode or with respect to the VSYNC of the master link in semi-automatic mode	0bXXXXX: High bits of desired frame sync margin

FSYNC_5 (0x4A5)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_L	7:0	Low byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: Low byte of number of PLCK cycles in FSYNC period

FSYNC_6 (0x4A6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_M	7:0	Middle byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: Middle byte of number of PLCK cycles in FSYNC period

FSYNC_7 (0x4A7)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_PERIOD_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_PERIOD_H	7:0	High byte of frame sync period in terms of pixel clock (effective when FSYNC_METH = 00 and FSYNC_MODE = 0x)	0xXX: High byte of number of PLCK cycles in FSYNC period

FSYNC_8 (0x4A8)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_ERR_THR_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_L	7:0	Low byte of the error threshold for the difference between the earliest and latest VSYNCs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0xXX: Low byte of number of PLCK cycles in VSYNC error threshold

FSYNC_9 (0x4A9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRM_DIFF_ERR_THR_H[4:0]				
Reset	–	–	–	0x0F				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_ERR_THR_H	4:0	High bits of the error threshold for the difference between the earliest and latest VSYNCs in terms of PCLK cycles (default is 40µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0bXXXXX: High bits of number of PLCK cycles in VSYNC error threshold

FSYNC_10 (0x4AA)

BIT	7	6	5	4	3	2	1	0
Field	OVLP_WINDOW_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
OVLP_WINDOW_L	7:0	Low byte of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0xXX: Low byte of number of PCLK cycles in the VSYNC-FSYNC overlap window

FSYNC_11 (0x4AB)

BIT	7	6	5	4	3	2	1	0
Field	EN_FSIN_LAST	–	–	OVLP_WINDOW_H[4:0]				
Reset	0x0	–	–	0x00				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EN_FSIN_LAST	7	When set to 0, FSIN can occur anywhere with respect to VS rising edges When set to 1, FSIN should occur after all VS rising edges	0b0: FSIN can occur anywhere with respect to VS rising edges 0b1: FSIN occurs after all rising edges
OVLP_WINDOW_H	4:0	High bits of the overlap window value in terms of PCLK cycles (default is 60µs for 96MHz PCLK) (disabled when all 13 bits are 0's)	0bXXXXX: High bits of number of PCLK cycles in the VSYNC-FSYNC overlap window

FSYNC_15 (0x4AF)

BIT	7	6	5	4	3	2	1	0
Field	FS_GPIO_TYPE	FS_USE_XTAL	–	AUTO_FS_LINKS	FS_LINK_3	FS_LINK_2	FS_LINK_1	FS_LINK_0
Reset	0x1	0x1	–	0x0	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FS_GPIO_TYPE	7	Selects the type of FSYNC signal to output from GPIO	0b0: GSML1 type 0b1: GMSL2 type
FS_USE_XTAL	6	Uses crystal oscillator clock for generating frame sync signal	0b0: Disabled 0b1: Enabled
AUTO_FS_LINKS	4	Selects how links are selected for frame sync generation	0b0: Include links selected by FS_LINK_x register bits in frame sync generation 0b1: Include all enabled links in frame sync generation
FS_LINK_3	3	Includes Video Pipe 3 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 3 in frame sync generation 0b1: Include Video Pipe 3 in frame sync generation
FS_LINK_2	2	Includes Video Pipe 2 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 2 in frame sync generation 0b1: Include Video Pipe 2 in frame sync generation
FS_LINK_1	1	Includes Video Pipe 1 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 1 in frame sync generation 0b1: Include Video Pipe 1 in frame sync generation
FS_LINK_0	0	Includes Video Pipe 0 in frame sync generation This is used only if AUTO_FS_LINKS = 0	0b0: Do not include Video Pipe 0 in frame sync generation 0b1: Include Video Pipe 0 in frame sync generation

FSYNC_16 (0x4B0)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_ERR_CNT	7:0	Frame Sync Error Counter (resets to 0 when read or when FSYNC_LOCKED (0x4B6) goes high)	0xXX: Number of frame sync errors detected since last error counter reset

FSYNC_17 (0x4B1)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_TX_ID[4:0]					FSYNC_ERR_THR[2:0]		
Reset	0x1E					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_TX_ID	7:3	GPIO ID used for transmitting FSYNC signal	0bXXXXX: GPIO ID associated with FSYNC transmission
FSYNC_ERR_THR	2:0	Frame sync error reporting threshold. FSYNC_ERR_FLAG is asserted when FSYNC_ERR_CNT ≥ FSYNC_ERR_THR.	0b000: 1 error 0b001: 2 errors 0b010: 4 errors 0b011: 8 errors 0b100: 16 errors 0b101: 32 errors 0b110: 64 errors 0b111: 128 errors

FSYNC_18 (0x4B2)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_L	7:0	Low byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: Low byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode.

FSYNC_19 (0x4B3)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_M[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_M	7:0	Middle byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: Middle byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode

FSYNC_20 (0x4B4)

BIT	7	6	5	4	3	2	1	0
Field	CALC_FRM_LEN_H[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CALC_FRM_LEN_H	7:0	High byte of calculated VS period of master link in terms of pixel clock in automatic or semi-automatic synchronization mode (Use when FSYNC_METH = 10 and FSYNC_MODE = 0x)	0xXX: High byte of number of PCLKs in VS period in master link auto or semi-auto synchronization mode

FSYNC_21 (0x4B5)

BIT	7	6	5	4	3	2	1	0
Field	FRM_DIFF_L[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
FRM_DIFF_L	7:0	Low byte of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0xXX: Low byte of the difference between the fastest and the slowest frame

FSYNC_22 (0x4B6)

BIT	7	6	5	4	3	2	1	0
Field	FSYNC_LOSS_OF_LOCK	FSYNC_LOCKED	FRM_DIFF_H[5:0]					
Reset	0x0	0x0	0x00					
Access Type	Read Clears All	Read Only	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_LOSS_OF_LOCK	7	Frame Synchronization Lost Lock This bit is set to 1 when frame synchronization loses lock. It is cleared when read.	0b0: Frame synchronization loss of lock has not been detected or has been cleared by a previous read operation 0b1: Frame synchronization loss of lock has been detected
FSYNC_LOCKED	6	Frame Synchronization Lock	0b0: Frame synchronization is not locked 0b1: Frame synchronization is locked
FRM_DIFF_H	5:0	High bits of the difference between the fastest and the slowest frame in terms of master PCLK cycles	0bXXXXX: High bits of the difference between the fastest and the slowest frame

FSYNC_23 (0x4B7)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	FSYNC_RST_MODE	–	RSVD	RSVD	RSVD	RSVD
Reset	0x0	0x0	0b0	–	0x0	0x0	0x0	0x0
Access Type			Write, Read	–				

BITFIELD	BITS	DESCRIPTION	DECODE
FSYNC_RST_MODE	5		0x0: Legacy 0x1: Start frame sync state machine regardless of video locks.

TR0 (0x500, 0x560)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN	RX_CRC_EN	RSVD[1:0]		PRIO_VAL[1:0]		PRIO_CFG[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x501, 0x561)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT[1:0]		BW_VAL[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL by 1 0b01: Multiply BW_VAL by 4 0b10: Multiply BW_VAL by 16 0b11: Multiply BW_VAL by 16

BITFIELD	BITS	DESCRIPTION	DECODE
BW_VAL	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL x BW_MULT/ 10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x503, 0x563)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x504, 0x564)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL = 00001001, packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x506, 0x566)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN	RT_CNT_OEN
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_OEN	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR—ARQ2 register) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x507, 0x567)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR	RT_CNT[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR	7	Reached maximum retransmit limit (MAX_RT—ARQ1) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x510)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjusts the priority to be used for requests from this channel	00: Priority from Tx adapter is used 01: Priority from Tx adapter is increased 10: Priority from Tx adapter is decreased 11: Priority in PRIO_VAL register is used

TR1 (0x511)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x513)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x514)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x516)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_B	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_B (0x517)) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_B (0x517) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x517)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B (0x516)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x520)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x521)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x523)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x524)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Received packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x526)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_C	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_C	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C (0x527)) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_C	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x527) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x527)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C (0x526)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x530)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjusts the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x531)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x533)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x534)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x536)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_D	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_D (0x537)) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x537) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x537)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D (0x536)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x570)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_B	RX_CRC_EN_B	RSVD[1:0]		PRIO_VAL_B[1:0]		PRIO_CFG_B[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_B	7	When set, calculates and appends CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_B	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_B	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_B	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x571)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_B[1:0]		BW_VAL_B[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_B	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_B by 1 0b01: Multiply BW_VAL_B by 4 0b10: Multiply BW_VAL_B by 16 0b11: Multiply BW_VAL_B by 16
BW_VAL_B	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_B x BW_MULT_B/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x573)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_B[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_B	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x574)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_B[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_B	7:0	Receives packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_B = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x576)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_B[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_B	RT_CNT_OEN_B
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_B	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_B	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR (0x577)) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_B	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT (0x577) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x577)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_B	RT_CNT_B[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_B	7	Reached maximum retransmit limit (MAX_RT_B (0x576)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_B	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x580)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_C	RX_CRC_EN_C	RSVD[1:0]		PRIO_VAL_C[1:0]		PRIO_CFG_C[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_C	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet
RX_CRC_EN_C	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_C	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_C	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x581)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_C[1:0]		BW_VAL_C[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_C	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_C by 1 0b01: Multiply BW_VAL_C by 4 0b10: Multiply BW_VAL_C by 16 0b11: Multiply BW_VAL_C by 16
BW_VAL_C	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_C x BW_MULT_C/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x583)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_C[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_C	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x584)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_C[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_C	7:0	Receive packets from selected sources Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_C = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x586)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_C[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_C	RT_CNT_OEN_C
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_C	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_C	1	Enable reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR_C—0X587) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_C	0	Enable reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_C (0x587) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x587)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_C	RT_CNT_C[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_C	7	Reached maximum retransmit limit (MAX_RT_C (0x586)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_C	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

TR0 (0x590)

BIT	7	6	5	4	3	2	1	0
Field	TX_CRC_EN_D	RX_CRC_EN_D	RSVD[1:0]		PRIO_VAL_D[1:0]		PRIO_CFG_D[1:0]	
Reset	0b1	0b1	0x3		0x0		0x0	
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TX_CRC_EN_D	7	When set, calculate and append CRC to each packet transmitted from this port	0b0: Do not calculate and append CRC to each packet 0b1: Calculate and append CRC to each packet

BITFIELD	BITS	DESCRIPTION	DECODE
RX_CRC_EN_D	6	When set, indicates that packets received at this port have appended CRC. CRC checking should be performed at each packet.	0b0: Do not perform CRC check at each packet 0b1: Perform CRC check at each packet
PRIO_VAL_D	3:2	Sets the priority for this channel's packet requests	0b00: Low priority 0b01: Normal priority 0b10: High priority 0b11: Urgent priority
PRIO_CFG_D	1:0	Adjust the priority to be used for requests from this channel	0b00: Priority from Tx adapter is used 0b01: Priority from Tx adapter is increased 0b10: Priority from Tx adapter is decreased 0b11: Priority in PRIO_VAL register is used

TR1 (0x591)

BIT	7	6	5	4	3	2	1	0
Field	BW_MULT_D[1:0]		BW_VAL_D[5:0]					
Reset	0x2		0x30					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
BW_MULT_D	7:6	Channel bandwidth-allocation multiplication factor	0b00: Multiply BW_VAL_D by 1 0b01: Multiply BW_VAL_D by 4 0b10: Multiply BW_VAL_D by 16 0b11: Multiply BW_VAL_D by 16
BW_VAL_D	5:0	Channel bandwidth-allocation base. Fair bandwidth use ratio = BW_VAL_D x BW_MULT_D/10 as a percentage of total link bandwidth	0bXXXXXX: Channel base-bandwidth value

TR3 (0x593)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TX_SRC_ID_D[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SRC_ID_D	2:0	Source identifier used in packets transmitted from this port. Default value is set by CFG0 pin.	0bXXX: Source ID for packets from this channel

TR4 (0x594)

BIT	7	6	5	4	3	2	1	0
Field	RX_SRC_SEL_D[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RX_SRC_SEL_D	7:0	Received packets from selected sources. Each bit indicates whether packets with that source ID should be received or not. For example, when RX_SRC_SEL_D = 00001001, then packets with source ID equal to 0 and 3 will be received.	0x00: No packets received 0x01: Packets from source ID 0 received 0x02: Packets from source ID 1 received 0x03: Packets from source ID 0 and 1 received 0x04: Packets from source ID 2 received ... ... 0xFF: Packets from all source IDs received

ARQ1 (0x596)

BIT	7	6	5	4	3	2	1	0
Field	–	MAX_RT_D[2:0]			RSVD	RSVD	MAX_RT_ERR_OEN_D	RT_CNT_OEN_D
Reset	–	0x7			0x0	0x0	0b1	0b0
Access Type	–	Write, Read					Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_D	6:4	Maximum retransmission limit. ARQ will stop retransmission after reaching the limit for a single packet.	
MAX_RT_ERR_OEN_D	1	Enables reporting of ARQ maximum retransmission limit errors (MAX_RT_ERR (0x597)) for this channel at ERRB pin	0b0: Disable reporting of ARQ maximum retransmission limit errors 0b1: Enable reporting of ARQ maximum retransmission limit errors
RT_CNT_OEN_D	0	Enables reporting of ARQ retransmission event for this channel at ERRB pin. When enabled, ERRB is asserted when RT_CNT_D (0x597) of this channel is greater than 0.	0b0: Disable reporting of ARQ retransmission event 0b1: Enable reporting of ARQ retransmission event

ARQ2 (0x597)

BIT	7	6	5	4	3	2	1	0
Field	MAX_RT_ERR_D	RT_CNT_D[6:0]						
Reset	0b0	0x0						
Access Type	Read Clears All	Read Clears All						

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_D	7	Reached maximum retransmit limit (MAX_RT_D (0x596)) for one packet in this channel	0b0: Maximum retransmission limit not reached 0b1: Maximum retransmission limit reached
RT_CNT_D	6:0	Total retransmission count in this channel	0bXXXXXXX: Count of retransmission for this channel

I2C_0 (0x640)

BIT	7	6	5	4	3	2	1	0
Field	–	RSVD	SLV_SH_P0_A[1:0]		–	SLV_TO_P0_A[2:0]		
Reset	–	0x0	0x2		–	0x6		
Access Type	–		Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_A	5:4	Link A GMSL1 and GMSL2 I²C-to-I²C Slave Setup and Hold Time Setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_A	2:0	Link A GMSL1 and GMSL2 I²C-to-I²C Slave Timeout Setting. Internal I²C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I²C Port 0 for GMSL2. This setting applies to all I²C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x641)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_A[2:0]			–	MST_TO_P0_A[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_A	6:4	Link A GMSL1 and GMSL2 I2C-to-I2C Master Bit Rate Setting. Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 0 for GMSL2 Link A. This setting applies to all I2C Ports for GMSL1 Link A. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P0_A	2:0	Link A GMSL1 and GMSL2 I2C-to-I2C Master Timeout Setting. Internal I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x642)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_A	7:1	Link A GMSL1 and GMSL2 I2C Address Translator Source A. When I2C device address matches SRC_A_P0_A, internal I2C master (on remote side) replaces the device address by DST_A_P0_A. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x643)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_A	7:1	Link A GMSL1 and GMSL2 I2C Address Translator Destination A. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_A_P0_A.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_4 (0x644)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_A	7:1	Link A GMSL1 and GMSL2 I2C Address Translator Source B. When I2C device address matches SRC_B_P0_A, internal I2C master (on remote side) replaces the device address by DST_B_P0_A. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_5 (0x645)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_A	7:1	Link A GMSL1 and GMSL2 I2C Address Translator Destination B. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_B_P0_A.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_0 (0x650)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_B[1:0]		–	SLV_TO_P0_B[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_B	5:4	Link B GMSL1 and GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_B	2:0	Link B GMSL1 and GMSL2 I2C-to-I2C Slave Timeout Setting Internal I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x651)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_B[2:0]			–	MST_TO_P0_B[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_B	6:4	Link B GMSL1 and GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 0 for GMSL2 Link B. This setting applies to all I2C Ports for GMSL1 Link B. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P0_B	2:0	Link B GMSL1 and GMSL2 I2C-to-I2C Master Timeout Setting Internal I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x652)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_B	7:1	Link B GMSL1 and GMSL2 I2C Address Translator Source A When I2C device address matches SRC_A_P0_B, internal I2C master (on remote side) replaces the device address by DST_A_P0_B. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x653)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_B	7:1	Link B GMSL1 and GMSL2 I2C Address Translator Destination A. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_A_P0_B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_4 (0x654)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_B	7:1	Link B GMSL1 and GMSL2 I2C Address Translator Source B When I2C device address matches SRC_B_P0_B, internal I2C master (on remote side) replaces the device address by DST_B_P0_B. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_5 (0x655)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_B	7:1	Link B GMSL1 and GMSL2 I2C Address Translator Destination B This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_B_P0_B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_0 (0x660)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_C[1:0]		–	SLV_TO_P0_C[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_C	5:4	Link C GMSL1 and GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold). Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_C	2:0	Link C GMSL1 and GMSL2 I2C-to-I2C Slave Timeout Setting Internal I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x661)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_C[2:0]			–	MST_TO_P0_C[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_C	6:4	Link C GMSL1 and GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 0 for GMSL2 Link C. This setting applies to all I2C Ports for GMSL1 Link C. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P0_C	2:0	Link C GMSL1 AND GMSL2 I2C-to-I2C Master Timeout Setting Internal I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x662)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_C	7:1	Link C GMSL1 and GMSL2 I2C Address Translator Source A When I2C device address matches SRC_A_P0_C, internal I2C master (on remote side) replaces the device address by DST_A_P0_C. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x663)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_C	7:1	Link C GMSL1 and GMSL2 I2C Address Translator Destination A This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_A_P0_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_4 (0x664)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_C	7:1	Link C GMSL1 and GMSL2 I2C Address Translator Source B When I2C device address matches SRC_B_P0_C, internal I2C master (on remote side) replaces the device address by DST_B_P0_C. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_5 (0x665)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_C	7:1	Link C GMSL1 and GMSL2 I2C Address Translator Destination B This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_B_P0_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_0 (0x670)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P0_D[1:0]		–	SLV_TO_P0_D[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P0_D	5:4	Link D GMSL1 and GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P0_D	2:0	Link D GMSL1 and GMSL2 I2C-to-I2C Slave Timeout Setting Internal I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x671)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P0_D[2:0]			–	MST_TO_P0_D[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P0_D	6:4	Link D GMSL1 and GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 0 for GMSL2 Link D. This setting applies to all I2C Ports for GMSL1 Link D. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P0_D	2:0	Link D GMSL1 and GMSL2 I2C-to-I2C Master Timeout Setting Internal I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x672)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P0_D	7:1	Link D GMSL1 and GMSL2 I2C Address Translator Source A. When I2C device address matches SRC_A_P0_D, internal I2C master (on remote side) replaces the device address by DST_A_P0_D. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x673)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P0_D	7:1	Link D GMSL1 and GMSL2 I2C Address Translator Destination A This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_A_P0_D.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_4 (0x674)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P0_D	7:1	Link D GMSL1 and GMSL2 I2C Address Translator Source B When I2C device address matches SRC_B_P0_D, internal I2C master (on remote side) replaces the device address by DST_B_P0_D. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_5 (0x675)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P0_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P0_D	7:1	Link D GMSL1 and GMSL2 I2C address translator destination B. This setting applies only to I2C Port 0 for GMSL2. This setting applies to all I2C Ports for GMSL1. See the description of SRC_B_P0_D.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_0 (0x680)

BIT	7	6	5	4	3	2	1	0
Field	–	I2C_HSM_P1	SLV_SH_P1_A[1:0]		–	SLV_TO_P1_A[2:0]		
Reset	–	0x0	0x2		–	0x6		
Access Type	–	Write, Read	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_HSM_P1	6	I2C High-Speed Mode Enable for Port 1 ALL GMSL2 links. Set this to run I2C at up to 5Mbps on local side and 3.4Mbps on remote side	
SLV_SH_P1_A	5:4	GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 1 for GMSL2 Link A.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_A	2:0	GMSL2 I2C-to-I2C Slave Timeout Setting Internal GMSL2 I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 1 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x681)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_A[2:0]			–	MST_TO_P1_A[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_A	6:4	GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 1 for GMSL2 Link A. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P1_A	2:0	GMSL2 I2C-to-I2C Master Timeout Setting Internal GMSL2 I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 1 for GMSL2 Link A.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x682)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_A	7:1	GMSL2 I2C Address Translator Source A. When I2C device address matches SRC_A_P1_A, internal I2C master (on remote side) replaces the device address by DST_A_P1_A. This setting applies only to I2C Port 1 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x683)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_A	7:1	GMSL2 I2C Address Translator Destination A. This setting applies only to I2C Port 1 for GMSL2 Link A. See the description of SRC_A_P1_A	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x684)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_A	7:1	GMSL2 I2C Address Translator Source B When I2C device address matches SRC_B_P1_A, internal I2C master (on remote side) replaces the device address by DST_B_P1_A. This setting applies only to I2C Port 1 for GMSL2 Link A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x685)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_A[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_A	7:1	GMSL2 I2C Address Translator Destination B. This setting applies only to I2C Port 1 for GMSL2 Link A. See the description of SRC_B_P1_A.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x690)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_B[1:0]		–	SLV_TO_P1_B[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_B	5:4	GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 1 for GMSL2 Link B.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_B	2:0	GMSL2 I2C-to-I2C Slave Timeout Setting Internal GMSL2 I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 1 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x691)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_B[2:0]			–	MST_TO_P1_B[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_B	6:4	GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 1 for GMSL2 Link B. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed

BITFIELD	BITS	DESCRIPTION	DECODE
MST_TO_P1_B	2:0	GMSL2 I2C-to-I2C Master Timeout Setting Internal GMSL2 I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 1 for GMSL2 Link B.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x692)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_B	7:1	GMSL2 I2C Address Translator Source A. When I2C device address matches SRC_A_P1_B, internal I2C master (on remote side) replaces the device address by DST_A_P1_B This setting applies only to I2C Port 1 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x693)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_B	7:1	GMSL2 I2C Address Translator Destination A. This setting applies only to I2C Port 1 for GMSL2 Link B. See the description of SRC_A_P1_B.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x694)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_B	7:1	GMSL2 I2C Address Translator Source B. When I2C device address matches SRC_B_P1_B, internal I2C master (on remote side) replaces the device address by DST_B_P1_B. This setting applies only to I2C Port 1 for GMSL2 Link B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_5 (0x695)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_B[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_B	7:1	GMSL2 I2C Address Translator Destination B. This setting applies only to I2C Port 1 for GMSL2 Link B. See the description of SRC_B_P1_B.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_0 (0x6A0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_C[1:0]		–	SLV_TO_P1_C[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_C	5:4	GMSL2 I2C-to-I2C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I2C slave. Set this according to the I2C speed mode. This setting applies only to I2C Port 1 for GMSL2 Link C.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved
SLV_TO_P1_C	2:0	GMSL2 I2C-to-I2C Slave Timeout Setting Internal GMSL2 I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 1 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6A1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_C[2:0]			–	MST_TO_P1_C[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_C	6:4	GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 1 for GMSL2 Link C. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P1_C	2:0	GMSL2 I2C-to-I2C Master Timeout Setting Internal GMSL2 I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 1 for GMSL2 Link C.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x6A2)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_C	7:1	GMSL2 I2C Address Translator Source A. When I2C device address matches SRC_A_P1_C, internal I2C master (on remote side) replaces the device address by DST_A_P1_C. This setting applies only to I2C Port 1 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_3 (0x6A3)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_C	7:1	GMSL2 I2C Address Translator Destination A. This setting applies only to I2C Port 1 for GMSL2 Link C. See the description of SRC_A_P1_C.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

I2C_4 (0x6A4)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_C	7:1	GMSL2 I²C Address Translator Source B. When I²C device address matches SRC_B_P1_C, internal I²C master (on remote side) replaces the device address by DST_B_P1_C. This setting applies only to I²C Port 1 for GMSL2 Link C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x6A5)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_C[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_C	7:1	GMSL2 I²C Address Translator Destination B. This setting applies only to I²C Port 1 for GMSL2 Link C. See the description of SRC_B_P1_C.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_0 (0x6B0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SLV_SH_P1_D[1:0]		–	SLV_TO_P1_D[2:0]		
Reset	–	–	0x2		–	0x6		
Access Type	–	–	Write, Read		–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_SH_P1_D	5:4	GMSL2 I²C-to-I²C Slave Setup and Hold Time Setting (setup, hold) Configures the interval between SDA and SCL transitions when driven by the internal I²C slave. Set this according to the I²C speed mode. This setting applies only to I²C Port 1 for GMSL2 Link D.	0b00: Fast-mode Plus 0b01: Fast-mode 0b10: Standard-mode 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
SLV_TO_P1_D	2:0	GMSL2 I2C-to-I2C Slave Timeout Setting Internal GMSL2 I2C slave times out after the configured duration if it does not receive any response while waiting for a packet from remote device. This setting applies only to I2C Port 1 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_1 (0x6B1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MST_BT_P1_D[2:0]			–	MST_TO_P1_D[2:0]		
Reset	0x0	0x5			–	0x6		
Access Type		Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
MST_BT_P1_D	6:4	GMSL2 I2C-to-I2C Master Bit Rate Setting Configures the I2C bit rate used by the internal I2C master (in the device on remote side from the external I2C master). This setting applies only to I2C Port 1 for GMSL2 Link D. Set this according to the I2C speed mode: Fast-mode Plus = 101 to 111 Fast-mode = 010 to 101 Standard-mode = 000 to 010	3b000: 9.92Kbps - Set for I2C Standard-mode speed 3b001: 33.2Kbps - Set for I2C Standard-mode speed 3b010: 99.2Kbps - Set for I2C Standard or Fast-mode speed 3b011: 123Kbps - Set for I2C Fast-mode speed 3b100: 203Kbps - Set for I2C Fast-mode speed 3b101: 397Kbps - Set for I2C Fast or Fast-mode Plus speed 3b110: 625Kbps - Set for I2C Fast or Fast-mode Plus speed 3b111: 980Kbps - Set for I2C Fast-mode Plus speed
MST_TO_P1_D	2:0	GMSL2 I2C-to-I2C Master Timeout Setting Internal GMSL2 I2C master times out after the configured duration if it does not receive any response while waiting for a packet from the remote device. This setting applies only to I2C Port 1 for GMSL2 Link D.	0b000: 16µs 0b001: 1ms 0b010: 2ms 0b011: 4ms 0b100: 8ms 0b101: 16ms 0b110: 32ms 0b111: Disabled

I2C_2 (0x6B2)

BIT	7	6	5	4	3	2	1	0
Field	SRC_A_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_A_P1_D	7:1	GMSL2 I2C Address Translator Source A When I2C device address matches SRC_A_P1_D, internal I2C master (on remote side) replaces the device address by DST_A_P1_D. This setting applies only to I2C Port 1 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_3 (0x6B3)

BIT	7	6	5	4	3	2	1	0
Field	DST_A_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_A_P1_D	7:1	GMSL2 I2C Address Translator Destination A This setting applies only to I2C Port 1 for GMSL2 Link D. See the description of SRC_A_P1_D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_4 (0x6B4)

BIT	7	6	5	4	3	2	1	0
Field	SRC_B_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_B_P1_D	7:1	GMSL2 I2C Address Translator Source B When I2C device address matches SRC_B_P1_D, internal I2C master (on remote side) replaces the device address by DST_B_P1_D. This setting applies only to I2C Port 1 for GMSL2 Link D.	0b0000000: Write/read device address is 0x00/0x01 0b0000001: Write/read device address is 0x02/0x03 ... ... 0b1111111: Write/read device address is 0xFE/0xFF

I2C_5 (0x6B5)

BIT	7	6	5	4	3	2	1	0
Field	DST_B_P1_D[6:0]							–
Reset	0x0							–
Access Type	Write, Read							–

BITFIELD	BITS	DESCRIPTION	DECODE
DST_B_P1_D	7:1	GMSL2 I2C Address Translator Destination B This setting applies only to I2C Port 1 for GMSL2 Link D. See the description of SRC_B_P1_D.	0b0000000: Write/read device address is 0x00/ 0x01 0b0000001: Write/read device address is 0x02/ 0x03 ... ... 0b1111111: Write/read device address is 0xFE/ 0xFF

PROFILE_MIPI_SEL (0x6E1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PROFILE_MIPI_SEL[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
PROFILE_MIPI_SEL	5:0	Changing PROFILE_SEL automatically implements the selected profile. Use PROFILE_DISABLE to prevent profiles from being implemented. Disables profiles from executing. For GMSL1 profiles that use YUV, the yuv_8_10_mux_mode# registers are set to 1. To know exactly which registers are written, refer to the MAX96724 User Guide.	0x0: Default - no configuration registers modified if written to 0 0x1: Implement profile 1 0x2: Implement profile 2 ... ... 0x10: Implement profile 16

PROFILE_GMSL_1_0 (0x6EA)

BIT	7	6	5	4	3	2	1	0
Field	–	PROFILE_GMSL_1[2:0]			–	PROFILE_GMSL_0[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
PROFILE_GMSL_1	6:4	

BITFIELD	BITS	DESCRIPTION
PROFILE_GMSL_0	2:0	Register version of the CFG1/MFP6 pin. Configures each GMSL PHY individually. Directly affects the following registers: CXTP_A GMSL2_A RX_RATE_A HIGHIMM_A (TERM_CAL_OFFSET)

PROFILE_GMSL_3_2 (0x6EB)

BIT	7	6	5	4	3	2	1	0
Field	–	PROFILE_GMSL_3[2:0]			–	PROFILE_GMSL_2[2:0]		
Reset	–	0x0			–	0x0		
Access Type	–	Write, Read			–	Write, Read		

BITFIELD	BITS	DESCRIPTION
PROFILE_GMSL_3	6:4	
PROFILE_GMSL_2	2:0	

MIPI_TX_EXT0 (0x800, 0x810, 0x820, 0x830)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0_H[2:0]			MAP_DST_0_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0_H	7:5	Video Pipe Extended VC Source Mapping register 0: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_0, for use in VC extended mode. See MAP_SRC_0 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_0_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 0th mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_0

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0_H	4:2	Video Pipe Extended VC Destination Mapping register 0: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_0, for use in VC extended mode. See MAP_DST_0 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_0_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the 0th mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_0

MIPI_TX_EXT1 (0x801, 0x811, 0x821, 0x831)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1_H[2:0]			MAP_DST_1_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1_H	7:5	Video Pipe Extended VC Source Mapping register 1: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_1, for use in VC extended mode. See MAP_SRC_1 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_1_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 1st mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_1

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1_H	4:2	Video Pipe Extended VC Destination Mapping register 1: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_1, for use in VC extended mode. See MAP_DST_1 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_1_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the first mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_1

MIPI_TX_EXT2 (0x802, 0x812, 0x822, 0x832)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2_H[2:0]			MAP_DST_2_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2_H	7:5	Video Pipe Extended VC Source Mapping register 2: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_2, for use in VC extended mode. See MAP_SRC_2 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_2_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 2nd mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_2

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2_H	4:2	Video Pipe Extended VC Destination Mapping register 2: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_2, for use in VC extended mode. See MAP_DST_2 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_2_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the second mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_2

MIPI_TX_EXT3 (0x803, 0x813, 0x823, 0x833)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3_H[2:0]			MAP_DST_3_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3_H	7:5	Video Pipe Extended VC Source Mapping register 3: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_3, for use in VC extended mode. See MAP_SRC_3 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_3_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the 3rd mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3_H	4:2	Video Pipe Extended VC Destination Mapping register 3: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_3, for use in VC extended mode. See MAP_DST_3 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_3_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the third mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_3

MIPI_TX_EXT4 (0x804, 0x814, 0x824, 0x834)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4_H[2:0]			MAP_DST_4_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4_H	7:5	Video Pipe Extended VC Source Mapping register 4: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_4, for use in VC extended mode. See MAP_SRC_4 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_4_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the fourth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_4

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4_H	4:2	Video Pipe Extended VC Destination Mapping register 4: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_4, for use in VC extended mode. See MAP_DST_4 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_4_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the fourth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_4

MIPI_TX_EXT5 (0x805, 0x815, 0x825, 0x835)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5_H[2:0]			MAP_DST_5_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5_H	7:5	Video Pipe Extended VC Source Mapping register 5: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_5, for use in VC extended mode. See MAP_SRC_5 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_5_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the fifth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_5

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5_H	4:2	Video Pipe Extended VC Destination Mapping register 5: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_5, for use in VC extended mode. See MAP_DST_5 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_5_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the fifth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_5

MIPI_TX_EXT6 (0x806, 0x816, 0x826, 0x836)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6_H[2:0]			MAP_DST_6_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6_H	7:5	Video Pipe Extended VC Source Mapping register 6: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_6, for use in VC extended mode. See MAP_SRC_6 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_6_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the sixth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_6

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6_H	4:2	Video Pipe Extended VC Destination Mapping register 6: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_6, for use in VC extended mode. See MAP_DST_6 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_6_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the sixth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_6

MIPI_TX_EXT7 (0x807, 0x817, 0x827, 0x837)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7_H[2:0]			MAP_DST_7_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7_H	7:5	Video Pipe Extended VC Source Mapping register 7: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_7, for use in VC extended mode. See MAP_SRC_7 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_7_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the seventh mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_7

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7_H	4:2	Video Pipe Extended VC Destination Mapping register 7: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_7, for use in VC extended mode. See MAP_DST_7 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_7_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the seventh mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_7

MIPI_TX_EXT8 (0x808, 0x818, 0x828, 0x838)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8_H[2:0]			MAP_DST_8_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8_H	7:5	Video Pipe Extended VC Source Mapping register 8: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_8, for use in VC extended mode. See MAP_SRC_8 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_8_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the eighth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_8

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8_H	4:2	Video Pipe Extended VC Destination Mapping register 8: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_8, for use in VC extended mode. See MAP_DST_8 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_8_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the eighth mapping pair.	0XXX: MS 3 bits of VC destination mapping for MAP_DST_8

MIPI_TX_EXT9 (0x809, 0x819, 0x829, 0x839)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9_H[2:0]			MAP_DST_9_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9_H	7:5	Video Pipe Extended VC Source Mapping register 9: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_9, for use in VC extended mode. See MAP_SRC_9 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_9_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the ninth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_9

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9_H	4:2	Video Pipe Extended VC Destination Mapping register 9: Most Significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_9, for use in VC extended mode. See MAP_DST_9 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_9_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the ninth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_9

MIPI_TX_EXT10 (0x80A, 0x81A, 0x82A, 0x83A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10_H[2:0]			MAP_DST_10_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10_H	7:5	Video Pipe Extended VC Source Mapping register 10: Most Significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_10, for use in VC extended mode. See MAP_SRC_10 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_10_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the tenth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_10

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10_H	4:2	Video Pipe Extended VC Destination Mapping register 10: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_10, for use in VC extended mode. See MAP_DST_10 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_10_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the tenth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_10

MIPI_TX_EXT11 (0x80B, 0x81B, 0x82B, 0x83B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11_H[2:0]			MAP_DST_11_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11_H	7:5	Video Pipe Extended VC Source Mapping register 11: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_11, for use in VC extended mode. See MAP_SRC_11 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_11_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the eleventh mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_11

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11_H	4:2	Video Pipe Extended VC Destination Mapping register 11: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_11, for use in VC extended mode. See MAP_DST_11 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_11_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the eleventh mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_11

MIPI_TX_EXT12 (0x80C, 0x81C, 0x82C, 0x83C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12_H[2:0]			MAP_DST_12_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12_H	7:5	Video Pipe Extended VC Source Mapping register 12: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_12, for use in VC extended mode. See MAP_SRC_12 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_12_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the twelfth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_12

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12_H	4:2	Video Pipe Extended VC Destination Mapping register 12: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_12, for use in VC extended mode. See MAP_DST_12 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_12_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the twelfth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_12

MIPI_TX_EXT13 (0x80D, 0x81D, 0x82D, 0x83D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13_H[2:0]			MAP_DST_13_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13_H	7:5	Video Pipe Extended VC Source Mapping register 13: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_13, for use in VC extended mode. See MAP_SRC_13 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_13_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the thirteenth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_13

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13_H	4:2	Video Pipe Extended VC Destination Mapping register 13: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_13, for use in VC extended mode. See MAP_DST_13 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_13_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the thirteenth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_13

MIPI_TX_EXT14 (0x80E, 0x81E, 0x82E, 0x83E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14_H[2:0]			MAP_DST_14_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14_H	7:5	Video Pipe Extended VC Source Mapping register 14: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_14, for use in VC extended mode. See MAP_SRC_14 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_14_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the fourteenth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_14

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14_H	4:2	Video Pipe Extended VC Destination Mapping register 14: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_14, for use in VC extended mode. See MAP_DST_14 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_14_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the fourteenth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_14

MIPI_TX_EXT15 (0x80F, 0x81F, 0x82F, 0x83F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15_H[2:0]			MAP_DST_15_H[2:0]			–	–
Reset	0x0			0x0			–	–
Access Type	Write, Read			Write, Read			–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15_H	7:5	Video Pipe Extended VC Source Mapping register 15: Most significant 3 bits of Virtual Channel (VC) Source Mapping register, MAP_SRC_15, for use in VC extended mode. See MAP_SRC_15 register associated with this Video Pipe. Incoming Video streams whose VC and Data Type match this setting are mapped to the VC and Data Type programmed in MAP_DST_15_H. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source part of the fifteenth mapping pair.	0bXXX: MS 3 bits of VC mapping for MAP_SRC_15

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15_H	4:2	Video Pipe Extended VC Destination Mapping register 15: Most significant 3 bits of Virtual Channel (VC) Destination mapping register, MAP_DST_15, for use in VC extended mode. See MAP_DST_15 register associated with this Video Pipe. This setting provides the corresponding destination map associated with the MAP_SRC_15_H register. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination part of the fifteenth mapping pair.	0bXXX: MS 3 bits of VC destination mapping for MAP_DST_15

MIPI_PHY0 (0x8A0)

BIT	7	6	5	4	3	2	1	0
Field	force_csi_out_en	force_clk3_en	force_clk0_en	phy_1x4b_22	phy_1x4a_22	phy_2x4	RSVD	phy_4x2
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
force_csi_out_en	7	Set to force all MIPI clocks running.	0b0: Normal mode 0b1: Force all MIPI clocks running
force_clk3_en	6	Set to force PHY3 MIPI clock running.	0b0: DPHY0 not enabled as clock 0b1: DPHY0 not enabled as clock
force_clk0_en	5	Set to force PHY0 MIPI clock running.	0b0: DPHY0 not enabled as clock 0b1: DPHY0 not enabled as clock
phy_1x4b_22	4	MIPI PHY 1x4b + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY2 and PHY3 combined as 4-lane. PHY0 and PHY1 are 2-lane ports	0b0: 2x4 not selected 0b1: 2x4 selected
phy_1x4a_22	3	MIPI PHY 1x4a + 2x2 mode: MIPI output configured as one 4-lane port and two 2-lane ports. PHY0 and PHY1 combined as 4-lane. PHY2 and PHY3 are 2-lane ports	0b0: 2x4 not selected 0b1: 2x4 selected
phy_2x4	2	MIPI PHY 2x4 mode: MIPI output configured as two ports with four data lanes each. PHY0 and PHY1 combined, and PHY2 and PHY3 combined.	0b0: 2x4 not selected 0b1: 2x4 selected
phy_4x2	0	MIPI PHY 4x2 mode: MIPI output configured as four 2-lane MIPI ports.	0b0: 4x2 configuration not selected 0b1: 4x2 configuration selected

MIPI_PHY1 (0x8A1)

BIT	7	6	5	4	3	2	1	0
Field	t_hs_przero[1:0]		t_hs_prep[1:0]		t_clk_trail[1:0]		t_clk_przero[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_hs_przero	7:6	Typical DPHY data lane HS_prep + HS_zero timing	0b00: 146ns + 24UI 0b01: 160ns + 24UI 0b10: 173ns + 24UI 0b11: 200ns + 24UI
t_hs_prep	5:4	Typical DPHY data lane HS_prepare timing	0b00: 46.7ns + 4UI 0b01: 53.4ns + 4UI 0b10: 60.0ns + 4UI 0b11: 66.7ns + 4UI
t_clk_trail	3:2	Typical DPHY clock HS_trail timing	0b00: 160ns 0b01: 167ns 0b10: 173ns 0b11: 180ns
t_clk_przero	1:0	Typical DPHY clock lane HS_prepare + HS_zero timing	0b00: 306ns 0b01: 600ns 0b10: 900ns 0b11: 1200ns

MIPI_PHY2 (0x8A2)

BIT	7	6	5	4	3	2	1	0
Field	phy_Stdby_n[3:0]				t_lpx[1:0]		t_hs_trail[1:0]	
Reset	0xF				0x1		0x0	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
phy_Stdby_n	7:4	MIPI PHY Enable bit [7]: Enable MIPI PHY3 bit [6]: Enable MIPI PHY2 bit [5]: Enable MIPI PHY1 bit [4]: Enable MIPI PHY0	0bXXX0: Put MIPI PHY0 in standby mode 0bXXX1: Enable MIPI PHY0 0bXX0X: Put MIPI PHY1 in standby mode 0bXX1X: Enable MIPI PHY1 0bX0XX: Put MIPI PHY2 in standby mode 0bX1XX: Enable MIPI PHY2 0b0XXX: Put MIPI PHY3 in standby mode 0b1XXX: Enable MIPI PHY3
t_lpx	3:2	Typical DPHY t_{LPX} timing	0b00: 53.4ns 0b01: 106.7ns 0b10: 160ns 0b11: 213.4ns
t_hs_trail	1:0	Typical DPHY data lane HS_trail timing	0b00: 66.7ns + 8UI 0b01: 80ns + 8UI 0b10: 93.4ns + 8UI 0b11: 106.7ns + 8UI

MIPI_PHY3 (0x8A3)

BIT	7	6	5	4	3	2	1	0
Field	phy1_lane_map[3:0]				phy0_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_lane_map	7:4	MIPI PHY1 lane mapping register: bits [5:4]: Set PHY1 D0 Output mapping bits [7:6]: Set PHY1 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration. See register fields in MIPI_PHY0 (0x8A0). For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to PHY1 for MIPI configurations 4x2 and (1x4b+2x2). For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused. In 4x2 mode, phy#_lane_map register bits [3] and [1] will always read back 1'b0 since hardware will mask them to 1'b0 in this mode.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

BITFIELD	BITS	DESCRIPTION	DECODE
phy0_lane_map	3:0	MIPI PHY0 lane mapping register: bits [1:0]: Set PHY0 D0 Output mapping bits [3:2]: Set PHY0 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration. See register fields in MIPI_PHY0 (0x8A0). For MIPI configurations 4x2 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = RSVD, do not use 2'b11 = RSVD, do not use Note: CSI-2 Controller 0 is mapped to PHY0 for MIPI configurations 4x2 and (1x4b+2x2). For MIPI configurations 2x4 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 1 is mapped to both PHY0 and PHY1 for MIPI configurations 2x4 and (1x4a+2x2). CSI-2 Controller 0 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

MIPI_PHY4 (0x8A4)

BIT	7	6	5	4	3	2	1	0
Field	phy3_lane_map[3:0]				phy2_lane_map[3:0]			
Reset	0xE				0x4			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_lane_map	7:4	MIPI PHY3 lane mapping register: bits [5:4]: Set PHY3 D0 Output mapping bits [7:6]: Set PHY3 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration. See register fields in MIPI_PHY0 (0x8A0). For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = RSVD, do not use 2'b11 = RSVD, do not use Note: CSI-2 Controller 3 is mapped to PHY3 for MIPI configurations 4x2 and (1x4a+2x2). For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3
phy2_lane_map	3:0	MIPI PHY2 lane mapping register: bits [1:0]: Set PHY2 D0 Output mapping bits [3:2]: Set PHY2 D1 Output mapping The settings for these bit fields are dependent upon the settings for the MIPI configuration. See register fields in MIPI_PHY0 (0x8A0). For MIPI configurations 4x2 and (1x4a+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to PHY2 for MIPI configurations 4x2 and (1x4a+2x2). For MIPI configurations 2x4 and (1x4b+2x2), the following mappings apply: 2'b00 = Map PHY Output to data lane D0 2'b01 = Map PHY Output to data lane D1 2'b10 = Map PHY Output to data lane D2 2'b11 = Map PHY Output to data lane D3 Note: CSI-2 Controller 2 is mapped to both PHY2 and PHY3 for MIPI configurations 2x4 and (1x4b+2x2). CSI-2 Controller 3 is unused.	0bXX00: Map D0 to data lane D0 0bXX01: Map D0 to data lane D1 0bXX10: Map D0 to data lane D2 0bXX11: Map D0 to data lane D3 0b00XX: Map D1 to data lane D0 0b01XX: Map D1 to data lane D1 0b10XX: Map D1 to data lane D2 0b11XX: Map D1 to data lane D3

MIPI_PHY5 (0x8A5)

BIT	7	6	5	4	3	2	1	0
Field	t_clk_prep[1:0]		phy1_pol_map[2:0]			phy0_pol_map[2:0]		
Reset	0x0		0x0			0x0		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
t_clk_prep	7:6	Typical DPHY clock lane HS_prepare timing	0b00: 40ns 0b01: 46.7ns 0b10: 53.4ns 0b11: 60ns
phy1_pol_map	5:3	MIPI PHY1 lane polarity register: bit [5]: Set polarity on PHY1 CLK lane bit [4]: Set polarity on PHY1 D1 lane bit [3]: Set polarity on PHY1 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive
phy0_pol_map	2:0	MIPI PHY0 lane polarity register: bit [2]: Set polarity on PHY0 CLK lane bit [1]: Set polarity on PHY0 D1 lane bit [0]: Set polarity on PHY0 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive

MIPI_PHY6 (0x8A6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	phy3_pol_map[2:0]			phy2_pol_map[2:0]		
Reset	–	–	0x0			0x0		
Access Type	–	–	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pol_map	5:3	MIPI PHY3 lane polarity register: bit [5]: Set polarity on PHY3 CLK lane bit [4]: Set polarity on PHY3 D1 lane bit [3]: Set polarity on PHY3 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive
phy2_pol_map	2:0	MIPI PHY0 lane polarity register: bit [2]: Set polarity on PHY2 CLK lane bit [1]: Set polarity on PHY2 D1 lane bit [0]: Set polarity on PHY2 D0 lane 1'b0 = normal polarity, 1'b1 = inversed polarity	0bXX0: D0 normal polarity, P is positive, N is negative 0bXX1: D0 inverse polarity, P is negative, N is positive 0bX0X: D1 normal polarity, P is positive, N is negative 0bX1X: D1 inverse polarity, P is negative, N is positive 0b0XX: CK normal polarity, P is positive, N is negative 0b1XX: CK inverse polarity, P is negative, N is positive

MIPI_PHY8 (0x8A8)

BIT	7	6	5	4	3	2	1	0
Field	t_lpxesc[2:0]			RSVD	RSVD	RSVD	RSVD	RSVD
Reset	0x0			0b0	0b0	0b0		0b0
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
t_lpxesc	7:5	Typical DPHY t_{LPX} timing in escape mode	0b000: 66.67ns 0b001: 80ns 0b010: 100ns 0b011: 133ns 0b100: 200ns 0b101: 400ns 0b110: 1000ns 0b111: 2000ns

MIPI_PHY9 (0x8A9)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp0[4:0]					–	RSVD	RSVD
Reset	0x00					–	0b0	0b0
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp0	7:3	PHY copy 0, replicates data from source PHY to destination PHY (valid source and destinations are PHY 0 and 1 only)	[4:3]: PHY copy 0 source [6:5]: PHY copy 0 destination [7]: PHY copy 0 enable

MIPI_PHY10 (0x8AA)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp1[4:0]					–	RSVD	RSVD
Reset	0x00					–	0b1	0b0
Access Type	Write, Read					–		

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp1	7:3	PHY copy 1, replicates data from source PHY to destination PHY (valid source and destinations are PHY 2 and 3 only)	[4:3]: PHY copy 0 source [6:5]: PHY copy 0 destination [7]: PHY copy 0 enable

MIPI_PHY11 (0x8AB)

BIT	7	6	5	4	3	2	1	0
Field	phy_cp_err[3:0]				–	–	RSVD	–
Reset	0x00				–	–	0b0	–
Access Type	Read Only				–	–		–

BITFIELD	BITS	DESCRIPTION	DECODE
phy_cp_err	7:4		0bXXX1: PHY copy 0 FIFO overflow 0bXX1X: PHY copy 0 FIFO underflow 0bX1XX: PHY copy 1 FIFO overflow 0b1XXX: PHY copy 1 FIFO underflow

MIPI_PHY13 (0x8AD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	t_t3_prebegin[5:0]					
Reset	–	–	0x1F					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_prebegin	5:0	CPHY pre-begin phase of the preamble (t3_prebegin + 1) x 7UI	0b000000: 7UI 0b000001: 14UI 0b111110: 441UI 0B111111: 448UI

MIPI_PHY14 (0x8AE)

BIT	7	6	5	4	3	2	1	0
Field	–	t_t3_post[4:0]					t_t3_prep[1:0]	
Reset	–	0x17					0x1	
Access Type	–	Write, Read					Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
t_t3_post	6:2	CPHY post length after HS data = (t3_post + 1) x 7UI	0bXXXXX: CPHY post length
t_t3_prep	1:0	CPHY Ths_prepare timing	0b00: 40ns 0b01: 55ns 0b10: 66.7ns 0b11: 86.7ns

MIPI_PHY16 (0x8B0)

BIT	7	6	5	4	3	2	1	0
Field	–	TUN_CONV_DATA_CRC_ERR_OEN	TUN_DATA_CRC_ERR_OEN	TUN_ECC_UNCORR_ERR_OEN	TUN_ECC_CORR_ERR_OEN	–	–	–
Reset	–	0x1	0x1	0b1	0b1	–	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_CONV_DATA_CRC_ERR_OEN	6	For tunneling mode, enable reporting at ERRB pin of DPHY/CPHY data CRC errors	0x0: Errorr not forwarded to ERRB pin 0x1: Error reporting forwarded to ERRB pin
TUN_DATA_CRC_ERR_OEN	5	For tunneling mode, enable reporting at ERRB pin of DPHY/CPHY data CRC errors	0x0: Errorr not forwarded to ERRB pin 0x1: Error reporting forwarded to ERRB pin
TUN_ECC_UNCORR_ERR_OEN	4	For tunneling mode, enable reporting at ERRB pin of uncorrectable errors on DPHY ECC or CPHY header CRC	0x0: Errorr not forwarded to ERRB pin 0x1: Error reporting forwarded to ERRB pin
TUN_ECC_CORR_ERR_OEN	3	For tunneling mode, enable reporting at ERRB pin of correctable errors on DPHY ECC or CPHY header CRC	0x0: Errorr not forwarded to ERRB pin 0x1: Error reporting forwarded to ERRB pin

MIPI_PHY17 (0x8B1)

BIT	7	6	5	4	3	2	1	0
Field	–	TUN_CONV_DATA_CRC_ERR	TUN_DATA_CRC_ERR	TUN_ECC_UNCORR_ERR	TUN_ECC_CORR_ERR	–	–	–
Reset	–	0b0	0b0	0b0	0b0	–	–	–
Access Type	–	Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_CONV_DATA_CRC_ERR	6	For tunneling mode, DPHY to CPHY conversion (header) data CRC errors Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.	0x0: no Error Detected 0x1: Error Detected
TUN_DATA_CRC_ERR	5	For tunneling mode, DPHY/CPHY data CRC errors Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.	0x0: no Error Detected 0x1: Error Detected
TUN_ECC_UNCORR_ERR	4	For tunneling mode, uncorrectable errors on DPHY ECC or CPHY header CRC Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.	0x0: no Error Detected 0x1: Error Detected
TUN_ECC_CORR_ERR	3	For tunneling mode, correctable errors on DPHY ECC or CPHY header CRC. Combined for all MIPI PHYs. Read individual MIPI_TX STATUS registers to clear.	0x0: no Error Detected 0x1: Error Detected

MIPI_PHY18 (0x8B2)

BIT	7	6	5	4	3	2	1	0
Field	csipll3_PLLORangeH	csipll3_PLLORangeL	csipll2_PLLORangeH	csipll2_PLLORangeL	csipll1_PLLORangeH	csipll1_PLLORangeL	csipll0_PLLORangeH	csipll0_PLLORangeL
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
csipll3_PLLORangeH	7	Live status bit that indicates csipll3 is above range.	0x0: within range 0x1: indicates csipll is above range
csipll3_PLLORangeL	6	Live status bit that indicates csipll3 is below range.	0x0: within range 0x1: indicates csipll is below range.
csipll2_PLLORangeH	5	Live status bit that indicates csipll2 is above range.	0x0: within range 0x1: indicates csipll is above range
csipll2_PLLORangeL	4	Live status bit that indicates csipll2 is below range.	0x0: within range 0x1: indicates csipll is below range.
csipll1_PLLORangeH	3	Live status bit that indicates csipll1 is above range.	0x0: within range 0x1: indicates csipll is above range
csipll1_PLLORangeL	2	Live status bit that indicates csipll1 is below range.	0x0: within range 0x1: indicates csipll is below range.
csipll0_PLLORangeH	1	Live status bit that indicates csipll0 is above range.	0x0: within range 0x1: indicates csipll is above range
csipll0_PLLORangeL	0	Live status bit that indicates csipll0 is below range.	0x0: within range 0x1: indicates csipll is below range.

MIPI_PHY19 (0x8B3)

BIT	7	6	5	4	3	2	1	0
Field	csipll3_PLLORangeH_flag	csipll3_PLLORangeL_flag	csipll2_PLLORangeH_flag	csipll2_PLLORangeL_flag	csipll1_PLLORangeH_flag	csipll1_PLLORangeL_flag	csipll0_PLLORangeH_flag	csipll0_PLLORangeL_flag
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
csipll3_PLLORangeH_flag	7	Sticky flag that indicates csipll3 was above range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was above range. Read clears.
csipll3_PLLORangeL_flag	6	Sticky flag that indicates csipll3 was below range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was below range. Read clears.
csipll2_PLLORangeH_flag	5	Sticky flag that indicates csipll2 was above range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was above range. Read clears.
csipll2_PLLORangeL_flag	4	Sticky flag that indicates csipll2 was below range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was below range. Read clears.
csipll1_PLLORangeH_flag	3	Sticky flag that indicates csipll1 was above range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was above range. Read clears.
csipll1_PLLORangeL_flag	2	Sticky flag that indicates csipll1 was below range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was below range. Read clears.
csipll0_PLLORangeH_flag	1	Sticky flag that indicates csipll0 was above range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was above range. Read clears.
csipll0_PLLORangeL_flag	0	Sticky flag that indicates csipll0 was below range at some point since last cleared (or since device was reset). Read clears the flag.	0x0: within range 0x1: Sticky flag that indicates csipll was below range. Read clears.

MIPI_PHY20 (0x8B4)

BIT	7	6	5	4	3	2	1	0
Field	csipll3_PLLORangeH_oen	csipll3_PLLORangeL_oen	csipll2_PLLORangeH_oen	csipll2_PLLORangeL_oen	csipll1_PLLORangeH_oen	csipll1_PLLORangeL_oen	csipll0_PLLORangeH_oen	csipll0_PLLORangeL_oen
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
csipll3_PLLORangeH_oen	7	This register controls whether csipll3_PLLORangeH_flag contributes to the setting of ERROR.	0x0: csipll3_PLLORangeH_flag does NOT contribute to ERROR condition 0x1: csipll3_PLLORangeH_flag is ORed with other flags to set ERROR condition

BITFIELD	BITS	DESCRIPTION	DECODE
csipll3_PLLORangeL_oen	6	This register controls whether csipll3_PLLORangeL_flag contributes to the setting of ERROR.	0x0: csipll3_PLLORangeL_flag does NOT contribute to ERROR condition 0x1: csipll3_PLLORangeL_flag is ORed with other flags to set ERROR condition
csipll2_PLLORangeH_oen	5	This register controls whether csipll2_PLLORangeH_flag contributes to the setting of ERROR.	0x0: csipll2_PLLORangeH_flag does NOT contribute to ERROR condition 0x1: csipll2_PLLORangeH_flag is ORed with other flags to set ERROR condition
csipll2_PLLORangeL_oen	4	This register controls whether csipll2_PLLORangeL_flag contributes to the setting of ERROR.	0x0: csipll2_PLLORangeL_flag does NOT contribute to ERROR condition 0x1: csipll2_PLLORangeL_flag is ORed with other flags to set ERROR condition
csipll1_PLLORangeH_oen	3	This register controls whether csipll1_PLLORangeH_flag contributes to the setting of ERROR.	0x0: csipll1_PLLORangeH_flag does NOT contribute to ERROR condition 0x1: csipll1_PLLORangeH_flag is ORed with other flags to set ERROR condition
csipll1_PLLORangeL_oen	2	This register controls whether csipll1_PLLORangeL_flag contributes to the setting of ERROR.	0x0: csipll1_PLLORangeL_flag does NOT contribute to ERROR condition 0x1: csipll1_PLLORangeL_flag is ORed with other flags to set ERROR condition
csipll0_PLLORangeH_oen	1	This register controls whether csipll0_PLLORangeL_flag contributes to the setting of ERROR.	0x0: csipll0_PLLORangeH_flag does NOT contribute to ERROR condition 0x1: csipll0_PLLORangeH_flag is ORed with other flags to set ERROR condition
csipll0_PLLORangeL_oen	0	This register controls whether csipll0_PLLORangeL_flag contributes to the setting of ERROR.	0x0: csipll0_PLLORangeL_flag does NOT contribute to ERROR condition 0x1: csipll0_PLLORangeL_flag is ORed with other flags to set ERROR condition

MIPI_PRBS_0 (0x8C0)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_PRBS_EN_P1_LN1[1:0]		MIPI_PRBS_EN_P1_LN0[1:0]		MIPI_PRBS_EN_P0_LN1[1:0]		MIPI_PRBS_EN_P0_LN0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P1_LN1	7:6	PRBS enable for PHY1 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P1_LN0	5:4	PRBS enable for PHY1 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P0_LN1	3:2	PRBS enable for PHY0 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P0_LN0	1:0	PRBS enable for PHY0 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

MIPI_PRBS_1 (0x8C1)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_PRBS_EN_P3_LN1[1:0]		MIPI_PRBS_EN_P3_LN0[1:0]		MIPI_PRBS_EN_P2_LN1[1:0]		MIPI_PRBS_EN_P2_LN0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_PRBS_EN_P3_LN1	7:6	PRBS enable for PHY3 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P3_LN0	5:4	PRBS enable for PHY3 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN1	3:2	PRBS enable for PHY2 lane 1 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled
MIPI_PRBS_EN_P2_LN0	1:0	PRBS enable for PHY2 lane 0 eye diagram. Set CPHY enable for CPHY symbols.	0b00: Disabled 0b01: PRBS 9 enabled 0b10: PRBS 11 enabled 0b11: PRBS 18 enabled

MIPI_PRBS_2 (0x8C2)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CUST_SEED_EN_P3_LN1	MIPI_CUST_SEED_EN_P3_LN0	MIPI_CUST_SEED_EN_P2_LN1	MIPI_CUST_SEED_EN_P2_LN0	MIPI_CUST_SEED_EN_P1_LN1	MIPI_CUST_SEED_EN_P1_LN0	MIPI_CUST_SEED_EN_P0_LN1	MIPI_CUST_SEED_EN_P0_LN0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUST_SEED_EN_P3_LN1	7	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P3_LN0	6	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P2_LN1	5	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUST_SEED_EN_P2_LN0	4	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P1_LN1	3	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P1_LN0	2	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P0_LN1	1	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled
MIPI_CUST_SEED_EN_P0_LN0	0	Use custom seed for reset value of PRBS generator.	0b0: Disabled 0b1: Enabled

MIPI_PRBS_3 (0x8C3)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	–	–	MIPI_CUSTOM_SEED_2[1:0]	
Reset	0b1	0b1	0b1	0b1	–	–	0x2	
Access Type					–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_2	1:0	Custom seed [17:16] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [17:16]: Reset value for PRBS if enabled by MIPI custom seed enable register

MIPI_PRBS_4 (0x8C4)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CUSTOM_SEED_1[7:0]							
Reset	0x78							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_1	7:0	Custom seed [15:8] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [15:8]: Reset value for PRBS if enabled by MIPI custom seed enable register

MIPI_PRBS_5 (0x8C5)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CUSTOM_SEED_0[7:0]							
Reset	0x9a							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CUSTOM_SEED_0	7:0	Custom seed [7:0] for MIPI PRBS eye diagrams. Reset value for PRBS if enabled by MIPI custom seed enable register. Default reset is from CPHY spec.	Bits [7:0]: Reset value for PRBS if enabled by MIPI custom seed enable register

MIPI_PHY21 (0x8C6)

BIT	7	6	5	4	3	2	1	0
Field	Force_Video_Mask[3:0]				Auto_Mask_En[3:0]			
Reset	0x0				0xF			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Force_Video_Mask	7:4	Forces video output to be masked (send all 0's) in 4WxH or Wx4H synchronous aggregation modes. Masking impacts video streams from video pipes 0-3.	0bXXX1: Force video from Video Pipe 0 to be masked. 0bXX1X: Force video from Video Pipe 1 to be masked. 0bX1XX: Force video from Video Pipe 2 to be masked. 0b1XXX: Force video from Video Pipe 3 to be masked.
Auto_Mask_En	3:0	Auto Video Mask Enable Automatically insert 0s into synchronized aggregated video outputs if a Video Pipe 0-3 video lock is lost. This allows the other video streams to continue being transmitted on the MIPI interface.	0bXXX1: Auto video mask enabled for Video Pipe 0 0bXX1X: Auto video mask enabled for Video Pipe 1 0bX1XX: Auto video mask enabled for Video Pipe 2 0b1XXX: Auto video mask enabled for Video Pipe 3

MIPI_PHY22 (0x8C7)

BIT	7	6	5	4	3	2	1	0
Field	Video_Mask_Latch_Reset	–	–	–	Video_Mask_Restart_En[3:0]			
Reset	0b0	–	–	–	0xF			
Access Type	Write Clears All, Read	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Video_Mask_Latch_Reset	7	Reset all Video_Mask_Latched latches. Write 1 to activate reset, bit self clears and automatically releases reset.	0x0: No action 0x1: Reset latches

BITFIELD	BITS	DESCRIPTION	DECODE
Video_Mask_Restart_En	3:0	Automatically restarts video streams that were previously masked off due to loss of video lock	0bXXX1: Restart video from Video Pipe 0 0bXX1X: Restart video from Video Pipe 1 0bX1XX: Restart video from Video Pipe 2 0b1XXX: Restart video from Video Pipe 3

MIPI_PHY24 (0x8C9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	RST_MIPITX_LOC[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
RST_MIPITX_LOC	3:0	Active high reset to MIPI controllers. Disabled by asserting DP_RST_MIPI. Bit 0: Controller 0 reset Bit 1: Controller 1 reset Bit 2: Controller 2 reset Bit 3: Controller 3 reset	0bxxx0: Controller 0 reset not asserted 0bxxx1: Controller 0 reset asserted 0bxx0x: Controller 1 reset not asserted 0bxx1x: Controller 1 reset asserted 0bx0xx: Controller 2 reset not asserted 0bx1xx: Controller 2 reset asserted 0b0xxx: Controller 3 reset not asserted 0b1xxx: Controller 3 reset asserted

MIPI_CTRL_SEL (0x8CA)

BIT	7	6	5	4	3	2	1	0
Field	MIPI_CTRL_SEL_3[1:0]		MIPI_CTRL_SEL_2[1:0]		MIPI_CTRL_SEL_1[1:0]		MIPI_CTRL_SEL_0[1:0]	
Reset	0x3		0x2		0x1		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CTRL_SEL_3	7:6	Selects target MIPI Controller for video pipe 3 This can be used in place of the FCFS MAP_SRC and MAP_DST registers to re-map everything. Using this register will map everything by default, then the user can re-map specific data types to other controllers as before.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset
MIPI_CTRL_SEL_2	5:4	Selects target MIPI Controller for video pipe 2 This can be used in place of the FCFS MAP_SRC and MAP_DST registers to re-map everything. Using this register will map everything by default, then the user can re-map specific data types to other controllers as before.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset
MIPI_CTRL_SEL_1	3:2	Selects target MIPI Controller for video pipe 1 This can be used in place of the FCFS MAP_SRC and MAP_DST registers to re-map everything. Using this register will map everything by default, then the user can re-map specific data types to other controllers as before.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset

BITFIELD	BITS	DESCRIPTION	DECODE
MIPI_CTRL_SEL_0	1:0	Selects target MIPI Controller for video pipe 0 This can be used in place of the FCFS MAP_SRC and MAP_DST registers to re-map everything. Using this register will map everything by default, then the user can re-map specific data types to other controllers as before. Note: The MIPI CRTL reset logic from RESET_LINK uses the mapping registers. If only MIPI_CTRL_SEL is used for mapping, then the reset logic may not work as expected because it does not know which controller to reset. In other words, RESET_LINK_0 will reset CTRL0 and RESET_LINK_1 will reset CTRL_1, unless only the mapping registers are used.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset

MIPI_PHY25 (0x8D0)

BIT	7	6	5	4	3	2	1	0
Field	csi2_tx1_pkt_cnt[3:0]				csi2_tx0_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
csi2_tx1_pkt_cnt	7:4	Packet count of CSI2 Controller 1
csi2_tx0_pkt_cnt	3:0	Packet count of CSI2 Controller 0

MIPI_PHY26 (0x8D1)

BIT	7	6	5	4	3	2	1	0
Field	csi2_tx3_pkt_cnt[3:0]				csi2_tx2_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
csi2_tx3_pkt_cnt	7:4	Packet count of CSI2 Controller 3	0bXXXX: Toggling bits indicate MIPI data is active on controller 3
csi2_tx2_pkt_cnt	3:0	Packet count of CSI2 Controller 2	0bXXXX: Toggling bits indicate MIPI data is active on controller 2

MIPI_PHY27 (0x8D2)

BIT	7	6	5	4	3	2	1	0
Field	phy1_pkt_cnt[3:0]				phy0_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy1_pkt_cnt	7:4	Packet count of MIPI PHY1	0bXXXX: Toggling bits indicate MIPI data is active on PHY 1
phy0_pkt_cnt	3:0	Packet count of MIPI PHY0	0bXXXX: Toggling bits indicate MIPI data is active on PHY 0

MIPI_PHY28 (0x8D3)

BIT	7	6	5	4	3	2	1	0
Field	phy3_pkt_cnt[3:0]				phy2_pkt_cnt[3:0]			
Reset	0x00				0x00			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
phy3_pkt_cnt	7:4	Packet count of MIPI PHY3	0bXXXX: Toggling bits indicate MIPI data is active on PHY 3
phy2_pkt_cnt	3:0	Packet count of MIPI PHY2	0bXXXX: Toggling bits indicate MIPI data is active on PHY 2

MIPI_PHY_CP_ERR_OE (0x8D4)

BIT	7	6	5	4	3	2	1	0
Field	PHY_CP1_UF_ERR_OEN	PHY_CP1_OV_ERR_OEN	PHY_CP0_UF_ERR_OEN	PHY_CP0_OV_ERR_OEN	–	–	–	–
Reset	0b1	0b1	0b1	0b1	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PHY_CP1_UF_ERR_OEN	7	Enable Reflection of phy_cp_err[3] onto the ERRB pin. This corresponds to the PHY copy 1 FIFO underflow error. See the phy_cp_err register field bit 3. (bit 7 of register byte)	0x0: Mask error from ERRB pin 0x1: Enable error onto ERRB pin
PHY_CP1_OV_ERR_OEN	6	Enable Reflection of phy_cp_err[2] onto the ERRB pin. This corresponds to the PHY copy 1 FIFO overflow error. See the phy_cp_err register field bit 2. (bit 6 of register byte)	0x0: Mask error from ERRB pin 0x1: Enable error onto ERRB pin
PHY_CP0_UF_ERR_OEN	5	Enable Reflection of phy_cp_err[1] onto the ERRB pin. This corresponds to the PHY copy 0 FIFO underflow error. See the phy_cp_err register field bit 1. (bit 5 of register byte)	0x0: Mask error from ERRB pin 0x1: Enable error onto ERRB pin
PHY_CP0_OV_ERR_OEN	4	Enable Reflection of phy_cp_err[0] onto the ERRB pin. This corresponds to the PHY copy 0 FIFO overflow error. See the phy_cp_err register field bit 0. (bit 4 of register byte)	0x0: Mask error from ERRB pin 0x1: Enable error onto ERRB pin

MIPI_PHY_FLAGS (0x8D5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DESKEW_START_OVERLAP_FLAG_3	DESKEW_START_OVERLAP_FLAG_2	DESKEW_START_OVERLAP_FLAG_1	DESKEW_START_OVERLAP_FLAG_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_START_OVERLAP_FLAG_3	3	Error flag that indicates that the MIPI controller tried to start outputing data while initial deskew was still running. Either speed up the MIPI output so the deskew finishes sooner or increase n_vs_block.	0x0: No error 0x1: Initial deskew and tx_start overlapped.
DESKEW_START_OVERLAP_FLAG_2	2	Error flag that indicates that the MIPI controller tried to start outputing data while initial deskew was still running. Either speed up the MIPI output so the deskew finishes sooner or increase n_vs_block.	0x0: No error 0x1: Initial deskew and tx_start overlapped.
DESKEW_START_OVERLAP_FLAG_1	1	Error flag that indicates that the MIPI controller tried to start outputing data while initial deskew was still running. Either speed up the MIPI output so the deskew finishes sooner or increase n_vs_block.	0x0: No error 0x1: Initial deskew and tx_start overlapped.
DESKEW_START_OVERLAP_FLAG_0	0	Error flag that indicates that the MIPI controller tried to start outputing data while initial deskew was still running. Either speed up the MIPI output so the deskew finishes sooner or increase n_vs_block.	0x0: No error 0x1: Initial deskew and tx_start overlapped.

MIPI_PHY_OEN (0x8D6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DESKEW_START_OVERLAP_OEN_3	DESKEW_START_OVERLAP_OEN_2	DESKEW_START_OVERLAP_OEN_1	DESKEW_START_OVERLAP_OEN_0
Reset	–	–	–	–	0b1	0b1	0b1	0b1
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_START_OVERLAP_OEN_3	3	Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.	0x0: Does not affect ERRB pin. 0x1: Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.
DESKEW_START_OVERLAP_OEN_2	2	Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.	0x0: Does not affect ERRB pin. 0x1: Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.
DESKEW_START_OVERLAP_OEN_1	1	Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.	0x0: Does not affect ERRB pin. 0x1: Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.
DESKEW_START_OVERLAP_OEN_0	0	Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.	0x0: Does not affect ERRB pin. 0x1: Enable DESKEW_START_OVERLAP_ERR_FLAG to go to ERRB pin.

MIPI_ERR_PKT_0 (0x8D8)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_EN_0	–	ERR_PKT_DT_0[5:0]					
Reset	0b0	–	0x3E					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_EN_0	7	Enable output of special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 0. 0 = Disabled 1 = Enabled	0x0: Disabled 0x1: Enabled
ERR_PKT_DT_0	5:0	Specifies the MIPI Data Type for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN control. See the ERR_PKT_EN register field.	0x0 0x1: Datatype value

MIPI_ERR_PKT_1 (0x8D9)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_EN_1	–	ERR_PKT_DT_1[5:0]					
Reset	0b0	–	0x3E					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_EN_1	7	Enable output of special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 1. 0 = Disabled 1 = Enabled	0x0: Disabled 0x1: Enabled
ERR_PKT_DT_1	5:0	Specifies the MIPI Data Type for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN control. See the ERR_PKT_EN register field.	0x0 0x1: Datatype value

MIPI_ERR_PKT_2 (0x8DA)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_EN_2	–	ERR_PKT_DT_2[5:0]					
Reset	0b0	–	0x3E					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_EN_2	7	Enable output of special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 2. 0 = Disabled 1 = Enabled	0x0: Disabled 0x1: Enabled
ERR_PKT_DT_2	5:0	Specifies the MIPI Data Type for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN control. See the ERR_PKT_EN register field.	0x0 0x1: Datatype value

MIPI_ERR_PKT_3 (0x8DB)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_EN_3	–	ERR_PKT_DT_3[5:0]					
Reset	0b0	–	0x3E					
Access Type	Write, Read	–	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_EN_3	7	Enable output of special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 3. 0 = Disabled 1 = Enabled	0x0: Disabled 0x1: Enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_DT_3	5:0	Specifies the MIPI Data Type for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN control. See the ERR_PKT_EN register field.	0x0 0x1: Datatype value

MIPI_ERR_PKT_4 (0x8DC)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_VC_OVRD_EN_0	–	–	ERR_PKT_VC_OVRD_0[4:0]				
Reset	0b0	–	–	0x0F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_OVRD_EN_0	7	Enable virtual channel override value for special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 0.	0x0: Use VC of random video stream in current controller 0x1: Use VC specified in ERR_PKT_VC_OVRD_0 register
ERR_PKT_VC_OVRD_0	4:0	Specifies the MIPI Virtual Channel for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN_0 and ERR_PKT_VC_OVRD_EN_0. See the ERR_PKT_EN_0 register field.	0x0: 0x0 0x1: 0x1 0x2: 0x2 0x3: 0x3 0x4: 0x0 0x5: 0x1 0x6: 0x2 0x7: 0x3 0x8: 0x0 0x9: 0x1 0xA: 0x2 0xB: 0x3 0xC: 0x0 0xD: 0x1 0xE: 0x2 0xF: 0x3 0x10: 0x0 0x11: 0x1 0x12: 0x2 0x13: 0x3 0x14: 0x0 0x15: 0x1 0x16: 0x2 0x17: 0x3 0x18: 0x0 0x19: 0x1 0x1A: 0x2 0x1B: 0x3 0x1C: 0x0 0x1D: 0x1 0x1E: 0x2 0x1F: 0x3

MIPI_ERR_PKT_5 (0x8DD)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_VC_OVRD_EN_1	–	–	ERR_PKT_VC_OVRD_1[4:0]				
Reset	0b0	–	–	0x0F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_OVRD_EN_1	7	Enable virtual channel override value for special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 1.	0x0: Use VC of random video stream in current controller 0x1: Use VC specified in ERR_PKT_VC_OVRD_1 register
ERR_PKT_VC_OVRD_1	4:0	Specifies the MIPI Virtual Channel for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN_1 and ERR_PKT_VC_OVRD_EN_1. See the ERR_PKT_EN_1 register field.	0x0: 0x0 0x1: 0x1 0x2: 0x2 0x3: 0x3 0x4: 0x0 0x5: 0x1 0x6: 0x2 0x7: 0x3 0x8: 0x0 0x9: 0x1 0xA: 0x2 0xB: 0x3 0xC: 0x0 0xD: 0x1 0xE: 0x2 0xF: 0x3 0x10: 0x0 0x11: 0x1 0x12: 0x2 0x13: 0x3 0x14: 0x0 0x15: 0x1 0x16: 0x2 0x17: 0x3 0x18: 0x0 0x19: 0x1 0x1A: 0x2 0x1B: 0x3 0x1C: 0x0 0x1D: 0x1 0x1E: 0x2 0x1F: 0x3

MIPI_ERR_PKT_6 (0x8DE)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_VC_OVRD_EN_2	–	–	ERR_PKT_VC_OVRD_2[4:0]				
Reset	0b0	–	–	0x0F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_OVRD_EN_2	7	Enable virtual channel override value for special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 2.	0x0: Use VC of random video stream in current controller 0x1: Use VC specified in ERR_PKT_VC_OVRD_2 register
ERR_PKT_VC_OVRD_2	4:0	Specifies the MIPI Virtual Channel for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN_2 and ERR_PKT_VC_OVRD_EN_2. See the ERR_PKT_EN_2 register field.	0x0: 0x0 0x1: 0x1 0x2: 0x2 0x3: 0x3 0x4: 0x0 0x5: 0x1 0x6: 0x2 0x7: 0x3 0x8: 0x0 0x9: 0x1 0xA: 0x2 0xB: 0x3 0xC: 0x0 0xD: 0x1 0xE: 0x2 0xF: 0x3 0x10: 0x0 0x11: 0x1 0x12: 0x2 0x13: 0x3 0x14: 0x0 0x15: 0x1 0x16: 0x2 0x17: 0x3 0x18: 0x0 0x19: 0x1 0x1A: 0x2 0x1B: 0x3 0x1C: 0x0 0x1D: 0x1 0x1E: 0x2 0x1F: 0x3

MIPI_ERR_PKT_7 (0x8E0)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_VC_OVRD_EN_3	–	–	ERR_PKT_VC_OVRD_3[4:0]				
Reset	0b0	–	–	0x0F				
Access Type	Write, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_OVRD_EN_3	7	Enable virtual channel override value for special MIPI Error Packet when uncorrectable header errors occur in Tunnel Mode for MIPI controller 3.	0x0: Use VC of random video stream in current controller 0x1: Use VC specified in ERR_PKT_VC_OVRD_3 register
ERR_PKT_VC_OVRD_3	4:0	Specifies the MIPI Virtual Channel for the special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. Must be enabled using the ERR_PKT_EN_3 and ERR_PKT_VC_OVRD_EN_3. See the ERR_PKT_EN_3 register field.	0x0: 0x0 0x1: 0x1 0x2: 0x2 0x3: 0x3 0x4: 0x0 0x5: 0x1 0x6: 0x2 0x7: 0x3 0x8: 0x0 0x9: 0x1 0xA: 0x2 0xB: 0x3 0xC: 0x0 0xD: 0x1 0xE: 0x2 0xF: 0x3 0x10: 0x0 0x11: 0x1 0x12: 0x2 0x13: 0x3 0x14: 0x0 0x15: 0x1 0x16: 0x2 0x17: 0x3 0x18: 0x0 0x19: 0x1 0x1A: 0x2 0x1B: 0x3 0x1C: 0x0 0x1D: 0x1 0x1E: 0x2 0x1F: 0x3

MIPI_ERR_PKT_8 (0x8E1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERR_PKT_VC_0[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_0	4:0	Reads back the MIPI Virtual Channel value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Virtual Channel value

MIPI_ERR_PKT_9 (0x8E2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERR_PKT_VC_1[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_1	4:0	Reads back the MIPI Virtual Channel value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Virtual Channel value

MIPI_ERR_PKT_10 (0x8E3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERR_PKT_VC_2[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_2	4:0	Reads back the MIPI Virtual Channel value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Virtual Channel value

MIPI_ERR_PKT_11 (0x8E4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ERR_PKT_VC_3[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_VC_3	4:0	Reads back the MIPI Virtual Channel value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Virtual Channel value

MIPI_ERR_PKT_12 (0x8E5)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_OVRD_EN_3	ERR_PKT_WC_OVRD_EN_2	ERR_PKT_WC_OVRD_EN_1	ERR_PKT_WC_OVRD_EN_0	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_OVRD_EN_3	7	0 = Pick random word count from video source in MIPI controller 3 as the word count for MIPI Error Packets 1 = Use word count specified in ERR_PKT_WC_3_H/L register as the word count for MIPI Error Packets	0x0: 0 = Pick random word count from video source in MIPI controller 3 as the word count for MIPI Error Packets 0x1: 1 = Use word count specified in ERR_PKT_WC_3_H/L register as the word count for MIPI Error Packets
ERR_PKT_WC_OVRD_EN_2	6	0 = Pick random word count from video source in MIPI controller 2 as the word count for MIPI Error Packets 1 = Use word count specified in ERR_PKT_WC_2_H/L register as the word count for MIPI Error Packets	0x0: 0 = Pick random word count from video source in MIPI controller 2 as the word count for MIPI Error Packets 0x1: 1 = Use word count specified in ERR_PKT_WC_2_H/L register as the word count for MIPI Error Packets
ERR_PKT_WC_OVRD_EN_1	5	0 = Pick random word count from video source in MIPI controller 1 as the word count for MIPI Error Packets 1 = Use word count specified in ERR_PKT_WC_1_H/L register as the word count for MIPI Error Packets	0x0: 0 = Pick random word count from video source in MIPI controller 1 as the word count for MIPI Error Packets 0x1: 1 = Use word count specified in ERR_PKT_WC_1_H/L register as the word count for MIPI Error Packets
ERR_PKT_WC_OVRD_EN_0	4	0 = Pick random word count from video source in MIPI controller 0 as the word count for MIPI Error Packets 1 = Use word count specified in ERR_PKT_WC_0_H/L register as the word count for MIPI Error Packets	0x0: 0 = Pick random word count from video source in MIPI controller 0 as the word count for MIPI Error Packets 0x1: 1 = Use word count specified in ERR_PKT_WC_0_H/L register as the word count for MIPI Error Packets

MIPI_ERR_PKT_13 (0x8E6)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_0_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_0_H	7:0	If ERR_PKT_WC_OVRD_EN_0 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_14 (0x8E7)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_0_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_0_L	7:0	If ERR_PKT_WC_OVRD_EN_0 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_15 (0x8E8)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_1_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_1_H	7:0	If ERR_PKT_WC_OVRD_EN_1 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_16 (0x8E9)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_1_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_1_L	7:0	If ERR_PKT_WC_OVRD_EN_1 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_17 (0x8EA)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_2_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_2_H	7:0	If ERR_PKT_WC_OVRD_EN_2 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_18 (0x8EB)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_2_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_2_L	7:0	If ERR_PKT_WC_OVRD_EN_2 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_19 (0x8EC)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_3_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_3_H	7:0	If ERR_PKT_WC_OVRD_EN_3 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_ERR_PKT_20 (0x8ED)

BIT	7	6	5	4	3	2	1	0
Field	ERR_PKT_WC_3_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ERR_PKT_WC_3_L	7:0	If ERR_PKT_WC_OVRD_EN_3 is set, this register sets the word count for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode. When not in WC override mode, this register reads back the word count value for special MIPI Error Packet which is output when uncorrectable header errors occur in Tunnel Mode.	0x0 0x1: Word Count value. See register description

MIPI_TX1 (0x901, 0x941)

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI Tx mode: b0 = 1: Enables MIPI VS short packet counter, cyclic 1~16.	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MIPI_TX2 (0x902, 0x942)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx Status Register The register is split into decode segments: bit[0] SYNC mode enable. bit[1] Video sync flag bit[2] Loss of video sync flag bit[3] Tunneling mode: DPHY ECC or CPHY header CRC error (correctable) bit[4] Tunneling mode: DPHY ECC or CPHY header CRC error (uncorrectable) bit[5] Tunneling mode: DPHY/CPHY data CRC error bit[6] Tunneling mode: DPHY to CPHY conversion data protection CRC error	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0xXXXXX0XX: No loss of video sync 0xXXXXX1XX: Video sync lost after last read of this register or reset.

MIPI_TX3 (0x903, 0x943)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x87							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY Deskew Initial Calibration Control The register is split into six decode segments: Bit [7]: Selects auto-initial deskew calibration on or off Bit [6]: Reserved Bit [5]: Any bit change initiates an initial calibration if bit 4 = 1 Bit [4]: Selects manual initial on or off Bit [3]: Reserved Bits [2:0]: Selects initial deskew width	0bXXXXX000: Initial deskew width = 1 x 32k UI 0bXXXXX001: Initial deskew width = 2 x 32k UI 0bXXXXX010: Initial deskew width = 3 x 32k UI 0bXXXXX011: Initial deskew width = 4 x 32k UI 0bXXXXX100: Initial deskew width = 5 x 32k UI 0bXXXXX101: Initial deskew width = 6 x 32k UI 0bXXXXX110: Initial deskew width = 7 x 32k UI 0bXXXXX111: Initial deskew width = 8 x 32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on (should be used only in DPHY mode and PLL greater than or equal to 1.5G)

MIPI_TX4 (0x904, 0x944)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x81							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY Periodic Deskew Calibration Control The register is split into four decode segments: bit [7]: Selects periodic deskew calibration on or off bit [6]: Selects generation on rising or falling edge of VS bits [5:3]: Selects periodic interval bits [2:0]: Selects periodic deskew width	0bXXXXX000: Periodic deskew width = 1k UI 0bXXXXX001: Periodic deskew width = 2k UI 0bXXXXX010: Periodic deskew width = 3k UI 0bXXXXX011: Periodic deskew width = 4k UI 0bXXXXX100: Periodic deskew width = 5k UI 0bXXXXX101: Periodic deskew width = 6k UI 0bXXXXX110: Periodic deskew width = 7k UI 0bXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodic deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x905, 0x945)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of clock cycles to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX6 (0x906, 0x946)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_POST[7:0]							
Reset	0x19							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_POST	7:0	Number of byte clocks to hold clock active after data	0xXX: Number of MIPI byte clocks

MIPI_TX7 (0x907, 0x947)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TX_GAP[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TX_GAP	7:0	Sets the number of clocks to wait after the HS CLK has entered LP before enabling it again for the next transmission	0xXX: Number of MIPI byte clocks

MIPI_TX8 (0x908, 0x948)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_L	7:0	Sets DPHY timing parameter t_{WAKEUP}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX9 (0x909, 0x949)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_M[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_M	7:0	Sets DPHY timing parameter t_{WAKEUP}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX10 (0x90A, 0x94A)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
Reset	0x3		0b0	0x1	–	0x0		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	MIPI Lane Count In 4x2 mode, CSI2_LANE_CNT register bit [1] will always read back 1'b0 since hardware will mask this to 1'b0 in this mode.	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes (Reserved for registers 0x90A and 0x9CA) 0b11: Four data lanes (Reserved for registers 0x90A and 0x9CA)
CSI2_CPHY_EN	5	CPHY Enable	0b0: DPHY mode 0b1: CPHY mode
csi2_vcx_en	4	Enables virtual channel extension	0b0: Select 2-bit VC 0b1: Select 5-bit VC (CPHY) or 4-bit VC (DPHY)
CSI2_TWAKEUP_H	2:0	High bits of DPHY timing parameter t_{WAKEUP}. Sets the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0bXXX: Number of MIPI byte clocks

MIPI_TX11 (0x90B, 0x94B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b00000000: No mapping enabled 0bXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXX1X: Map SRC_1 to DES_1 0bXXXXX1XX: Map SRC_2 to DES_2 0bXXXX1XXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7

MIPI_TX12 (0x90C, 0x94C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b0000000: No mapping enabled 0bXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXX1X: Map SRC_9 to DES_9 0bXXXXX1XX: Map SRC_10 to DES_10 0bXXXX1XXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15

MIPI_TX13 (0x90D, 0x94D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Video Pipe Source Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. See register MAP_DST_0 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX14 (0x90E, 0x94E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Video Pipe Destination Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. See register MAP_SRC_0 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX15 (0x90F, 0x94F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Video Pipe Source Mapping Register 1 - Virtual Channel/Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the first mapping pair. See register MAP_DST_1 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX16 (0x910, 0x950)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Video Pipe Destination Mapping Register 1 - Virtual Channel/Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the first mapping pair. See register MAP_SRC_1 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX17 (0x911, 0x951)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Video Pipe Source Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the second mapping pair. See register MAP_DST_2 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX18 (0x912, 0x952)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Video Pipe Destination Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the second mapping pair. See register MAP_SRC_2 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX19 (0x913, 0x953)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Video Pipe Source Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the third mapping pair. See register MAP_DST_3 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX20 (0x914, 0x954)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Video Pipe Destination Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the third mapping pair. See register MAP_SRC_3 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX21 (0x915, 0x955)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Video Pipe Source Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fourth mapping pair. See register MAP_DST_4 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX22 (0x916, 0x956)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Video Pipe Destination Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fourth mapping pair. See register MAP_SRC_4 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX23 (0x917, 0x957)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Video Pipe Source Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fifth mapping pair. See register MAP_DST_5 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX24 (0x918, 0x958)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Video Pipe Destination Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fifth mapping pair. See register MAP_SRC_5 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX25 (0x919, 0x959)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Video Pipe Source Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. his register is the source setting of the sixth mapping pair. See register MAP_DST_6 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX26 (0x91A, 0x95A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Video Pipe Destination Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the sixth mapping pair. See register MAP_SRC_6 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX27 (0x91B, 0x95B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Video Pipe Source Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the seventh mapping pair. See register MAP_DST_7 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX28 (0x91C, 0x95C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Video Pipe Destination Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the seventh mapping pair. See register MAP_SRC_7 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX29 (0x91D, 0x95D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Video Pipe Source Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the eighth mapping pair. See register MAP_DST_8 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX30 (0x91E, 0x95E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Video Pipe Destination Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the eighth mapping pair. See register MAP_SRC_8 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX31 (0x91F, 0x95F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Video Pipe Source Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the ninth mapping pair. See register MAP_DST_9 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX32 (0x920, 0x960)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Video Pipe Destination Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the ninth mapping pair. See register MAP_SRC_9 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX33 (0x921, 0x961)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Video Pipe Source Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the tenth mapping pair. See register MAP_DST_10 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX34 (0x922, 0x962)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Video Pipe Destination Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the tenth mapping pair. See register MAP_SRC_10 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX35 (0x923, 0x963)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Video Pipe Source Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the eleventh mapping pair. See register MAP_DST_11 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX36 (0x924, 0x964)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Video Pipe Destination Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the eleventh mapping pair. See register MAP_SRC_11 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX37 (0x925, 0x965)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Video Pipe Source Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the twelfth mapping pair. See register MAP_DST_12 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX38 (0x926, 0x966)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Video Pipe Destination Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the twelfth mapping pair. See register MAP_SRC_12 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX39 (0x927, 0x967)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Video Pipe Source Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the thirteenth mapping pair. See register MAP_DST_13 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX40 (0x928, 0x968)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Video Pipe Destination Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the thirteenth mapping pair. See register MAP_SRC_13 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX41 (0x929, 0x969)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Video Pipe Source Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fourteenth mapping pair. See register MAP_DST_14 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX42 (0x92A, 0x96A)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Video Pipe Destination Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fourteenth mapping pair. See register MAP_SRC_14 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX43 (0x92B, 0x96B)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Video Pipe Source Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fifteenth mapping pair. See register MAP_DST_15 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX44 (0x92C, 0x96C)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Video Pipe Destination Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: bits [7:6]: VC - Virtual channel bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fifteenth mapping pair. See register MAP_SRC_15 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX45 (0x92D, 0x96D)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_3 and MAP_DST_3 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_2	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_2 and MAP_DST_2 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_1	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_1 and MAP_DST_1 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_0	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_0 and MAP_DST_0 mapping registers.	0b00: Map to controller 0 0b01: Map to controller 1 0b10: Map to controller 2 0b11: Map to controller 3

MIPI_TX46 (0x92E, 0x96E)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_7 and MAP_DST_7 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_6	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_6 and MAP_DST_6 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_5 and MAP_DST_5 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_4 and MAP_DST_4 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX47 (0x92F, 0x96F)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_11 and MAP_DST_11 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_10 and MAP_DST_10 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_9	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_9 and MAP_DST_9 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_8	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_8 and MAP_DST_8 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX48 (0x930, 0x970)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_15 and MAP_DST_15 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_14 and MAP_DST_14 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_13 and MAP_DST_13 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_12 and MAP_DST_12 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX49 (0x931, 0x971)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	MIPI controller SYNC concatenation register. The register is split into four decode segments: bit [7]: 1'b1 = 4WxH, 1'b0 = Wx4H bit [6]: Reserved bits [5:4]: Select the first line to concatenate. All others follow in order bits [3:0]. 2'b00 = Select Pipe 0 to be the master 2'b01 = Select Pipe 1 to be the master 2'b10 = Select Pipe 2 to be the master 2'b11 = Select Pipe 3 to be the master bit [3]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 3 bit [2]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 2 bit [1]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 1 bit [0]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 0	0bXXXXXXX1: Concatenate Video Pipeline 0 0bXXXXXX1X: Concatenate Video Pipeline 1 0bXXXXX1XX: Concatenate Video Pipeline 2 0bXXXX1XXX: Concatenate Video Pipeline 3 0bXX00XXXX: Select Video Pipeline 0 as master 0bXX01XXXX: Select Video Pipeline 1 as master 0bXX10XXXX: Select Video Pipeline 2 as master 0bXX11XXXX: Select Video Pipeline 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX50 (0x932, 0x972)

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: bit [7]: Select periodic deskew calibration for one or all virtual channels bits [6:5]: Reserved bits [4:0]: Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7	0b0xxxxxxx: Generate periodic calibration deskew calibration on all virtual channels 0b1xx00000: Periodic deskew calibration generated by virtual Channel 0 0b1xx00001: Periodic deskew calibration generated by virtual Channel 1 0b1xx00010: Periodic deskew calibration generated by virtual Channel 2 0b1xx00011: Periodic deskew calibration generated by virtual Channel 3 0b1xx00100: Periodic deskew calibration generated by virtual Channel 4 0b1xx00101: Periodic deskew calibration generated by virtual Channel 5 0b1xx00110: Periodic deskew calibration generated by virtual Channel 6 0b1xx00111: Periodic deskew calibration generated by virtual Channel 7 0b1xx01000: Periodic deskew calibration generated by virtual Channel 8 0b1xx01001: Periodic deskew calibration generated by virtual Channel 9 0b1xx01010: Periodic deskew calibration generated by virtual Channel 10 0b1xx01011: Periodic deskew calibration generated by virtual Channel 11 0b1xx01100: Periodic deskew calibration generated by virtual Channel 12 0b1xx01101: Periodic deskew calibration generated by virtual Channel 13 0b1xx01110: Periodic deskew calibration generated by virtual Channel 14 0b1xx01111: Periodic deskew calibration generated by virtual Channel 15

MIPI_TX51 (0x933, 0x973)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory read mapping enable for 8-bit DT when sharing the same video pipe with RAW16	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
MODE_DT	3	Select 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

MIPI_TX52 (0x934, 0x974)

BIT	7	6	5	4	3	2	1	0
Field	video_masked_latched[3:0]				video_masked[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
video_masked_latched	7:4	Indicates video pipes 0-3 were masked off at one point while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off
video_masked	3:0	Video pipe currently masked off while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off

MIPI_TX54 (0x936, 0x976)

BIT	7	6	5	4	3	2	1	0
Field	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
Reset	0x0	0x0		0x1		0x0		0x0
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_CORR	7	Do not enable header error correction in tunneling mode	0x0: Automatic correction for correctable header error 0x1: Turn off correction for correctable header error
DESKEW_TUN	6:5	Deskew Mode for CSI2 Tunneling	0: Periodic deskew as in HS94 (determined by deskew_per_* registers). 1: Periodic deskew follows SER. 2: Periodic deskew START follows SER but width as register defined. 3: Not used

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_SER_LANE_NUM	4:3	Tunneling Serializer Lane Number Used ONLY in tunneling mode when source is in CPHY mode	0x0: 1-lane 0x1: 2-lanes
DESKEW_TUN_SRC	2:1	Tunneling Deskew Source Select DESKEW_TUN_SRC register must select one of the mapped pipes for this controller.	0x0: Pipe 0 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3
TUN_EN	0	Tunneling Enabled This register takes effect only if DIS_AUTO_TUN_DET is 1.	0b0: Tunneling disabled 0b1: Tunneling enabled

MIPI_TX56 (0x938, 0x978)

BIT	7	6	5	4	3	2	1	0
Field	PKT_START_ADDR[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PKT_START_ADDR	7:0	Specifies the start address of the long packet. 0: The long packet is sent out when the whole line is filled in line memory. Not 0: The long packet begins when PKT_START_ADDR x 128 bytes are filled in the line memory in tunnel mode or when PKT_START_ADDR x 64 pixels are filled in the line memory in pixel mode. Make sure register n_vs_block is 2 or more (default = 1). Notes: • "Cut-through" only works with 1-3 virtual channels. May increase to 4 VCs in future revisions. • Bytes are packed differently into memory when in tunnel mode. For example, in tunnel mode, a BPP of 24 is equal to 1.33 pixels per address. In pixel mode, a BPP of 24 is equal to 1 pixel per address. • When in tunnel mode, the units for PKT_START_ADDR are in bytes. In pixel mode, the units are in pixels.

MIPI_TX57 (0x939, 0x979)

BIT	7	6	5	4	3	2	1	0
Field	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	RSVD
Reset	0x0	0x0	0x1		–	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_AUTO_SER_LANE_DET	7	Disable auto SER lane count detect. When this register is set to 1 (automatic detection of SER lane count is disabled), TUN_SER_LANE_NUM register will need to be set to the SER lane count.	0b0: Tunneling disabled 0b1: Tunneling enabled
DIS_AUTO_TUN_DET	6	Disable auto tunneling mode detect. When this register is set to 1 (automatic detection of tunneling mode disabled), TUN_EN registers will set pixel mode (TUN_EN = 0) or tunneling mode (TUN_EN =1).	0b0: Tunneling disabled 0b1: Tunneling enabled
TUN_DEST	5:4	Tunneling controller Destination	0x0: Controller 0 0x1: Controller 1
TUN_DPHY_TO_CPHY_CONV	2	Only used when TUN_DPHY_TO_CPHY_CONV_OVRD bit is set. Manual override bit to enable DPHY to CPHY conversion in tunneling mode (must also disable auto tunneling mode detect DIS_AUTO_TUN_DET = 1 and manually set tunneling mode TUN_EN = 1). When set to 0, SER headers are evaluated to detect DPHY/CPHY mode, if SER is sending DPHY and the DES MIPI PHY is sent to CPHY mode, conversion is turn on.	0x0: Controller 0 0x1: Controller 1
TUN_DPHY_TO_CPHY_CONV_OVRD	1	Enable value in TUN_DPHY_TO_CPHY_CONV register to override automatic detection.	0x0: Controller 0 0x1: Controller 1

MIPI_ERR_INJ_B1 (0x93A, 0x97A)

BIT	7	6	5	4	3	2	1	0
Field	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
Reset	0b0	–	–	0x00				
Access Type	Write Clears All, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DCPHY_CONV_ERR_INJ_B1_EN	7	Enable Error Injection for the first bit error injection location selection. See the DCPHY_CONV_ERR_INJ_B1_SITE register field description. Write 1 to trigger the error injection. This bit will self clear.	
DCPHY_CONV_ERR_INJ_B1_SITE	4:0	First Bit Error Injection location in the DPHY header. Used to inject errors into the MIPI DPHY standard output header which is then converted to MIPI CPHY standard output during tunnel mode.	0-7: DATA ID (DT) 8-23: DATA FIELD 24-30: ECC 31-32: VCX

MIPI_ERR_INJ_B2 (0x93B, 0x97B)

BIT	7	6	5	4	3	2	1	0
Field	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
Reset	0b0	–	–	0x00				
Access Type	Write Clears All, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DCPHY_CONV_ERR_INJ_B2_EN	7	Enable Error Injection for the second bit error injection location selection. See the DCPHY_CONV_ERR_INJ_B2_SITE register field description. Write 1 to trigger the error injection. This bit will self clear.	
DCPHY_CONV_ERR_INJ_B2_SITE	4:0	Second Bit Error Injection location in the DPHY header. Used to inject errors into the MIPI DPHY standard output header which is then converted to MIPI CPHY standard output during tunnel mode.	0-7: DATA ID (DT) 8-23: DATA FIELD 24-30: ECC 31-32: VCX

MIPI_ERRB_DESKEW_ORDER (0x93C, 0x97C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
Reset	–	–	–	–	0x0	0x0	0x0	–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_BEFORE_ERRB_PKT_MODE	3	This bit can control when the DESKEW occurs relative to ERRB_PKT. This register, DESKEW_BEFORE_ERRB_PKT_MODE, has priority over DESKEW_AFTER_ERRB_PKT_MODE Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW may occur before or after ERRB_PKT depending on other registers (see complete table) 0x1: DESKEW occurs before ERRB_PKT
DESKEW_AFTER_ERRB_PKT_MODE	2	This bit can control when the DESKEW occurs relative to ERRB_PKT. Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW may occur before or after ERRB_PKT depending on other registers (see complete table) 0x1: DESKEW occurs after ERRB_PKT
DESKEW_BEFORE_VS_PKT_MODE	1	This bit can control when the DESKEW occurs relative to a VS (frame-start or frame-end) pkt. Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW occurs after the VS pkt 0x1: DESKEW occurs before the VS pkt

MIPI_TX1 (0x981, 0x9C1)

BIT	7	6	5	4	3	2	1	0
Field	MODE[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	7:0	MIPI Tx mode: b0 = 1: Enables MIPI VS short packet counter, cyclic 1~16.	0bXXXXXXX0: Disable MIPI VS short packet counter 0bXXXXXXX1: Enable MIPI VS short packet counter

MIPI_TX2 (0x982, 0x9C2)

BIT	7	6	5	4	3	2	1	0
Field	STATUS[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
STATUS	7:0	MIPI Tx Status Register The register is split into decode segments: Bit[0] SYNC mode enable. Bit[1] Video sync flag Bit[2] Loss of video sync flag Bit[3] Tunneling mode: DPHY ECC or CPHY header CRC error (correctable) Bit[4] Tunneling mode: DPHY ECC or CPHY header CRC error (uncorrectable) Bit[5] Tunneling mode: DPHY/CPHY data CRC error Bit[6] Tunneling mode: DPHY to CPHY conversion data protection CRC error	0bXXXXXXX0: SYNC mode disabled 0bXXXXXXX1: SYNC mode enabled 0bXXXXXX0X: Video channels not in-sync 0bXXXXXX1X: Video channels in-sync 0xXXXXX0XX: No loss of video sync 0xXXXXX1XX: Video sync lost after last read of this register or reset.

MIPI_TX3 (0x983, 0x9C3)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_INIT[7:0]							
Reset	0x87							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_INIT	7:0	DPHY Deskew Initial Calibration Control The register is split into six decode segments: Bit [7]: Selects auto-initial deskew calibration on or off Bit [6]: Reserved Bit [5]: Any bit change initiates an initial calibration if bit 4 = 1 Bit [4]: Selects manual initial on or off Bit [3]: Reserved Bits [2:0]: Selects initial deskew width	0bXXXXX000: Initial deskew width = 1 x 32k UI 0bXXXXX001: Initial deskew width = 2 x 32k UI 0bXXXXX010: Initial deskew width = 3 x 32k UI 0bXXXXX011: Initial deskew width = 4 x 32k UI 0bXXXXX100: Initial deskew width = 5 x 32k UI 0bXXXXX101: Initial deskew width = 6 x 32k UI 0bXXXXX110: Initial deskew width = 7 x 32k UI 0bXXXXX111: Initial deskew width = 8 x 32k UI 0bXXXX0XXX: Reserved 0bXXXX1XXX: Reserved 0bXXX0XXXX: Manual initial off 0bXXX1XXXX: Manual initial on 0bXX0XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bXX1XXXXX: If bit 4 = 1, triggers one time immediate initial skew calibration 0bX0XXXXXX: Reserved 0bX1XXXXXX: Reserved 0b0XXXXXXX: Auto initial deskew off 0b1XXXXXXX: Auto initial deskew on (should be used only in DPHY mode and PLL greater than or equal to 1.5G)

MIPI_TX4 (0x984, 0x9C4)

BIT	7	6	5	4	3	2	1	0
Field	DESKEW_PER[7:0]							
Reset	0x81							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_PER	7:0	DPHY Periodic Deskew Calibration Control The register is split into four decode segments: Bit [7]: Selects periodic deskew calibration on or off Bit [6]: Selects generation on rising or falling edge of VS Bits [5:3]: Selects periodic interval Bits [2:0]: Selects periodic deskew width	0bXXXXX000: Periodic deskew width = 1k UI 0bXXXXX001: Periodic deskew width = 2k UI 0bXXXXX010: Periodic deskew width = 3k UI 0bXXXXX011: Periodic deskew width = 4k UI 0bXXXXX100: Periodic deskew width = 5k UI 0bXXXXX101: Periodic deskew width = 6k UI 0bXXXXX110: Periodic deskew width = 7k UI 0bXXXXX111: Periodic deskew width = 8k UI 0bXX000XXX: Periodic deskew calibration generated every frame 0bXX001XXX: Periodic deskew calibration generated every 2 frames 0bXX010XXX: Periodic deskew calibration generated every 4 frames 0bXX011XXX: Periodic deskew calibration generated every 8 frames 0bXX100XXX: Periodic deskew calibration generated every 16 frames 0bXX101XXX: Periodic deskew calibration generated every 32 frames 0bXX110XXX: Periodic deskew calibration generated every 64 frames 0bXX111XXX: Periodic deskew calibration generated every 128 frames 0bX0XXXXXX: Periodic deskew calibration generated at rising edge of VS 0bX1XXXXXX: Periodic deskew calibration generated at falling edge of VS 0b0XXXXXXX: Periodic deskew calibration off 0b1XXXXXXX: Periodic deskew calibration on

MIPI_TX5 (0x985, 0x9C5)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_PRE[7:0]							
Reset	0x71							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_PRE	7:0	Number of clock cycles to wait before enabling HS data	0xXX: Number of MIPI byte clocks

MIPI_TX6 (0x986, 0x9C6)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_T_POST[7:0]							
Reset	0x19							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_T_POST	7:0	Number of byte clocks to hold clock active after data	0xXX: Number of MIPI byte clocks

MIPI_TX7 (0x987, 0x9C7)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TX_GAP[7:0]							
Reset	0x1C							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TX_GAP	7:0	Sets the number of clocks to wait after the HS CLK has entered LP before enabling it again for the next transmission	0xXX: Number of MIPI byte clocks

MIPI_TX8 (0x988, 0x9C8)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_L	7:0	Sets DPHY timing parameter T_{wakeup}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX9 (0x989, 0x9C9)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_TWAKEUP_M[7:0]							
Reset	0x01							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_TWAKEUP_M	7:0	Sets DPHY timing parameter T_{wakeup}. Set the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0xXX: Number of MIPI byte clocks

MIPI_TX10 (0x98A, 0x9CA)

BIT	7	6	5	4	3	2	1	0
Field	CSI2_LANE_CNT[1:0]		CSI2_CPHY_EN	csi2_vcx_en	–	CSI2_TWAKEUP_H[2:0]		
Reset	0x3		0b0	0x1	–	0x0		
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CSI2_LANE_CNT	7:6	MIPI Lane Count	0b00: One data lane 0b01: Two data lanes 0b10: Three data lanes (Reserved for registers 0x90A and 0x9CA) 0b11: Four data lanes (Reserved for registers 0x90A and 0x9CA)
CSI2_CPHY_EN	5	CPHY Enable	0b0: DPHY mode 0b1: CPHY mode
csi2_vcx_en	4	Enables virtual channel extension	0b0: Select 2-bit VC 0b1: Select 5-bit VC (CPHY) or 4-bit VC (DPHY)
CSI2_TWAKEUP_H	2:0	High bits of DPHY timing parameter T_{wakeup}. Sets the number of clock cycles to keep clock and data in Mark-1 state after exiting ULPS.	0bXXX: Number of MIPI byte clocks

MIPI_TX11 (0x98B, 0x9CB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_L	7:0	Mapping enable low byte [7:0]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b00000000: No mapping enabled 0bXXXXXXX1: Map SRC_0 to DES_0 0bXXXXXX1X: Map SRC_1 to DES_1 0bXXXXX1XX: Map SRC_2 to DES_2 0bXXXX1XXX: Map SRC_3 to DES_3 0bXXX1XXXX: Map SRC_4 to DES_4 0bXX1XXXXX: Map SRC_5 to DES_5 0bX1XXXXXX: Map SRC_6 to DES_6 0b1XXXXXXX: Map SRC_7 to DES_7

MIPI_TX12 (0x98C, 0x9CC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_EN_H[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_EN_H	7:0	Mapping enable high byte [15:8]. Each bit enables 1 of 8 mapping and distribution entries (defined in MAP_SRC_x, MAP_DST_x, and MAP_DPHY_DST_x) for the current video stream. Non-matched virtual channel (VC) and data types (DT) pass to the corresponding CSI2 controller.	0b0000000: No mapping enabled 0bXXXXXXX1: Map SRC_8 to DES_8 0bXXXXXX1X: Map SRC_9 to DES_9 0bXXXXX1XX: Map SRC_10 to DES_10 0bXXXX1XXX: Map SRC_11 to DES_11 0bXXX1XXXX: Map SRC_12 to DES_12 0bXX1XXXXX: Map SRC_13 to DES_13 0bX1XXXXXX: Map SRC_14 to DES_14 0b1XXXXXXX: Map SRC_15 to DES_15

MIPI_TX13 (0x98D, 0x9CD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_0	7:0	Video Pipe Source Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. See register MAP_DST_0 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX14 (0x98E, 0x9CE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_0	7:0	Video Pipe Destination Mapping Register 0 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_0_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. See register MAP_SRC_0 to program the source setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX15 (0x98F, 0x9CF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_1	7:0	Video Pipe Source Mapping Register 1 - Virtual Channel/Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the first mapping pair. See register MAP_DST_1 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX16 (0x990, 0x9D0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_1	7:0	Video Pipe Destination Mapping Register 1 - Virtual Channel/Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_1_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the first mapping pair. See register MAP_SRC_1 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX17 (0x991, 0x9D1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_2	7:0	Video Pipe Source Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the second mapping pair. See register MAP_DST_2 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX18 (0x992, 0x9D2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_2	7:0	Video Pipe Destination Mapping Register 2 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_2_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the second mapping pair. See register MAP_SRC_2 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX19 (0x993, 0x9D3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_3	7:0	Video Pipe Source Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the third mapping pair. See register MAP_DST_3 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX20 (0x994, 0x9D4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_3	7:0	Video Pipe Destination Mapping Register 3 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_3_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the third mapping pair. See register MAP_SRC_3 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX21 (0x995, 0x9D5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_4	7:0	Video Pipe Source Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fourth mapping pair. See register MAP_DST_4 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX22 (0x996, 0x9D6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_4[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_4	7:0	Video Pipe Destination Mapping Register 4 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_4_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fourth mapping pair. See register MAP_SRC_4 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX23 (0x997, 0x9D7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_5	7:0	Video Pipe Source Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fifth mapping pair. See register MAP_DST_5 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX24 (0x998, 0x9D8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_5[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_5	7:0	Video Pipe Destination Mapping Register 5 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_5_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fifth mapping pair. See register MAP_SRC_5 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX25 (0x999, 0x9D9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_6	7:0	Video Pipe Source Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the sixth mapping pair. See register MAP_DST_6 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX26 (0x99A, 0x9DA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_6[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_6	7:0	Video Pipe Destination Mapping Register 6 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_6_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the sixth mapping pair. See register MAP_SRC_6 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX27 (0x99B, 0x9DB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_7	7:0	Video Pipe Source Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the seventh mapping pair. See register MAP_DST_7 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX28 (0x99C, 0x9DC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_7[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_7	7:0	Video Pipe Destination Mapping Register 7 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_7_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the seventh mapping pair. See register MAP_SRC_7 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX29 (0x99D, 0x9DD)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_8	7:0	Video Pipe Source Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the eighth mapping pair. See register MAP_DST_8 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX30 (0x99E, 0x9DE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_8[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_8	7:0	Video Pipe Destination Mapping Register 8 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_8_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the eighth mapping pair. See register MAP_SRC_8 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX31 (0x99F, 0x9DF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_9	7:0	Video Pipe Source Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the ninth mapping pair. See register MAP_DST_9 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX32 (0x9A0, 0x9E0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_9[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_9	7:0	Video Pipe Destination Mapping Register 9 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_9_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the ninth mapping pair. See register MAP_SRC_9 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX33 (0x9A1, 0x9E1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_10	7:0	Video Pipe Source Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the tenth mapping pair. See register MAP_DST_10 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX34 (0x9A2, 0x9E2)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_10[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_10	7:0	Video Pipe Destination Mapping Register 10 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_10_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the tenth mapping pair. See register MAP_SRC_10 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX35 (0x9A3, 0x9E3)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_11	7:0	Video Pipe Source Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the eleventh mapping pair. See register MAP_DST_11 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX36 (0x9A4, 0x9E4)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_11[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_11	7:0	Video Pipe Destination Mapping Register 11 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_11_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the eleventh mapping pair. See register MAP_SRC_11 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX37 (0x9A5, 0x9E5)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_12	7:0	Video Pipe Source Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the twelfth mapping pair. See register MAP_DST_12 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX38 (0x9A6, 0x9E6)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_12[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_12	7:0	Video Pipe Destination Mapping Register 12 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_12_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the twelfth mapping pair. See register MAP_SRC_12 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX39 (0x9A7, 0x9E7)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_13	7:0	Video Pipe Source Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the thirteenth mapping pair. See register MAP_DST_13 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX40 (0x9A8, 0x9E8)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_13[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_13	7:0	Video Pipe Destination Mapping Register 13 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_13_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the thirteenth mapping pair. See register MAP_SRC_13 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX41 (0x9A9, 0x9E9)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_14	7:0	Video Pipe Source Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fourteenth mapping pair. See register MAP_DST_14 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX42 (0x9AA, 0x9EA)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_14[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_14	7:0	Video Pipe Destination Mapping Register 14 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_14_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fourteenth mapping pair. See register MAP_SRC_14 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX43 (0x9AB, 0x9EB)

BIT	7	6	5	4	3	2	1	0
Field	MAP_SRC_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_SRC_15	7:0	Video Pipe Source Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_SRC_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the source setting of the fifteenth mapping pair. See register MAP_DST_15 to program the destination setting.	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX44 (0x9AC, 0x9EC)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DST_15[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DST_15	7:0	Video Pipe Destination Mapping Register 15 - Virtual Channel / Data Type The register is split into two decode segments: Bits [7:6]: VC - Virtual channel Bits [5:0]: DT - Data type In addition, the VC field can be extended using VC extended mode. See register MAP_DST_15_H associated with this Video Pipe. The Data Type field decode matches that in the MIPI specification. Note: Each Video Pipe has 16 distinct source-to-destination mappings. This register is the destination setting of the fifteenth mapping pair. See register MAP_SRC_15 to program the source setting	[7:6]: VC – 0bXX [5:0]: DT– 0bXXXXXX

MIPI_TX45 (0x9AD, 0x9ED)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_3[1:0]		MAP_DPHY_DEST_2[1:0]		MAP_DPHY_DEST_1[1:0]		MAP_DPHY_DEST_0[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_3	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_3 and MAP_DST_3 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_2	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_2 and MAP_DST_2 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_1	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_1 and MAP_DST_1 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_0	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_0 and MAP_DST_0 mapping registers.	0b00: Map to controller 0 0b01: Map to controller 1 0b10: Map to controller 2 0b11: Map to controller 3

MIPI_TX46 (0x9AE, 0x9EE)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_7[1:0]		MAP_DPHY_DEST_6[1:0]		MAP_DPHY_DEST_5[1:0]		MAP_DPHY_DEST_4[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_7	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_7 and MAP_DST_7 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_6	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_6 and MAP_DST_6 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_5	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_5 and MAP_DST_5 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_4	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_4 and MAP_DST_4 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX47 (0x9AF, 0x9EF)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_11[1:0]		MAP_DPHY_DEST_10[1:0]		MAP_DPHY_DEST_9[1:0]		MAP_DPHY_DEST_8[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_11	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_11 and MAP_DST_11 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_10	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_10 and MAP_DST_10 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_9	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_9 and MAP_DST_9 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_8	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_8 and MAP_DST_8 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX48 (0x9B0, 0x9F0)

BIT	7	6	5	4	3	2	1	0
Field	MAP_DPHY_DEST_15[1:0]		MAP_DPHY_DEST_14[1:0]		MAP_DPHY_DEST_13[1:0]		MAP_DPHY_DEST_12[1:0]	
Reset	0x0		0x0		0x0		0x0	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_DPHY_DEST_15	7:6	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_15 and MAP_DST_15 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_14	5:4	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_14 and MAP_DST_14 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_13	3:2	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_13 and MAP_DST_13 mapping registers.	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3
MAP_DPHY_DEST_12	1:0	DPHY and CPHY Mapping destination controller register. CSI2 PHY destination for MAP_SRC_12 and MAP_DST_12 mapping registers	0b00: CSI2 controller 0 0b01: CSI2 controller 1 0b10: CSI2 controller 2 0b11: CSI2 controller 3

MIPI_TX49 (0x9B1, 0x9F1)

BIT	7	6	5	4	3	2	1	0
Field	MAP_CON[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MAP_CON	7:0	MIPI controller SYNC concatenation register. The register is split into four decode segments: Bit [7]: 1'b1 = 4WxH, 1'b0 = Wx4H Bit [6]: Reserved Bits [5:4]: Select the first line to concatenate. All others follow in order bits [3:0]. 2'b00 = Select Pipe 0 to be the master 2'b01 = Select Pipe 1 to be the master 2'b10 = Select Pipe 2 to be the master 2'b11 = Select Pipe 3 to be the master Bit [3]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 3 Bit [2]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 2 Bit [1]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 1 Bit [0]: 1'b0 = disable, 1'b1 = concatenate Video Pipe 0	0bXXXXXXX1: Concatenate Video Pipeline 0 0bXXXXXX1X: Concatenate Video Pipeline 1 0bXXXXX1XX: Concatenate Video Pipeline 2 0bXXXX1XXX: Concatenate Video Pipeline 3 0bXX00XXXX: Select Video Pipeline 0 as master 0bXX01XXXX: Select Video Pipeline 1 as master 0bXX10XXXX: Select Video Pipeline 2 as master 0bXX11XXXX: Select Video Pipeline 3 as master 0b0XXXXXXX: Enable Wx4H mode 0b1XXXXXXX: Enable 4WxH mode

MIPI_TX50 (0x9B2, 0x9F2)

BIT	7	6	5	4	3	2	1	0
Field	SKEW_PER_SEL[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SKEW_PER_SEL	7:0	Periodic deskew select register. The register is split into three decode segments: Bit [7]: Select periodic deskew calibration for one or all virtual channels Bits [6:5]: Reserved Bits [4:0]: Virtual channel to generate periodic deskew calibration when only one channel is selected by bit 7	0b0xxxxxxx: Generate periodic calibration deskew calibration on all virtual channels 0b1xx00000: Periodic deskew calibration generated by virtual Channel 0 0b1xx00001: Periodic deskew calibration generated by virtual Channel 1 0b1xx00010: Periodic deskew calibration generated by virtual Channel 2 0b1xx00011: Periodic deskew calibration generated by virtual Channel 3 0b1xx00100: Periodic deskew calibration generated by virtual Channel 4 0b1xx00101: Periodic deskew calibration generated by virtual Channel 5 0b1xx00110: Periodic deskew calibration generated by virtual Channel 6 0b1xx00111: Periodic deskew calibration generated by virtual Channel 7 0b1xx01000: Periodic deskew calibration generated by virtual Channel 8 0b1xx01001: Periodic deskew calibration generated by virtual Channel 9 0b1xx01010: Periodic deskew calibration generated by virtual Channel 10 0b1xx01011: Periodic deskew calibration generated by virtual Channel 11 0b1xx01100: Periodic deskew calibration generated by virtual Channel 12 0b1xx01101: Periodic deskew calibration generated by virtual Channel 13 0b1xx01110: Periodic deskew calibration generated by virtual Channel 14 0b1xx01111: Periodic deskew calibration generated by virtual Channel 15

MIPI_TX51 (0x9B3, 0x9F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ALT2_MEM_MAP8	MODE_DT	ALT_MEM_MAP10	ALT_MEM_MAP8	ALT_MEM_MAP12
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ALT2_MEM_MAP8	4	Alternative memory read mapping enable for 8-bit DT when sharing the same video pipe with RAW16	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
MODE_DT	3	Select 24-bit mode for user-defined data types	0b0: 24-bit mode for user-defined data types not enabled 0b1: 24-bit mode for user-defined data types enabled

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_MEM_MAP10	2	Alternative memory read mapping enable for 10-bit DT	0b0: Alternative memory read mapping not enabled for 10-bit DT 0b1: Alternative memory read mapping enabled for 10-bit DT
ALT_MEM_MAP8	1	Alternative memory read mapping enable for 8-bit DT	0b0: Alternative memory read mapping not enabled for 8-bit DT 0b1: Alternative memory read mapping enabled for 8-bit DT
ALT_MEM_MAP12	0	Alternative memory read mapping enable for 12-bit DT	0b0: Alternative memory read mapping not enabled for 12-bit DT 0b1: Alternative memory read mapping enabled for 12-bit DT

MIPI_TX52 (0x9B4, 0x9F4)

BIT	7	6	5	4	3	2	1	0
Field	video_masked_latched[3:0]				video_masked[3:0]			
Reset	0x0				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
video_masked_latched	7:4	Indicates video pipes 0-3 were masked off at one point while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off
video_masked	3:0	Video pipe currently masked off while in 4WxH or Wx4H synchronous aggregation mode.	0bXXX1: Video pipe 0 previously masked off 0bXX1X: Video pipe 1 previously masked off 0bX1XX: Video pipe 2 previously masked off 0b1XXX: Video pipe 3 previously masked off

MIPI_TX54 (0x9B6, 0x9F6)

BIT	7	6	5	4	3	2	1	0
Field	TUN_NO_CORR	DESKEW_TUN[1:0]		TUN_SER_LANE_NUM[1:0]		DESKEW_TUN_SRC[1:0]		TUN_EN
Reset	0x0	0x0		0x1		0x0		0x0
Access Type	Write, Read	Write, Read		Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_NO_CORR	7	Do not enable header error correction in tunneling mode	0x0: Automatic correction for correctable header error 0x1: Turn off correction for correctable header error
DESKEW_TUN	6:5	Deskew Mode for CSI2 Tunneling	0: periodic deskew as in HS94 (determined by deskew_per_* registers). 1: periodic deskew follows SER. 2: periodic deskew START follows SER but width as register defined. 3: not used

BITFIELD	BITS	DESCRIPTION	DECODE
TUN_SER_LANE_NUM	4:3	Tunneling Serializer Lane Number Used ONLY in tunneling mode when source is in CPHY mode	0x0: 1-lane 0x1: 2-lanes
DESKEW_TUN_SRC	2:1	Tunneling Deskew Source Select DESKEW_TUN_SRC register must select one of the mapped pipes for this controller.	0x0: Pipe 0 0x1: Pipe 1 0x2: Pipe 2 0x3: Pipe 3
TUN_EN	0	Tunneling Enabled This register takes effect only if DIS_AUTO_TUN_DET is 1.	0b0: Tunneling disabled 0b1: Tunneling enabled

MIPI_TX56 (0x9B8, 0x9F8)

BIT	7	6	5	4	3	2	1	0
Field	PKT_START_ADDR[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PKT_START_ADDR	7:0	Specifies the start address of the long packet. 0: The long packet is sent out when the whole line is filled in line memory. Not 0: The long packet begins when PKT_START_ADDR x 128 bytes are filled in the line memory in tunnel mode or when PKT_START_ADDR x 64 pixels are filled in the line memory in pixel mode. Make sure register n_vs_block is 2 or more (default = 1). Notes: • "Cut-through" only works with 1-3 virtual channels. May increase to 4 VCs in future revisions. • Bytes are packed differently into memory when in tunnel mode. For example, in tunnel mode, a BPP of 24 is equal to 1.33 pixels per address. In pixel mode, a BPP of 24 is equal to 1 pixel per address. • When in tunnel mode, the units for PKT_START_ADDR are in bytes. In pixel mode, the units are in pixels.

MIPI_TX57 (0x9B9, 0x9F9)

BIT	7	6	5	4	3	2	1	0
Field	DIS_AUTO_SER_LANE_DET	DIS_AUTO_TUN_DET	TUN_DEST[1:0]		–	TUN_DPHY_TO_CPHY_CONV	TUN_DPHY_TO_CPHY_CONV_OVRD	TUN_NO_CORR_LENGTH
Reset	0x0	0x0	0x1		–	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_AUTO_SER_LANE_DET	7	Disable auto SER lane count detect. When this register is set to 1 (automatic detection of SER lane count is disabled), TUN_SER_LANE_NUM register will need to be set to the SER lane count.	0b0: Tunneling disabled 0b1: Tunneling enabled
DIS_AUTO_TUN_DET	6	Disable auto tunneling mode detect. When this register is set to 1 (automatic detection of tunneling mode disabled), TUN_EN registers will set pixel mode (TUN_EN = 0) or tunneling mode (TUN_EN =1).	0b0: Tunneling disabled 0b1: Tunneling enabled
TUN_DEST	5:4	Tunneling Controller Destination	0x0: Controller 0 0x1: Controller 1
TUN_DPHY_TO_CPHY_CONV	2	Only used when TUN_DPHY_TO_CPHY_CONV_OVRD bit is set. Manual override bit to enable DPHY to CPHY conversion in tunneling mode (must also disable auto tunneling mode detect DIS_AUTO_TUN_DET = 1 and manually set tunneling mode TUN_EN = 1). When set to 0, SER headers are evaluated to detect DPHY/CPHY mode, if SER is sending DPHY and the DES MIPI PHY is sent to CPHY mode, conversion is turn on.	0x0: Controller 0 0x1: Controller 1
TUN_DPHY_TO_CPHY_CONV_OVRD	1	Enable value in TUN_DPHY_TO_CPHY_CONV register to override automatic detection.	0x0: Controller 0 0x1: Controller 1
TUN_NO_CORR_LENGTH	0	Do not enable header error packet length correction in tunneling mode	0b0: Tunneling error correction enabled 0b1: Tunneling error correction disabled

MIPI_ERR_INJ_B1 (0x9BA, 0x9FA)

BIT	7	6	5	4	3	2	1	0
Field	DCPHY_CONV_ERR_INJ_B1_EN	–	–	DCPHY_CONV_ERR_INJ_B1_SITE[4:0]				
Reset	0b0	–	–	0x00				
Access Type	Write Clears All, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DCPHY_CONV_ERR_INJ_B1_EN	7	Enable Error Injection for the first bit error injection location selection. See the DCPHY_CONV_ERR_INJ_B1_SITE register field description. Write 1 to trigger the error injection. This bit will self clear.	

BITFIELD	BITS	DESCRIPTION	DECODE
DCPHY_CONV_ERR_INJ_B1_SITE	4:0	First Bit Error injection location in the DPHY header. Used to inject errors into the MIPI DPHY standard output header which is then converted to MIPI CPHY standard output during tunnel mode.	0-7: DATA ID (DT) 8-23: DATA FIELD 24-30: ECC 31-32: VCX

MIPI_ERR_INJ_B2 (0x9BB, 0x9FB)

BIT	7	6	5	4	3	2	1	0
Field	DCPHY_CONV_ERR_INJ_B2_EN	–	–	DCPHY_CONV_ERR_INJ_B2_SITE[4:0]				
Reset	0b0	–	–	0x00				
Access Type	Write Clears All, Read	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
DCPHY_CONV_ERR_INJ_B2_EN	7	Enable Error Injection for the second bit error injection location selection. See the DCPHY_CONV_ERR_INJ_B2_SITE register field description. Write 1 to trigger the error injection. This bit will self clear.	
DCPHY_CONV_ERR_INJ_B2_SITE	4:0	Second Bit Error injection location in the DPHY header. Used to inject errors into the MIPI DPHY standard output header which is then converted to MIPI CPHY standard output during tunnel mode.	0-7: DATA ID (DT) 8-23: DATA FIELD 24-30: ECC 31-32: VCX

MIPI_DESKEW_ERRB_ORDER (0x9BC, 0x9FC)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DESKEW_BEFORE_ERRB_PKT_MODE	DESKEW_AFTER_ERRB_PKT_MODE	DESKEW_BEFORE_VS_PKT_MODE	–
Reset	–	–	–	–	0x0	0x0		–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
DESKEW_BEFORE_ERRB_PKT_MODE	3	This bit can control when the DESKEW occurs relative to ERRB_PKT. This register, DESKEW_BEFORE_ERRB_PKT_MODE, has priority over DESKEW_AFTER_ERRB_PKT_MODE Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW may occur before or after ERRB_PKT depending on other registers (see complete table) 0x1: DESKEW occurs before ERRB_PKT
DESKEW_AFTER_ERRB_PKT_MODE	2	This bit can control when the DESKEW occurs relative to ERRB_PKT. Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW may occur before or after ERRB_PKT depending on other registers (see complete table) 0x1: DESKEW occurs after ERRB_PKT
DESKEW_BEFORE_VS_PKT_MODE	1	This bit can control when the DESKEW occurs relative to a VS (frame-start or frame-end) pkt. Note: When trying to control the order of DESKEW, VS, and ERRB_PKT, please consider these registers: ERRB_PKT_Insert_Mode[1:0] ERRB_PKT_EDGE_SEL DESKEW_PER[6] DESKEW_BEFORE_VS_PKT_MODE DESKEW_AFTER_ERRB_PKT_MODE DESKEW_BEFORE_ERRB_PKT_MODE	0x0: DESKEW occurs after the VS pkt 0x1: DESKEW occurs before the VS pkt

GMSL1_4 (0xB04, 0xC04, 0xD04, 0xE04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PRBSEN	–	CC_PORT_SEL	–	REVCCEN	FWDCCEN
Reset	–	–	0x0	–	0b0	–	0x1	0x1
Access Type	–	–	Write, Read	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PRBSEN	5	PRBS test enable (in HIBW mode, PRBS_TYPE—0xB0F must be set to zero)	0b0: Set device normal operation 0b1: Enable PRBS test
CC_PORT_SEL	3	Selects which I^2C port is connected to this link	0b00: Port 0 (RX0_SDA0, TX0_SCL0) 0b01: Port 1 (RX1_SDA1, TX1_SCL1)
REVCCEN	1	Enables reverse control channel from deserializer	0b0: Disable reverse control channel receiver 0b1: Enable reverse control channel receiver
FWDCCEN	0	Enables forward control channel to deserializer	0b0: Disable forward control channel transmitter 0b1: Enable forward control channel transmitter

GMSL1_5 (0xB05, 0xC05, 0xD05, 0xE05)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	NO_REM_MST	HVTR_MODE	EN_EQ	EQTUNE[3:0]			
Reset	0x0	0x0	0x1	0x1	0x9			
Access Type		Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
NO_REM_MST	6	Set to 1 to indicate that there is no I^2C master on remote side so this (local) chip should ignore any I^2C packet initiation (start condition) from remote side	0b0: Master 0b1: No master
HVTR_MODE	5	HV tracking allows continuous HSYNC format	0b0: Use partial periodic HV tracking 0b1: Use partial and full periodic HV tracking
EN_EQ	4	Enables equalizer for manual and adaptive modes	0b0: Disable equalization 0b1: Enable equalization
EQTUNE	3:0	Equalizer boost level at 750 MHz (effective when adaptive EQ is turned off)	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_6 (0xB06, 0xC06, 0xD06, 0xE06)

BIT	7	6	5	4	3	2	1	0
Field	HIGHIMM	MAX_RT_EN	I2C_RT_EN	GPI_COMP_EN	GPI_RT_EN	HV_SRC[2:0]		
Reset	0x0	0x1	0x1	0x0	0x1	0x7		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
HIGHIMM	7	Reverse channel high immunity mode (initial value set by the CFG1/MFP6 pin state at power-up)	0b0: Reverse channel high immunity mode disabled 0b1: Reverse channel high immunity mode enabled
MAX_RT_EN	6	Maximum retransmission limit enable	0b0: Disable maximum retransmission limit 0b1: Enable maximum retransmission limit
I2C_RT_EN	5	I^2C retransmission enable	0b0: Disable I^2C retransmission 0b1: Enable I^2C retransmission enable
GPI_COMP_EN	4	Reverse channel high immunity mode (initial value set by the CFG1/MFP6 pin state at power-up)	0b0: Disable GPI skew compensation 0b1: Enable GPI skew compensation
GPI_RT_EN	3	GPI retransmission enable	0b0: Disable GPI retransmission 0b1: Enable GPI retransmission
HV_SRC	2:0	HS_VS bit selection	0b000: Use D18/D19 for HS/VS (use this setting when the serializer is a 3.125Gbps device or if HIBW mode is used; otherwise, this setting is for use with the MAX9273 when DBL = 0 or HVEN = 1) 0b001: Use D14/D15 for HS/VS (for use with the MAX9271/ MAX96705 when DBL = 0 or HVEN = 1) 0b010: Use D12/D13 for HS/VS (for use with the MAX96707 when DBL = 0 or HVEN = 1) 0b011: Use D0/D1 for HS/VS (for use with the MAX9271/ MAX9273/MAX96705/MAX96707 when DBL = 1 and HVEN = 0) 0b100: Reserved 0b101: Reserved 0b110: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96707) 0b111: Automatically determine the source of HSYNC/VSYNC (for use with the MAX96705)

GMSL1_7 (0xB07, 0xC07, 0xD07, 0xE07)

BIT	7	6	5	4	3	2	1	0
Field	DBL	DRS	BWS	–	HIBW	HVEN	–	PXL_CRC
Reset	0x0	0x0	0x0	–	0x0	0x1	–	0x0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DBL	7	Double-output mode	0b0: Use single-rate output 0b1: Use double-rate output (2x word rate at 1/2x width)

BITFIELD	BITS	DESCRIPTION	DECODE
DRS	6	Data rate select	0b0: Use normal data rate output 0b1: Use 1/2 rate data output (for use with low data rates)
BWS	5	Bus width select	0b0: Set bus width for 22-/24-bit bus, 24-/27-bit mode (depending on HIBW setting) 0b1: Set bus width for 30-bit bus (32-bit mode)
HIBW	3	High-bandwidth mode	0b0: Disable high-bandwidth mode 0b1: Enable high-bandwidth mode (when BWS = 0)
HVEN	2	HS/VS encoding enable	0b0: Disable HS/VS encoding 0b1: Enable HS/VS encoding
PXL_CRC	0	Pixel error detection type (this is controllable by pin when LCCEN = 0)	0b0: Use 1-bit parity (compatible with all devices) 0b1: Use 6-bit CRC

GMSL1_8 (0xB08, 0xC08, 0xD08, 0xE08)

BIT	7	6	5	4	3	2	1	0
Field	GPI_SEL[1:0]		GPI_EN	EN_FSYNC_TX	–	PKTCC_EN	CC_CRC_LENGTH[1:0]	
Reset	0x0		0x1	0x0	–	0x0	0x1	
Access Type	Write, Read		Write, Read	Write, Read	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_SEL	7:6	Selects GPI pin to transmit to serializer	0b00: GPI_0 0b01: GPI_1 0b10: GPI_2 0b11: GPI_3
GPI_EN	5	Enables GPI-to-GPO signal transmission to serializer	0b0: Disable GPI-to-GPO transmission 0b1: Enable GPI-to-GPO transmission
EN_FSYNC_TX	4	Enables frame sync signal transmission	0b0: Disable frame sync signal transmission 0b1: Enable frame sync signal transmission
PKTCC_EN	2	Packet-based control-channel mode enable	0b0: Disable packet-based control-channel mode 0b1: Enable packet-based control-channel mode
CC_CRC_LENGTH	1:0	Control channel CRC length	0b00: 1-bit CRC 0b01: 5-bit CRC 0b10: 8-bit CRC 0b11: Reserved

GMSL1_D (0xB0D, 0xC0D, 0xD0D, 0xE0D)

BIT	7	6	5	4	3	2	1	0
Field	I2C_LOC_ACK	RSVD	–	–	–	HS_TRACK_FSYNC	RSVD	RSVD
Reset	0x0	0x0	–	–	–	0x0	0x0	0x0
Access Type	Write, Read		–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_LOC_ACK	7	Enables I²C-to-I²C slave local acknowledge when forward channel is not available	0b0: Disable local acknowledge when forward channel is not available 0b1: Enable local acknowledge when forward channel is not available
HS_TRACK_FSYNC	2	0 = Allow infinite length vertical blanking 1 = Lose HLOCKED with VLOCKED	0x0: Allow infinite length vertical blanking 0x1: Lose HLOCKED with VLOCKED

GMSL1_E (0xB0E, 0xC0E, 0xD0E, 0xE0E)

BIT	7	6	5	4	3	2	1	0
Field	DET_THR[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_THR	7:0	Threshold for detected errors	0xXX: Number of errors for detected error threshold

GMSL1_F (0xB0F, 0xC0F, 0xD0F, 0xE0F)

BIT	7	6	5	4	3	2	1	0
Field	–	EN_DE_FILT	EN_HS_FILT	EN_VS_FILT	DE_EN	–	–	PRBS_TYPE
Reset	–	0x0	0x0	0x0	0x0	–	–	0x1
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DE_FILT	6	Enables glitch filtering on DE	0b0: Disable DE glitch filtering 0b1: Enable DE glitch filtering
EN_HS_FILT	5	Enables glitch filtering on HS	0b0: Disable HS glitch filtering 0b1: Enable HS glitch filtering
EN_VS_FILT	4	Enables glitch filtering on VS	0b0: Disable VS glitch filtering 0b1: Enable VS glitch filtering
DE_EN	3	Enables processing separate HS and DE signals	0b0: Disable processing HS and DE signals 0b1: Enable processing HS and DE signals
PRBS_TYPE	0	PRBS type select (in HIBW mode, set PRBS_TYPE = 0)	0b0: GMSL legacy style PRBS test 0b1: MAX9272 style PRBS test

GMSL1_10 (0xB10, 0xC10, 0xD10, 0xE10)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_TYPE[1:0]		RCEG_BOUND	RCEG_ERR_NUM[3:0]				RCEG_EN
Reset	0x0		0x0	0x1				0x0
Access Type	Write, Read		Write, Read	Write, Read				Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_TYPE	7:6	Reverse channel generated error type	0b00: Random 0b01: Short burst 0b10: Long burst 0b11: Long burst
RCEG_BOUND	5	Reverse channel generated error boundary (effective when RCEG_TYPE = 0x)	0b0: Errors are unbounded to symbols 0b1: Errors are bounded to symbols
RCEG_ERR_NUM	4:1	Number of RCEG errors generated with each request (effective when RCEG_TYPE = 0x)	0xX: Number of errors generated per request
RCEG_EN	0	Enable reverse channel error generator	0b0: Disable reverse channel error generator 0b1: Enable reverse channel error generator enabled

GMSL1_11 (0xB11, 0xC11, 0xD11, 0xE11)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_RATE[3:0]				RCEG_LO_BST_PRB[1:0]		RCEG_LO_BST_LEN[1:0]	
Reset	0xF				0x0		0x0	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_RATE	7:4	Error generation rate in terms of bit time = $2^{-(RCEG\_ERR\_RATE + 3)}$. Effective when RCEG_TYPE = 0X.	0x0: Rate is 2^{-3} 0x1: Rate is 2^{-4} 0x2: Rate is 2^{-5} ... ... 0xF: Rate is 2^{-18}
RCEG_LO_BST_PRB	3:2	Long burst error probability. Effective when RCEG_TYPE = 10.	0b00: 1/1024 0b01: 1/128 0b10: 1/32 0b11: 1/8
RCEG_LO_BST_LEN	1:0	Long burst error length in terms of bit time. Effective when RCEG_TYPE = 10.	0b00: Continuous 0b01: 128 (~150µs) 0b10: 8192 (~9.83ms) 0b11: 1048576 (~1.26s)

GMSL1_12 (0xB12, 0xC12, 0xD12, 0xE12)

BIT	7	6	5	4	3	2	1	0
Field	UNDERBST_DET_EN	CC_CRC_ERR_EN	LINE_CRC_LOC[1:0]		LINE_CRC_EN_GMSL1	–	MAX_RT_ERR_EN	RCEG_ERR_PER_EN
Reset	0x0	0b1	0x1		0x0	–	0b1	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBST_DET_EN	7	Enable underboost detection	0b0: Disable underboost detection 0b1: Enable underboost detection

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERR_EN	6	Enables reporting of (CC_CRC_ERR_CNT > 0) on the ERRB pin. Note: This only applies to the composite GMSL1 error output to the ERRB pin. See registers G1_A_ERR_OEN, G1_B_ERR_OEN, G1_C_ERR_OEN, and G1_D_ERR_OEN For individual control see register CC_CRC_ERRB_OEN.	
LINE_CRC_LOC	5:4	Video line CRC insertion location	0b00: [1..4] 0b01: [5..8] 0b10: [9..12] 0b11: [13..16]
LINE_CRC_EN_GMSL1	3	Video line CRC enable	0b0: Disable video line CRC 0b1: Enable video line CRC
MAX_RT_ERR_EN	1	Enables reflection of maximum retransmission error on the ERRB pin. Note: This control only applies to the composite GMSL1 ERRB output. See registers G1_A_ERRB_OEN, G1_B_ERRB_OEN, G1_C_ERRB_OEN, and G1_D_ERRB_OEN This applies to both I^2C retransmissions as well as GPI transmissions. For individual control see registers MAX_RT_I2C_ERRB_OEN and MAX_RT_GPI_ERRB_OEN.	0b0: Disable maximum retransmission error on the ERROR pin 0b1: Enable maximum retransmission error on the ERROR pin
RCEG_ERR_PER_EN	0	Periodic error generation enable. Effective when RCEG_TYPE (0xB10) = 0x.	0b0: Disable periodic error generator 0b1: Enable periodic error generator

GMSL1_13 (0xB13, 0xC13, 0xD13, 0xE13)

BIT	7	6	5	4	3	2	1	0
Field	EOM_EN_G1	EOM_PER_MODE_G1	EOM_MAN_TRG_REQ_G1	EOM_MIN_THR_G1[4:0]				
Reset	0x1	0x1	0x0	0x00				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EN_G1	7	Eye-opening monitor enable	0b0: Disable EOM 0b1: Enable EOM
EOM_PER_MODE_G1	6	Eye-opening monitor periodic mode select	0b0: Set EOM to use nonperiodic mode 0b1: Set EOM to use periodic mode
EOM_MAN_TRG_REQ_G1	5	Eye-opening monitor (EOM) manual trigger request. Valid on the rising edge of this bit when not in periodic mode.	0b0: Do not trigger EOM 0b1: Manually trigger the EOM

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_MIN_THR_G1	4:0	Eye-opening minimum threshold (in terms of percent) for flagging ERRB pin	0b00000: Disabled 0b00001: 3.125% 0b00010: 6.25% 0b11111: 100%

GMSL1_14 (0xB14, 0xC14, 0xD14, 0xE14)

BIT	7	6	5	4	3	2	1	0
Field	AEQ_EN	AEQ_PER_MODE	AEQ_MAN_TRG_REQ	EOM_PER_THR[4:0]				
Reset	0x1	0x0	0x0	0x00				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEQ_EN	7	Adaptive equalization enable	0b0: Disable AEQ 0b1: Enable AEQ
AEQ_PER_MODE	6	Adaptive equalizer periodic mode select	0b0: Set AEQ to use nonperiodic mode 0b1: Set AEQ to use periodic mode
AEQ_MAN_TRG_REQ	5	Adaptive equalizer manual fine-tune request enable. Valid on the rising edge of this bit when not in periodic mode.	0b0: Do not trigger AEQ fine tuning 0b1: Manually trigger the AEQ fine tuning
EOM_PER_THR	4:0	Eye-opening threshold to trigger a fine-tune operation	0b00000: Eye-opening threshold is disabled 0b10000: 50% eye-opening triggers fine-tune operation All other values: Reserved

GMSL1_15 (0xB15, 0xC15, 0xD15, 0xE15)

BIT	7	6	5	4	3	2	1	0
Field	DET_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
DET_ERR	7:0	Detected error counter	0xXX: Number of detected errors

GMSL1_16 (0xB16, 0xC16, 0xD16, 0xE16)

BIT	7	6	5	4	3	2	1	0
Field	PRBS_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
PRBS_ERR	7:0	PRBS error counter	0xXX: Number of detected PRBS errors

GMSL1_17 (0xB17, 0xC17, 0xD17, 0xE17)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MAX_RT_ERR_I2C	PRBS_OK	GPI_IN	MAX_RT_ERR_GPI	–	–	–
Reset	0x0	0x0	0x0	0x0	0x0	–	–	–
Access Type		Read Only	Read Only	Read Only	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
MAX_RT_ERR_I2C	6	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached
PRBS_OK	5	MAX9271/73 compatible PRBS test for link is completed normally. Check PRBS_ERR register for the PRBS success. For other SERDES read PRBS_ERR registers.	0b0: No MAX9271/MAX9273 compatible PRBS test completed 0b1: MAX9271/MAX9273 compatible PRBS test completed normally
GPI_IN	4	GPI pin level	0b0: GPI is input low 0b1: GPI is input high
MAX_RT_ERR_GPI	3	Maximum retransmission error flag. Cleared when read.	0b0: No control-channel retransmission error 0b1: Control-channel retransmission maximum limit reached

GMSL1_18 (0xB18, 0xC18, 0xD18, 0xE18)

BIT	7	6	5	4	3	2	1	0
Field	CC_RETR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_RETR_CNT	7:0	I^2C packet retransmit count	0xXX: Number of I^2C packets retransmitted

GMSL1_19 (0xB19, 0xC19, 0xD19, 0xE19)

BIT	7	6	5	4	3	2	1	0
Field	CC_CRC_ERRCNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CC_CRC_ERRCNT	7:0	Packet-based control-channel CRC error counter	0xXX: Number of control-channel CRC errors

GMSL1_1A (0xB1A, 0xC1A, 0xD1A, 0xE1A)

BIT	7	6	5	4	3	2	1	0
Field	RCEG_ERR_CNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
RCEG_ERR_CNT	7:0	Control-channel number of generated errors	0xXX: Number of control-channel generated errors

GMSL1_1B (0xB1B, 0xC1B, 0xD1B, 0xE1B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	LINE_CRC_ERR	–	–
Reset	–	–	–	–	–	0x0	–	–
Access Type	–	–	–	–	–	Read Only	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
LINE_CRC_ERR	2	CRC error bit. Latched on error, cleared to 0 when read.	0b0: Video line CRC ok 0b1: Video line CRC mismatch detected

GMSL1_1C (0xB1C, 0xC1C, 0xD1C, 0xE1C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EOM_EYE_WIDTH[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
EOM_EYE_WIDTH	5:0	Measured eye opening. Opening width = EOM_EYE_WIDTH/63 x 100%	0b000000: Width is 0% 0b000001: Width is 1/63 x 100% 0b000010: Width is 2/63 x 100% ... ... 0b11111: Width is 63/63 x 100%

GMSL1_1D (0xB1D, 0xC1D, 0xD1D, 0xE1D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	UNDERBOOST_DET	AEQ_BST[3:0]			
Reset	–	–	–	0x0	0x0			
Access Type	–	–	–	Read Only	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
UNDERBOOST_DET	4	Underboost detected	0b0: Normal operation 0b1: Underboost (at maximum AEQ gain) detected
AEQ_BST	3:0	Adaptive equalizer boost value. Selected adaptive equalizer value; settings correspond to gain at 750MHz	0b0000: 1.6dB manual EQ setting 0b0001: 2.1dB manual EQ setting 0b0010: 2.8dB manual EQ setting 0b0011: 3.5dB manual EQ setting 0b0100: 4.3dB manual EQ setting 0b0101: 5.2dB manual EQ setting 0b0110: 6.3dB manual EQ setting 0b0111: 7.3dB manual EQ setting 0b1000: 8.5dB manual EQ setting 0b1001: 9.7dB manual EQ setting 0b1010: 11dB manual EQ setting 0b1011: 12.2dB manual EQ setting 0b1100: Reserved 0b1101: Reserved 0b1110: Reserved 0b1111: Reserved

GMSL1_20 (0xB20, 0xC20, 0xD20, 0xE20)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_0[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_0	7:0	Bits [7:0] of CRC output for the latest line	0xXX: CRC[7:0] of latest line

GMSL1_21 (0xB21, 0xC21, 0xD21, 0xE21)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_1[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_1	7:0	Bits [15:8] of CRC output for the latest line	0xXX: CRC[15:8] of latest line

GMSL1_22 (0xB22, 0xC22, 0xD22, 0xE22)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_2[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_2	7:0	Bits [23:16] of CRC output for the latest line	0xXX: CRC[23:16] of latest line

GMSL1_23 (0xB23, 0xC23, 0xD23, 0xE23)

BIT	7	6	5	4	3	2	1	0
Field	CRC_VALUE_3[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_VALUE_3	7:0	Bits [31:24] of CRC output for the latest line	0xXX: CRC[31:24] of latest line

GMSL1_96 (0xB96, 0xC96, 0xD96, 0xE96)

BIT	7	6	5	4	3	2	1	0
Field	CONV_GMSL1_DATATYPE[4:0]					RSVD	CONV_GMSL1_EN	DBL_ALIGN_TO
Reset	0x07					0x0	0x1	0x1
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONV_GMSL1_DATATYPE	7:3	Converts from GMSL1 color format mapping to GMSL2 CSI transmitter color format	0x0: RGB888 OLDI 0x1: RGB565 0x2: RGB666 0x3: YUV422 8-bit mux mode (use yuv_8_10_mux_mode) 0x4: YUV422 10-bit mux mode (use yuv_8_10_mux_mode) 0x5: RAW8 single 0x6: RAW10 single 0x7: RAW12 single 0x8: RAW14 0x9: User-defined generic 24-bit 0xA: User-defined YUV422 12-bit 0xB: User-defined generic 8-bit 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved 0x10: RGB888 VESA 0x11: Reserved 0x12: Reserved 0x13: YUV422 8-bit normal mode 0x14: YUV422 10-bit normal mode 0x15: RAW8 double (use alt_mem_map8) 0x16: RAW10 double (use alt_mem_map10) 0x17: RAW12 double (use alt_mem_map12) 0x18: Reserved 0x19: Reserved 0x1A: Reserved 0x1B: Reserved 0x1C: Reserved 0x1D: Reserved 0x1E: Reserved 0x1F: Reserved
CONV_GMSL1_EN	1	Enable conversion from GMSL1 color format mapping to GMSL2 CSI transmitter	0x0: GMSL1 color format conversion to GMSL2 not Enabled 0x1: GMSL1 color format conversion to GMSL2 Enabled
DBL_ALIGN_TO	0	HBM DBL mode type 1 = DBL-DBL mode with no alignment(d) 0 = DBL-Single mode with alignment	

GMSL1_CB (0xBCB, 0xCCB, 0xDCB, 0xECB)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	LOCKED_G1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type								Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
LOCKED_G1	0	Link Locked	0b0: Link not locked 0b1: Link locked

TX1 (0x1001)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type		–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error generator enable	0b0: Disable error generator for Link A 0b1: Enable error generator for Link A

TX2 (0x1002)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 0b10: 128 0b11: 1024
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits
ERRG_BURST	3:1	Error generator burst error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x1003)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0x4		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. Timeout Base = 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x1004)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0b0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Select the sub-type of low-bandwidth packets to count at PKT_CNT register	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved
PKT_CNT_SEL	3:0	Select the type of received packets to count at PKT_CNT (0x40–0x43)	0b0000: None 0b0001: Video 0b0010: Reserved 0b0011: INFOFR 0b0100: Reserved 0b0101: I^2C 0b0110: Reserved 0b0111: GPIO 0b1000: Reserved 0b1001: Reserved 0b1010: Reserved 0b1011: Reserved 0b1100: Reserved 0b1101: Reserved 0b1110: All non-idle packets 0b1111: Unknown/Error

GPIOA (0x1008)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0x1	0x01					
Access Type		Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_CASC	6	Allow multiple pin transitions to be transmitted in the same packet	0b0: Multiple pin transitions not allowed 0b1: Multiple pin transitions allowed

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x1009)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x08					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwdith usage efficiency.	0b00: Disabled 0b01: 200ns 0b10: 500ns 0b11: 1000ns
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

TX1 (0x1011, 0x1021, 0x1031)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	–	–	ERRG_EN	–	–	RSVD	RSVD
Reset	0b0	–	–	0b0	–	–	0b0	0b0
Access Type		–	–	Write, Read	–	–		

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_EN	4	Error generator enable	0b0: Disable error generator 0b1: Enable error generator

TX2 (0x1012, 0x1022, 0x1032)

BIT	7	6	5	4	3	2	1	0
Field	ERRG_CNT[1:0]		ERRG_RATE[1:0]		ERRG_BURST[2:0]			ERRG_PER
Reset	0x0		0x2		0x0			0b0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ERRG_CNT	7:6	Number of errors to be generated	0b00: Continuous 0b01: 16 errors 0b10: 128 errors 0b11: 1024 errors
ERRG_RATE	5:4	Error generator average bit error rate	0b00: 1/5120 bits 0b01: 1/81920 bits 0b10: 1/1310720 bits 0b11: 1/20971520 bits
ERRG_BURST	3:1	Error generator burst error length	0b000: 1 0b001: 2 0b010: 3 0b011: 4 0b100: 8 0b101: 12 0b110: 16 0b111: 20
ERRG_PER	0	Error generator error distribution selection	0b0: Pseudorandom 0b1: Periodic

TX3 (0x1013, 0x1023, 0x1033)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		–	–	–	TIMEOUT[2:0]		
Reset	0x1		–	–	–	0x4		
Access Type			–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
TIMEOUT	2:0	Link ARQ Timeout Duration Multiplier Multiplies a timeout base constant to set the ARQ timeout. Timeout Base = 8µs	0b000: 0.5 x Timeout Base 0b001: 1.0 x Timeout Base 0b010: 1.5 x Timeout Base 0b011: 2.0 x Timeout Base 0b100: 2.5 x Timeout Base 0b101: 3.0 x Timeout Base 0b110: 3.5 x Timeout Base 0b111: 4.0 x Timeout Base

RX0 (0x1014, 0x1024, 0x1034)

BIT	7	6	5	4	3	2	1	0
Field	PKT_CNT_LBW[1:0]		–	RSVD	PKT_CNT_SEL[3:0]			
Reset	0x0		–	0b0	0x0			
Access Type	Write, Read		–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_LBW	7:6	Selects the sub-type of low-bandwidth packets to count at PKT_CNT_x bitfield (0x40–0x43).	0b00: Count data packets 0b01: Count acknowledge packets 0b10: Count data and acknowledge packets 0b11: Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
PKT_CNT_SEL	3:0	Selects the type of received packets to count at PKT_CNT_x bitfield (0x40–0x43)	0x0: None 0x1: Video 0x2: Reserved 0x3: INFOFR 0x4: Reserved 0x5: I^2C 0x6: Reserved 0x7: GPIO 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: All non-idle packets 0xF: Unknown/Error

GPIOA (0x1018, 0x1028, 0x1038)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	GPIO_TX_CASC	GPIO_FWD_CDLY[5:0]					
Reset	0b0	0x1	0x01					
Access Type		Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_CASC	6	Allows multiple pin transitions to be transmitted in the same packet	0b0: Multiple pin transitions not allowed 0b1: Multiple pin transitions allowed
GPIO_FWD_CDLY	5:0	Compensation delay multiplier for the forward direction. This must be same value as GPIO_FWD_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 3.4µs.	0bXXXXXX: Forward compensation delay multiplier value

GPIOB (0x1019, 0x1029, 0x1039)

BIT	7	6	5	4	3	2	1	0
Field	GPIO_TX_WNDW[1:0]		GPIO_REV_CDLY[5:0]					
Reset	0x2		0x08					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_TX_WNDW	7:6	Wait time after a GPIO transition to create a packet. This allows grouping transitions of different GPIO inputs in a single packet and so increases GPIO bandwidth usage efficiency.	0b00: Disabled 0b01: 200 ns 0b10: 500 ns 0b11: 1000 ns

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_REV_CDLY	5:0	Compensation delay multiplier for the reverse direction. This must be same value as GPIO_REV_CDLY of the chip on the other side of the link. Total delay is the (value + 1) multiplied by 1.7µs. Default delay is 15.3µs.	0bXXXXXX: Reverse compensation delay multiplier value

PATGEN_0 (0x1050)

BIT	7	6	5	4	3	2	1	0
Field	GEN_VS	GEN_HS	GEN_DE	VS_INV	HS_INV	DE_INV	VTG_MODE[1:0]	
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_VS	7	Enable to generate VS output according to the timing definition	0b0: Do not generate VS 0b1: Generate VS
GEN_HS	6	Enable to generate HS output according to the timing definition Also, consider setting LS_LE_EN* to 1 as this bit defaults to 0 for some parts.	0b0: Do not generate HS 0b1: Generate HS
GEN_DE	5	Enable to generate DE output according to the timing definition	0b0: Do not generate DE 0b1: Generate DE
VS_INV	4	Inverts VSYNC output of video timing generator	0b0: Do not invert VS 0b1: Invert VS
HS_INV	3	Inverts HSYNC output of video timing generator	0b0: Do not invert HS 0b1: Invert HS
DE_INV	2	Inverts DE output of video timing generator	0b0: Do not invert DE 0b1: Invert DE

BITFIELD	BITS	DESCRIPTION	DECODE
VTG_MODE	1:0	Video interface timing generation mode. 00 or 11 = VS tracking mode. VS input's period (VS_HIGH + VS_LOW) is tracked. After VS tracking is locked, any VS input edge (glitches) not in the expected PCLK cycle is ignored. VS tracking is locked with three consecutive matches and unlocked by three consecutive mismatches. When unlocked or power-up, the next VS input edge is assumed to be the right VS edge. 01 = VS one-trigger mode One VS input edge will trigger the generation of one frame of VSO/HSO/DEO. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO. 10 = Auto-repeat mode (default) VS input edge will trigger the generation of continuous frames of VSO/HSO/DEO even if there are no more VS input edges. If next VS input edge comes earlier or later than expected by VS period, the newly generated frame will be correct. The current VSO/HSO/DEO will be cut or extended at the time point of rising edge of the newly generated VSO/HSO/DEO.	0b00: VS tracking mode 0b01: VS on trigger mode 0b10: Auto-repeat mode 0b11: Free-running mode

PATGEN_1 (0x1051)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_MODE	–	PATGEN_MODE[1:0]		–	–	–	VS_TRIG
Reset	0x0	–	0x0		–	–	–	0x0
Access Type	Write, Read	–	Write, Read		–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_MODE	7	Gradient pattern generator mode	0b0: Gradient mode disabled 0b1: Gradient mode enabled
PATGEN_MODE	5:4	Pattern generator mode	0b00: Reserved 0b01: Generate checkerboard pattern 0b10: Generate gradient pattern 0b11: Reserved
VS_TRIG	0	Select VS trigger edge	0b0: Falling edge 0b1: Rising edge

VS_DLY_2 (0x1052)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_2	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [23:16])	0xXX: Most significant byte of VS delay

VS_DLY_1 (0x1053)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_1	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [15:8])	0xXX: Middle significant byte of VS delay

VS_DLY_0 (0x1054)

BIT	7	6	5	4	3	2	1	0
Field	VS_DLY_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DLY_0	7:0	VS delay in terms of PCLK cycles. The output VS is delayed by VS_DELAY cycles from the input VS. (bits [7:0])	0xXX: Least significant byte of VS delay

VS_HIGH_2 (0x1055)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_2	7:0	VS high period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS high period

VS_HIGH_1 (0x1056)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_1[7:0]							
Reset	0x2A							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_1	7:0	VS high period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS high period

VS_HIGH_0 (0x1057)

BIT	7	6	5	4	3	2	1	0
Field	VS_HIGH_0[7:0]							
Reset	0xF8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_HIGH_0	7:0	VS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS high period

VS_LOW_2 (0x1058)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_2[7:0]							
Reset	0x26							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_2	7:0	VS low period in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS low period

VS_LOW_1 (0x1059)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_1[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_1	7:0	VS low period in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS low period

VS_LOW_0 (0x105A)

BIT	7	6	5	4	3	2	1	0
Field	VS_LOW_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VS_LOW_0	7:0	VS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS low period

V2H_2 (0x105B)

BIT	7	6	5	4	3	2	1	0
Field	V2H_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_2	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first HS rising edge

V2H_1 (0x105C)

BIT	7	6	5	4	3	2	1	0
Field	V2H_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_1	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first HS rising edge

V2H_0 (0x105D)

BIT	7	6	5	4	3	2	1	0
Field	V2H_0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2H_0	7:0	VS edge to the rising edge of the first HS in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of VS edge to first HS rising edge

HS_HIGH_1 (0x105E)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_1	7:0	HS high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS high period

HS_HIGH_0 (0x105F)

BIT	7	6	5	4	3	2	1	0
Field	HS_HIGH_0[7:0]							
Reset	0xD0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_HIGH_0	7:0	HS high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS high period

HS_LOW_1 (0x1060)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_1[7:0]							
Reset	0x09							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_1	7:0	HS low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of HS low period

HS_LOW_0 (0x1061)

BIT	7	6	5	4	3	2	1	0
Field	HS_LOW_0[7:0]							
Reset	0x50							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_LOW_0	7:0	HS low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of HS low period

HS_CNT_1 (0x1062)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_1	7:0	HS pulses per frame (bits [15:8])	0xXX: Most significant byte of HS pulses per frame

HS_CNT_0 (0x1063)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0[7:0]							
Reset	0xDA							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
HS_CNT_0	7:0	HS pulses per frame (bits [7:0])	0xXX: Least significant byte of HS pulses per frame

V2D_2 (0x1064)

BIT	7	6	5	4	3	2	1	0
Field	V2D_2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_2	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Most significant byte of VS edge to first DE

V2D_1 (0x1065)

BIT	7	6	5	4	3	2	1	0
Field	V2D_1[7:0]							
Reset	0x55							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_1	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [15:8])	0xXX: Middle significant byte of VS edge to first DE

V2D_0 (0x1066)

BIT	7	6	5	4	3	2	1	0
Field	V2D_0[7:0]							
Reset	0xF0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
V2D_0	7:0	VS edge to the rising edge of the first DE in terms of PCLK cycles (bits [23:16])	0xXX: Least significant byte of VS edge to first DE

DE_HIGH_1 (0x1067)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_1[7:0]							
Reset	0x07							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_1	7:0	DE high period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE high period

DE_HIGH_0 (0x1068)

BIT	7	6	5	4	3	2	1	0
Field	DE_HIGH_0[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_HIGH_0	7:0	DE high period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE high period

DE_LOW_1 (0x1069)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_1	7:0	DE low period in terms of PCLK cycles (bits [15:8])	0xXX: Most significant byte of DE low period

DE_LOW_0 (0x106A)

BIT	7	6	5	4	3	2	1	0
Field	DE_LOW_0[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_LOW_0	7:0	DE low period in terms of PCLK cycles (bits [7:0])	0xXX: Least significant byte of DE low period

DE_CNT_1 (0x106B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_1	7:0	Active lines per frame (bits [15:8])	0xXX: Most significant byte of DE pulses per frame

DE_CNT_0 (0x106C)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0[7:0]							
Reset	0xB0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0	7:0	Active lines per frame (bits [7:0])	0xXX: Least significant byte of DE pulses per frame

GRAD_INCR (0x106D)

BIT	7	6	5	4	3	2	1	0
Field	GRAD_INCR[7:0]							
Reset	0x06							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GRAD_INCR	7:0	Gradient mode increment amount (increment amount is the register value divided by 4)	0xXX: Gradient increment base

CHKR_COLOR_A_L (0x106E)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_L[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_L	7:0	Checkerboard mode color A low byte	0xXX: Least significant byte of checkerboard mode color A

CHKR_COLOR_A_M (0x106F)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_M[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_M	7:0	Checkerboard mode color A middle byte	0xXX: Middle significant byte of checkerboard mode color A

CHKR_COLOR_A_H (0x1070)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_A_H[7:0]							
Reset	0x04							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_A_H	7:0	Checkerboard mode color A high byte	0xXX: Most significant byte of checkerboard mode color A

CHKR_COLOR_B_L (0x1071)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_L[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_L	7:0	Checkerboard mode color B low byte	0xXX: Least significant byte of checkerboard mode color B

CHKR_COLOR_B_M (0x1072)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_M[7:0]							
Reset	0x08							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_M	7:0	Checkerboard mode color B middle byte	0xXX: Middle significant byte of checkerboard mode color B

CHKR_COLOR_B_H (0x1073)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_COLOR_B_H[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_COLOR_B_H	7:0	Checkerboard mode color B high byte	0xXX: Most significant byte of checkerboard mode color B

CHKR_RPT_A (0x1074)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_A[7:0]							
Reset	0x50							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_A	7:0	Checkerboard mode color A repeat count	0xXX: Repeat count of checkerboard mode color A

CHKR_RPT_B (0x1075)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_RPT_B[7:0]							
Reset	0x50							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_RPT_B	7:0	Checkerboard mode color B repeat count	0xXX: Repeat count of checkerboard mode color B

CHKR_ALT (0x1076)

BIT	7	6	5	4	3	2	1	0
Field	CHKR_ALT[7:0]							
Reset	0x50							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHKR_ALT	7:0	Checkerboard mode alternate line count	0xXX: Checkerboard mode alternate line count

DP_ORSTB_CTL (0x1191)

BIT	7	6	5	4	3	2	1	0
Field	DPLL_AUTO_RST	DP_RST_MIPI3	DP_RST_STABLE	DP_RST_MIPI2	DP_RST_MIPI	DP_RST_VP	DP_RST_FS	DP_RST_CC
Reset	0x1	0x1	0x1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DPLL_AUTO_RST	7		0x0: No auto reset will be generated (If user changes phy0_csi_tx_dpll_predef_freq, assert either config_soft_rst_n_CSI1, config_soft_rst_n_CSI2, or phy_Stdby_n[1:0]. 0x1: When changes to phy#_csi_tx_dpll_predef_freq occur, a reset pulse to associated csipll#_rstb is generated. When changes to phy_4x2, phy_2x4, force_csi_out_en occur (or any write to 0x08A0), a reset pulse to all csipll#_rstb is generated.
DP_RST_MIPI3	6	Selects RST mode CMD FIFO read pointer	0b0: Rev B behavior – CMD FIFO read pointer is not reset automatically when video lock is lost 0b1: (Default) Rev C behavior – CMD FIFO read pointer is reset automatically when video lock is lost
DP_RST_STABLE	5	Selects RST mode	0b0: Do not prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior) 0b1: (Default) Prevent reset glitches when changing reset behavior between individualized resets (Rev C behavior) vs. non-individualized resets (Rev B behavior)
DP_RST_MIPI2	4	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset automatically based on the associated GMSL PHY and Video Pipe reset during a one-shot reset or link reset

BITFIELD	BITS	DESCRIPTION	DECODE
DP_RST_MIPI	3	Selects RST mode to MIPI controllers.	0b0: (Default) Rev B behavior – All MIPI controllers will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each MIPI controller can be reset individually based on RST_MIPITX_LOC[3:0] (0x8C9)
DP_RST_VP	2	Selects RST mode to video_rx, vrx blocks.	0b0: (Default) Rev B behavior – All video pipes will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each video pipe will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset
DP_RST_FS	1	Selects reset mode to frame sync block	0b0: (Default) Rev B behavior – Frame sync block will be reset during any one-shot reset or link reset 0b1: Rev C behavior – The internal frame sync block will not be reset during a one-shot reset or link reset
DP_RST_CC	0	Selects reset mode for iic_mux_uart blocks	0b0: (Default) Rev B behavior – All I^2C ports will be reset during any one-shot reset or link reset 0b1: Rev C behavior – Each I^2C port will be reset individually based on the associated GMSL PHY reset during a one-shot reset or link reset

CNT_AX (0x11D0)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AX	7:0	Total number of video pixel CRC errors detected at video stream AX. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream AX

CNT_AY (0x11D1)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AY	7:0	Total number of video pixel CRC errors detected at video stream AY. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream AY

CNT_AZ (0x11D2)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AZ	7:0	Total number of video pixel CRC errors detected at video stream AZ. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream AZ

CNT_AU (0x11E0)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_AU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_AU	7:0	Total number of video pixel CRC errors detected at video stream AU. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream AU

CNT_BX (0x11E1)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BX	7:0	Total number of video pixel CRC errors detected at video stream BX. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream BX

CNT_BY (0x11E2)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BY	7:0	Total number of video pixel CRC errors detected at video stream BY. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream BY

CNT_BZ (0x11E3)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BZ	7:0	Total number of video pixel CRC errors detected at video stream BZ. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream BZ

CNT_BU (0x11E4)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_BU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_BU	7:0	Total number of video pixel CRC errors detected at video stream BU. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream BU

CNT_CX (0x11E5)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CX	7:0	Total number of video pixel CRC errors detected at video stream CX. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream CX

CNT_CY (0x11E6)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CY	7:0	Total number of video pixel CRC errors detected at video stream CY. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream CY

CNT_CZ (0x11E7)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CZ	7:0	Total number of video pixel CRC errors detected at video stream CZ. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream CZ

CNT_CU (0x11E8)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_CU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_CU	7:0	Total number of video pixel CRC errors detected at video stream CU. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream CU

CNT_DX (0x11E9)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DX[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DX	7:0	Total number of video pixel CRC errors detected at video stream DX. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream DX

CNT_DY (0x11EA)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DY[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DY	7:0	Total number of video pixel CRC errors detected at video stream DY. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream DY

CNT_DZ (0x11EB)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DZ[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DZ	7:0	Total number of video pixel CRC errors detected at video stream DZ. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream DZ

CNT_DU (0x11EC)

BIT	7	6	5	4	3	2	1	0
Field	VID_PXL_CRC_ERR_DU[7:0]							
Reset	0x00							
Access Type	Read Clears All							

BITFIELD	BITS	DESCRIPTION	DECODE
VID_PXL_CRC_ERR_DU	7:0	Total number of video pixel CRC errors detected at video stream DU. Reset after reading or with the rising edge of LOCK. Note: With STREAM_SEL_ALL set to 1 or enabled (default), all Video Pixel CRC Errors will end up at video stream X only. If desired, set STREAM_SEL_ALL to 0 or disabled to allow visibility on specific video pixel stream CRC errors by matching SER STR_SEL and DES PIPE_SEL.	0xXX: Total number of video pixel CRC errors detected at video stream DU

DE_DET (0x11F0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_DET_3	DE_DET_2	DE_DET_1	DE_DET_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_3	3	DE activity is detected in Video Pipe 3. Bit stays high if DE period < ~1ms.	0b0: DE is not detected 0b1: DE is detected

BITFIELD	BITS	DESCRIPTION	DECODE
DE_DET_2	2	DE activity is detected in Video Pipe 2. Bit stays high if DE period < ~1ms.	0b0: DE is not detected 0b1: DE is detected
DE_DET_1	1	DE activity is detected in Video Pipe 1. Bit stays high if DE period < ~1ms.	0b0: DE is not detected 0b1: DE is detected
DE_DET_0	0	DE activity is detected in Video Pipe 0. Bit stays high if DE period < ~1ms.	0b0: DE is not detected 0b1: DE is detected

HS_DET (0x11F1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_DET_3	HS_DET_2	HS_DET_1	HS_DET_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HS_DET_3	3	HS activity is detected in Video Pipe 3. Bit stays high if HS period < ~1ms.	0b0: HS is not detected 0b1: HS is detected
HS_DET_2	2	HS activity is detected in Video Pipe 2. Bit stays high if HS period < ~1ms.	0b0: HS is not detected 0b1: HS is detected
HS_DET_1	1	HS activity is detected in Video Pipe 1. Bit stays high if HS period < ~1ms.	0b0: HS is not detected 0b1: HS is detected
HS_DET_0	0	HS activity is detected in Video Pipe 0. Bit stays high if HS period < ~1ms.	0b0: HS is not detected 0b1: HS is detected

VS_DET (0x11F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VS_DET_3	VS_DET_2	VS_DET_1	VS_DET_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS_DET_3	3	VS activity is detected in Video Pipe 3. Bit stays high if VS period < ~128ms.	0b0: VS is not detected 0b1: VS is detected
VS_DET_2	2	VS activity is detected in Video Pipe 2. Bit stays high if VS period < ~128ms.	0b0: VS is not detected 0b1: VS is detected
VS_DET_1	1	VS activity is detected in Video Pipe 1. Bit stays high if VS period < ~128ms.	0b0: VS is not detected 0b1: VS is detected
VS_DET_0	0	VS activity is detected in Video Pipe 0. Bit stays high if VS period < ~128ms.	0b0: VS is not detected 0b1: VS is detected

HS_POL (0x11F3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_POL_3	HS_POL_2	HS_POL_1	HS_POL_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
HS_POL_3	3	Detected HS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
HS_POL_2	2	Detected HS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
HS_POL_1	1	Detected HS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
HS_POL_0	0	Detected HS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

VS_POL (0x11F4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VS_POL_3	VS_POL_2	VS_POL_1	VS_POL_0
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
VS_POL_3	3	Detected VS polarity in Video Pipe 3	0b0: Active low 0b1: Active high
VS_POL_2	2	Detected VS polarity in Video Pipe 2	0b0: Active low 0b1: Active high
VS_POL_1	1	Detected VS polarity in Video Pipe 1	0b0: Active low 0b1: Active high
VS_POL_0	0	Detected VS polarity in Video Pipe 0	0b0: Active low 0b1: Active high

HVD_CNT_CTRL (0x11F9)

BIT	7	6	5	4	3	2	1	0
Field	HVD_CNT_RST_3	HVD_CNT_RST_2	HVD_CNT_RST_1	HVD_CNT_RST_0	HVD_CNT_EN_3	HVD_CNT_EN_2	HVD_CNT_EN_1	HVD_CNT_EN_0
Reset	0x0	0x0	0x0	0x0	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HVD_CNT_RST_3	7	Reset counter values.	0x0 0x1: Reset counter values
HVD_CNT_RST_2	6	Reset counter values.	0x0 0x1: Reset counter values
HVD_CNT_RST_1	5	Reset counter values.	0x0 0x1: Reset counter values
HVD_CNT_RST_0	4	Reset counter values.	0x0 0x1: Reset counter values
HVD_CNT_EN_3	3	Enable VS and frames per line counters.	0x0: Disable 0x1: Enable
HVD_CNT_EN_2	2	Enable VS and frames per line counters.	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
HVD_CNT_EN_1	1	Enable VS and frames per line counters.	0x0: Disable 0x1: Enable
HVD_CNT_EN_0	0	Enable VS and frames per line counters.	0x0: Disable 0x1: Enable

HVD_CNT_OS (0x11FA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HVD_CNT_OS_EN_3	HVD_CNT_OS_EN_2	HVD_CNT_OS_EN_1	HVD_CNT_OS_EN_0
Reset	–	–	–	–	0x0	0x0	0x0	0x0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
HVD_CNT_OS_EN_3	3	Enable VS and frames per line counters in one-shot mode. Must be used when HVD_CNT_EN is disabled.	0x0: Disable 0x1: Enable
HVD_CNT_OS_EN_2	2	Enable VS and frames per line counters in one-shot mode. Must be used when HVD_CNT_EN is disabled.	0x0: Disable 0x1: Enable
HVD_CNT_OS_EN_1	1	Enable VS and frames per line counters in one-shot mode. Must be used when HVD_CNT_EN is disabled.	0x0: Disable 0x1: Enable
HVD_CNT_OS_EN_0	0	Enable VS and frames per line counters in one-shot mode. Must be used when HVD_CNT_EN is disabled.	0x0: Disable 0x1: Enable

VS_CNT_WNDW_0_MSB (0x1200)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VS_CNT_WINDOW_0_MSB[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_0_MSB	1:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023s. Default set at 1s.

VS_CNT_WNDW_0_LSB (0x1201)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_WINDOW_0_LSB[7:0]							
Reset	0xE8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_0_LSB	7:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023ms. Default set at 1ms.

VS_CNT_0_CMP (0x1202)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_0_CMP[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VS_CNT_0_CMP	5:0	Compare register for VS count value. When this register is non-zero, the counted value in VS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the VS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_0_CMP_MSB (0x1203)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_0_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
HS_CNT_0_CMP_MSB	3:0	Upper 4-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_0_CMP_LSB (0x1204)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HS_CNT_0_CMP_LSB	7:0	Lower 8-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_0_CMP_MSB (0x1205)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_0_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DE_CNT_0_CMP_MSB	3:0	Upper 4-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_0_CMP_LSB (0x1206)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DE_CNT_0_CMP_LSB	7:0	Lower 8-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

VS_CNT_0 (0x1207)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_0[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
VS_CNT_0	5:0	VS counts within window specificed in VS_CNT_WINDOW registers.

HS_CNT_0_MSB (0x1208)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_0_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
HS_CNT_0_MSB	3:0	Lines per frame HS counter.

HS_CNT_0_LSB (0x1209)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_0_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HS_CNT_0_LSB	7:0	Lines per frame HS counter.

DE_CNT_0_MSB (0x120A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_0_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
DE_CNT_0_MSB	3:0	Lines per frame DE counter.

DE_CNT_0_LSB (0x120B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_0_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DE_CNT_0_LSB	7:0	Lines per frame DE counter.

VRX_0_CMP_ERR_OEN (0x120C)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_0_CMP_ERR_OEN	HS_CNT_0_CMP_ERR_OEN	DE_CNT_0_CMP_ERR_OEN	–	–	–	–	–
Reset	0x1	0x1	0x1	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_0_CMP_ERR_OEN	7	VS count comparison error flag output enable. Refer to VS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
HS_CNT_0_CMP_ERR_OEN	6	HS count comparison error flag output enable. Refer to HS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin

BITFIELD	BITS	DESCRIPTION	DECODE
DE_CNT_0_CMP_ERR_OEN	5	DE count comparison error flag output enable. Refer to DE_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin

VRX_0_CMP_ERR_FLAG (0x120D)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_0_CMP_ERR_FLAG	HS_CNT_0_CMP_ERR_FLAG	DE_CNT_0_CMP_ERR_FLAG	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Read Only	Read Only	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_0_CMP_ERR_FLAG	7	VS count comparison error flag. Refer to VS_CNT_x_CMP register.	0x0: No VS count error detected 0x1: VS count error detected
HS_CNT_0_CMP_ERR_FLAG	6	HS count comparison error flag. Refer to HS_CNT_x_CMP register.	0x0: No HS count error detected 0x1: HS count error detected
DE_CNT_0_CMP_ERR_FLAG	5	DE count comparison error flag. Refer to DE_CNT_x_CMP register.	0x0: No DE count error detected 0x1: DE count error detected

VS_CNT_WNDW_1_MSB (0x1210)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VS_CNT_WINDOW_1_MSB[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_1_MSB	1:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023s. Default set at 1s.

VS_CNT_WNDW_1_LSB (0x1211)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_WINDOW_1_LSB[7:0]							
Reset	0xE8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_1_LSB	7:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023ms. Default set at 1ms.

VS_CNT_1_CMP (0x1212)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_1_CMP[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VS_CNT_1_CMP	5:0	Compare register for VS count value. When this register is non-zero, the counted value in VS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the VS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_1_CMP_MSB (0x1213)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_1_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
HS_CNT_1_CMP_MSB	3:0	Upper 4-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_1_CMP_LSB (0x1214)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HS_CNT_1_CMP_LSB	7:0	Lower 8-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_1_CMP_MSB (0x1215)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_1_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DE_CNT_1_CMP_MSB	3:0	Upper 4-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_1_CMP_LSB (0x1216)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DE_CNT_1_CMP_LSB	7:0	Lower 8-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

VS_CNT_1 (0x1217)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_1[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
VS_CNT_1	5:0	VS counts within window specified in VS_CNT_WINDOW registers.

HS_CNT_1_MSB (0x1218)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_1_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
HS_CNT_1_MSB	3:0	Lines per frame HS counter.

HS_CNT_1_LSB (0x1219)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_1_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HS_CNT_1_LSB	7:0	Lines per frame HS counter.

DE_CNT_1_MSB (0x121A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_1_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
DE_CNT_1_MSB	3:0	Lines per frame DE counter.

DE_CNT_1_LSB (0x121B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_1_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DE_CNT_1_LSB	7:0	Lines per frame DE counter.

VRX_1_CMP_ERR_OEN (0x121C)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_1_CMP_ERR_OEN	HS_CNT_1_CMP_ERR_OEN	DE_CNT_1_CMP_ERR_OEN	–	–	–	–	–
Reset	0x1	0x1	0x1	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_1_CMP_ERR_OEN	7	VS count comparison error flag output enable. Refer to VS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
HS_CNT_1_CMP_ERR_OEN	6	HS count comparison error flag output enable. Refer to HS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
DE_CNT_1_CMP_ERR_OEN	5	DE count comparison error flag output enable. Refer to DE_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin

VRX_1_CMP_ERR_FLAG (0x121D)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_1_CMP_ERR_FLAG	HS_CNT_1_CMP_ERR_FLAG	DE_CNT_1_CMP_ERR_FLAG	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Read Only	Read Only	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_1_CMP_ERR_FLAG	7	VS count comparison error flag. Refer to VS_CNT_x_CMP register.	0x0: No VS count error detected 0x1: VS count error detected
HS_CNT_1_CMP_ERR_FLAG	6	HS count comparison error flag. Refer to HS_CNT_x_CMP register.	0x0: No HS count error detected 0x1: HS count error detected
DE_CNT_1_CMP_ERR_FLAG	5	DE count comparison error flag. Refer to DE_CNT_x_CMP register.	0x0: No DE count error detected 0x1: DE count error detected

VS_CNT_WNDW_2_MSB (0x1220)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VS_CNT_WINDOW_2_MSB[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_2_MSB	1:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023s. Default set at 1s.

VS_CNT_WNDW_2_LSB (0x1221)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_WINDOW_2_LSB[7:0]							
Reset	0xE8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_2_LSB	7:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023ms. Default set at 1ms.

VS_CNT_2_CMP (0x1222)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_2_CMP[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VS_CNT_2_CMP	5:0	Compare register for VS count value. When this register is non-zero, the counted value in VS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the VS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_2_CMP_MSB (0x1223)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_2_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
HS_CNT_2_CMP_MSB	3:0	Upper 4-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_2_CMP_LSB (0x1224)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_2_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HS_CNT_2_CMP_LSB	7:0	Lower 8-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_2_CMP_MSB (0x1225)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_2_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DE_CNT_2_CMP_MSB	3:0	Upper 4-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_2_CMP_LSB (0x1226)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_2_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DE_CNT_2_CMP_LSB	7:0	Lower 8-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

VS_CNT_2 (0x1227)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_2[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
VS_CNT_2	5:0	VS counts within window specified in VS_CNT_WINDOW registers.

HS_CNT_2_MSB (0x1228)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_2_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
HS_CNT_2_MSB	3:0	Lines per frame HS counter.

HS_CNT_2_LSB (0x1229)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_2_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HS_CNT_2_LSB	7:0	Lines per frame HS counter.

DE_CNT_2_MSB (0x122A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_2_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
DE_CNT_2_MSB	3:0	Lines per frame DE counter.

DE_CNT_2_LSB (0x122B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_2_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DE_CNT_2_LSB	7:0	Lines per frame DE counter.

VRX_2_CMP_ERR_OEN (0x122C)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_2_CMP_ERR_OEN	HS_CNT_2_CMP_ERR_OEN	DE_CNT_2_CMP_ERR_OEN	–	–	–	–	–
Reset	0x1	0x1	0x1	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_2_CMP_ERR_OEN	7	VS count comparison error flag output enable. Refer to VS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
HS_CNT_2_CMP_ERR_OEN	6	HS count comparison error flag output enable. Refer to HS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
DE_CNT_2_CMP_ERR_OEN	5	DE count comparison error flag output enable. Refer to DE_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin

VRX_2_CMP_ERR_FLAG (0x122D)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_2_CMP_ERR_FLAG	HS_CNT_2_CMP_ERR_FLAG	DE_CNT_2_CMP_ERR_FLAG	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Read Only	Read Only	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_2_CMP_ERR_FLAG	7	VS count comparison error flag. Refer to VS_CNT_x_CMP register.	0x0: No VS count error detected 0x1: VS count error detected
HS_CNT_2_CMP_ERR_FLAG	6	HS count comparison error flag. Refer to HS_CNT_x_CMP register.	0x0: No HS count error detected 0x1: HS count error detected
DE_CNT_2_CMP_ERR_FLAG	5	DE count comparison error flag. Refer to DE_CNT_x_CMP register.	0x0: No DE count error detected 0x1: DE count error detected

VS_CNT_WNDW_3_MSB (0x1230)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VS_CNT_WINDOW_3_MSB[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_3_MSB	1:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023s. Default set at 1ms.

VS_CNT_WNDW_3_LSB (0x1231)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_WINDOW_3_LSB[7:0]							
Reset	0xE8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
VS_CNT_WINDOW_3_LSB	7:0	VS counter counts number of frames within window specified in this register in milliseconds. Max window at 1.023ms. Default set at 1s.

VS_CNT_3_CMP (0x1232)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_3_CMP[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
VS_CNT_3_CMP	5:0	Compare register for VS count value. When this register is non-zero, the counted value in VS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the VS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_3_CMP_MSB (0x1233)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_3_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
HS_CNT_3_CMP_MSB	3:0	Upper 4-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

HS_CNT_3_CMP_LSB (0x1234)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_3_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
HS_CNT_3_CMP_LSB	7:0	Lower 8-bits of compare register for HS count value. When this register is non-zero, the counted value in HS_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the HS_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_3_CMP_MSB (0x1235)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_3_CMP_MSB[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
DE_CNT_3_CMP_MSB	3:0	Upper 4-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

DE_CNT_3_CMP_LSB (0x1236)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_3_CMP_LSB[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DE_CNT_3_CMP_LSB	7:0	Lower 8-bits of compare register for DE count value. When this register is non-zero, the counted value in DE_CNT_x is checked against the value in this register. If the two values are not within +/- 2, the DE_CNT_x_CMP_ERR flag will get set. When this register is 0, the compare feature is disabled.

VS_CNT_3 (0x1237)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VS_CNT_3[5:0]					
Reset	–	–						
Access Type	–	–	Read Only					

BITFIELD	BITS	DESCRIPTION
VS_CNT_3	5:0	VS counts within window specified in VS_CNT_WINDOW registers.

HS_CNT_3_MSB (0x1238)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	HS_CNT_3_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
HS_CNT_3_MSB	3:0	Lines per frame HS counter.

HS_CNT_3_LSB (0x1239)

BIT	7	6	5	4	3	2	1	0
Field	HS_CNT_3_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
HS_CNT_3_LSB	7:0	Lines per frame HS counter.

DE_CNT_3_MSB (0x123A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DE_CNT_3_MSB[3:0]			
Reset	–	–	–	–				
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
DE_CNT_3_MSB	3:0	Lines per frame DE counter.

DE_CNT_3_LSB (0x123B)

BIT	7	6	5	4	3	2	1	0
Field	DE_CNT_3_LSB[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DE_CNT_3_LSB	7:0	Lines per frame DE counter.

VRX_3_CMP_ERR_OEN (0x123C)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_3_CMP_ERR_OEN	HS_CNT_3_CMP_ERR_OEN	DE_CNT_3_CMP_ERR_OEN	–	–	–	–	–
Reset	0x1	0x1	0x1	–	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_3_CMP_ERR_OEN	7	VS count comparison error flag output enable. Refer to VS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
HS_CNT_3_CMP_ERR_OEN	6	HS count comparison error flag output enable. Refer to HS_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin
DE_CNT_3_CMP_ERR_OEN	5	DE count comparison error flag output enable. Refer to DE_CNT_x_CMP register.	0x0: Disable reporting of error to ERRB pin 0x1: Enable reporting of error to ERRB pin

VRX_3_CMP_ERR_FLAG (0x123D)

BIT	7	6	5	4	3	2	1	0
Field	VS_CNT_3_CMP_ERR_FLAG	HS_CNT_3_CMP_ERR_FLAG	DE_CNT_3_CMP_ERR_FLAG	–	–	–	–	–
Reset	0x0	0x0	0x0	–	–	–	–	–
Access Type	Read Only	Read Only	Read Only	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
VS_CNT_3_CMP_ERR_FLAG	7	VS count comparison error flag. Refer to VS_CNT_x_CMP register.	0x0: No VS count error detected 0x1: VS count error detected
HS_CNT_3_CMP_ERR_FLAG	6	HS count comparison error flag. Refer to HS_CNT_x_CMP register.	0x0: No HS count error detected 0x1: HS count error detected
DE_CNT_3_CMP_ERR_FLAG	5	DE count comparison error flag. Refer to DE_CNT_x_CMP register.	0x0: No DE count error detected 0x1: DE count error detected

TUN_MODE_DET (0x1260)

BIT	7	6	5	4	3	2	1	0
Field	CPHY_MODE_OVRD_EN	–	–	–	BACKTOP4_TUN_DET	BACKTOP3_TUN_DET	BACKTOP2_TUN_DET	BACKTOP1_TUN_DET
Reset	0x0	–	–	–				
Access Type	Write, Read	–	–	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CPHY_MODE_OVRD_EN	7	Each backtop use values set in BACKTOPx_CPHY_MODE_OVRD register instead of detected (BACKTOPx_CPHY_MODE_DET). Used only in Wx4H aggregation in tunneling mode.	0x0: Controller 0 0x1: Controller 1
BACKTOP4_TUN_DET	3	Detected tunneling mode flag	0x0: Tunnel Mode not detected 0x1: Tunnel Mode detected
BACKTOP3_TUN_DET	2	Detected tunneling mode flag	0x0: Tunnel Mode not detected 0x1: Tunnel Mode detected
BACKTOP2_TUN_DET	1	Detected tunneling mode flag	0x0: Tunnel Mode not detected 0x1: Tunnel Mode detected
BACKTOP1_TUN_DET	0	Detected tunneling mode flag	0x0: Tunnel Mode not detected 0x1: Tunnel Mode detected

TUN_CPHY_DET (0x1261)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP4_CPHY_MODE_OVRD	BACKTOP3_CPHY_MODE_OVRD	BACKTOP2_CPHY_MODE_OVRD	BACKTOP1_CPHY_MODE_OVRD	BACKTOP4_CPHY_MODE_DET	BACKTOP3_CPHY_MODE_DET	BACKTOP2_CPHY_MODE_DET	BACKTOP1_CPHY_MODE_DET
Reset	0x1	0x1	0x1	0x1				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP4_CPHY_MODE_OVRD	7	Must also set CPHY_MODE_OVRD register to 1. BACKTOP4 cphy_mode override value (used only in Wx4H aggregation and DPHY-to-CPHY conversion in tunneling mode).	0x0: Controller 0 0x1: Controller 1
BACKTOP3_CPHY_MODE_OVRD	6	Must also set CPHY_MODE_OVRD register to 1. BACKTOP3 cphy_mode override value (used only in Wx4H aggregation and DPHY-to-CPHY conversion in tunneling mode).	0x0: Controller 0 0x1: Controller 1
BACKTOP2_CPHY_MODE_OVRD	5	Must also set CPHY_MODE_OVRD register to 1. BACKTOP2 cphy_mode override value (used only in Wx4H aggregation and DPHY-to-CPHY conversion in tunneling mode).	0x0: Controller 0 0x1: Controller 1
BACKTOP1_CPHY_MODE_OVRD	4	Must also set CPHY_MODE_OVRD register to 1. BACKTOP1 cphy_mode override value (used only in Wx4H aggregation and DPHY-to-CPHY conversion in tunneling mode).	0x0: Controller 0 0x1: Controller 1
BACKTOP4_CPHY_MODE_DET	3	Detected CPHY mode header/packets from SER in tunneling mode (used for Wx4H aggregation and setting DPHY-to-CPHY conversion mode in tunneling mode)	0x0: CPHY Tunnel Mode not Detected 0x1: CPHY Tunnel Mode Detected
BACKTOP3_CPHY_MODE_DET	2	Detected CPHY mode header/packets from SER in tunneling mode (used for Wx4H aggregation and setting DPHY-to-CPHY conversion mode in tunneling mode)	0x0: CPHY Tunnel Mode not Detected 0x1: CPHY Tunnel Mode Detected
BACKTOP2_CPHY_MODE_DET	1	Detected CPHY mode header/packets from SER in tunneling mode (used for Wx4H aggregation and setting DPHY-to-CPHY conversion mode in tunneling mode)	0x0: CPHY Tunnel Mode not Detected 0x1: CPHY Tunnel Mode Detected
BACKTOP1_CPHY_MODE_DET	0	Detected CPHY mode header/packets from SER in tunneling mode (used for Wx4H aggregation and setting DPHY-to-CPHY conversion mode in tunneling mode)	0x0: CPHY Tunnel Mode not Detected 0x1: CPHY Tunnel Mode Detected

TUN_CPHY_LANE_DET (0x1262)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP4_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP3_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP2_TUN_CPHY_SER_LANE_DET[1:0]		BACKTOP1_TUN_CPHY_SER_LANE_DET[1:0]	
Reset								
Access Type	Read Only		Read Only		Read Only		Read Only	

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP4_TUN_CPHY_SER_LANE_DET	7:6	Detected number of CPHY lanes in SER	0x0: 1-lane 0x1: 2-lanes
BACKTOP3_TUN_CPHY_SER_LANE_DET	5:4	Detected number of CPHY lanes in SER	0x0: 1-lane 0x1: 2-lanes
BACKTOP2_TUN_CPHY_SER_LANE_DET	3:2	Detected number of CPHY lanes in SER	0x0: 1-lane 0x1: 2-lanes
BACKTOP1_TUN_CPHY_SER_LANE_DET	1:0	Detected number of CPHY lanes in SER	0x0: 1-lane 0x1: 2-lanes

TMD_HEADER_ERR_FLAGS_1 (0x1264)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP1_TMD_SP_DET_ERR	–	BACKTOP1_TMD_CRC_2L_ERR_FLAG	BACKTOP1_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP1_TMD_ECC_ERR_FLAG	BACKTOP1_TMD_ECC_FLAG
Reset		–			–	–		
Access Type	Read Only	–	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP1_TMD_SP_DET_ERR	7	Detected header error in short-packet detect state. Short packet header after detected three consecutive matching headers did not match in mode (DPHY/CPHY 1-lane/CPHY 2-lane). This error will also reset the tmd_pkt_cnt in the same backtop.	0x0: No error detected 0x1: Detected Header Error
BACKTOP1_TMD_CRC_2L_ERR_FLAG	5	2-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP1_TMD_CRC_1L_ERR_FLAG	4	1-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP1_TMD_ECC_ERR_FLAG	1	DPHY mode uncorrectable ECC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP1_TMD_ECC_FLAG	0	DPHY mode ECC error (1-bit correctable) detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error

TMD_HEADER_ERR_FLAGS_2 (0x1265)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP2_TMD_SP_DET_ERR	–	BACKTOP2_TMD_CRC_2L_ERR_FLAG	BACKTOP2_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP2_TMD_ECC_ERR_FLAG	BACKTOP2_TMD_ECC_FLAG
Reset		–			–	–		
Access Type	Read Only	–	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP2_TMD_SP_DET_ERR	7	Detected header error in short-packet detect state. Short packet header after detected 3-consecutive matching headers did not match in mode (DPHY/CPHY 1-lane/CPHY 2-lane). This error will also reset the tmd_pkt_cnt in the same backtop.	0x0: No error detected 0x1: Detected Header Error
BACKTOP2_TMD_CRC_2L_ERR_FLAG	5	2-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP2_TMD_CRC_1L_ERR_FLAG	4	1-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP2_TMD_ECC_ERR_FLAG	1	DPHY mode uncorrectable ECC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP2_TMD_ECC_FLAG	0	DPHY mode ECC error (1-bit correctable) detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error

TMD_HEADER_ERR_FLAGS_3 (0x1266)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP3_TMD_SP_DET_ERR	–	BACKTOP3_TMD_CRC_2L_ERR_FLAG	BACKTOP3_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP3_TMD_ECC_ERR_FLAG	BACKTOP3_TMD_ECC_FLAG
Reset		–			–	–		
Access Type	Read Only	–	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP3_TMD_SP_DET_ERR	7	Detected header error in short-packet detect state. Short packet header after detected 3-consecutive matching headers did not match in mode (DPHY/CPHY 1-lane/CPHY 2-lane). This error will also reset the tmd_pkt_cnt in the same backtop.	0x0: No error detected 0x1: Detected Header Error
BACKTOP3_TMD_CRC_2L_ERR_FLAG	5	2-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP3_TMD_CRC_1L_ERR_FLAG	4	1-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP3_TMD_ECC_ERR_FLAG	1	DPHY mode uncorrectable ECC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP3_TMD_ECC_FLAG	0	DPHY mode ECC error (1-bit correctable) detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error

TMD_HEADER_ERR_FLAGS_4 (0x1267)

BIT	7	6	5	4	3	2	1	0
Field	BACKTOP4_TMD_SP_DET_ERR	–	BACKTOP4_TMD_CRC_2L_ERR_FLAG	BACKTOP4_TMD_CRC_1L_ERR_FLAG	–	–	BACKTOP4_TMD_ECC_ERR_FLAG	BACKTOP4_TMD_ECC_FLAG
Reset		–			–	–		
Access Type	Read Only	–	Read Only	Read Only	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP4_TMD_SP_DET_ERR	7	Detected header error in short-packet detect state. Short packet header after detected 3-consecutive matching headers did not match in mode (DPHY/CPHY 1-lane/CPHY 2-lane). This error will also reset the tmd_pkt_cnt in the same backtop.	0x0: No error detected 0x1: Detected Header Error

BITFIELD	BITS	DESCRIPTION	DECODE
BACKTOP4_TMD_CRC_2L_ERR_FLAG	5	2-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP4_TMD_CRC_1L_ERR_FLAG	4	1-lane CPHY mode CRC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP4_TMD_ECC_ERR_FLAG	1	DPHY mode uncorrectable ECC error detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error
BACKTOP4_TMD_ECC_FLAG	0	DPHY mode ECC error (1-bit correctable) detected. This flag is sticky and will update when header is enabled (i.e. during tunnel mode detection OR Wx4H aggregation)	0x0: No error detected 0x1: Detected Error

TMD_PKT_CNT_1 (0x126A)

BIT	7	6	5	4	3	2	1	0
Field	TMD_PKT_CNT_1[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_1	7:0	Number of packets used to determine tunnel/pixel mode in BACKTOP1

TMD_PKT_CNT_2 (0x126B)

BIT	7	6	5	4	3	2	1	0
Field	TMD_PKT_CNT_2[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_2	7:0	Number of packets used to determine tunnel/pixel mode in BACKTOP2

TMD_PKT_CNT_3 (0x126C)

BIT	7	6	5	4	3	2	1	0
Field	TMD_PKT_CNT_3[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_3	7:0	Number of packets used to determine tunnel/pixel mode in BACKTOP3

TMD_PKT_CNT_4 (0x126D)

BIT	7	6	5	4	3	2	1	0
Field	TMD_PKT_CNT_4[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_4	7:0	Number of packets used to determine tunnel/pixel mode in BACKTOP4

TMD_PKT_CNT_1_H (0x126E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TMD_PKT_CNT_1_H[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_1_H	4:0	Number of packets used to determine tunnel/pixel mode in BACKTOP1

TMD_PKT_CNT_2_H (0x126F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TMD_PKT_CNT_2_H[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_2_H	4:0	Number of packets used to determine tunnel/pixel mode in BACKTOP2

TMD_PKT_CNT_3_H (0x1270)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TMD_PKT_CNT_3_H[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_3_H	4:0	Number of packets used to determine tunnel/pixel mode in BACKTOP3

TMD_PKT_CNT_4_H (0x1271)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TMD_PKT_CNT_4_H[4:0]				
Reset	–	–	–					
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
TMD_PKT_CNT_4_H	4:0	Number of packets used to determine tunnel/pixel mode in BACKTOP4

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/22	Initial Release	—
1	7/22	Corrected typos in Table 9. MFP Pin Function Map	41
2	9/22	General description and Simplified Block Diagram updated.	1-2
3	10/22	Removed asterisks from future products in the Ordering Information table.	46
4	1/23	Changed the verbiage in the tunneling and pixel mode sections and adjusted the pictures.	34

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