TS3USB3031 2-Channel, 1:3, USB 2.0 High-Speed (480 Mbps) and Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) Switch

1 Features

- V_{CC} Range: 2.5 V to 4.3 V
- Mobile High-definition Link (MHL) or Mobility Display Port (MyDP) Switch:
  - Bandwidth (–3 dB): 6.5 GHz
  - R_{ON} (Typical): 5.5 Ω
  - C_{ON} (Typical): 1.3 pF
- USB Switches (2 Sets):
  - Bandwidth (–3 dB): 6.5 GHz
  - R_{ON} (Typical): 4.5 Ω
  - C_{ON} (Typical): 1 pF
- Current Consumption: 28 µA (Typical)
- Special Features:
  - I_{OFF} Protection Prevents Current Leakage in Powered-Down State (V_{CC} = 0 V)
  - 1.8-V Compatible Control Inputs (SEL)
  - Overvoltage Tolerance (OVT) on All I/O Pins up to 5.5 V Without External Components
- ESD Performance:
  - 2-kV Human-Body Model (A114B, Class II)
  - 1-kV Charged-Device Model (C101)
- Package:
  - 12-Pin VQFN Package (1.8-mm × 1.8-mm, 0.5-mm Pitch)

2 Applications

- Smart Phones, Tablets, Mobile Phones
- Portable Instrumentation
- Digital Cameras USB 2.0 MHL

3 Description

The TS3USB3031 device is a 2-channel, 1:3 multiplexer that includes a high-speed Mobile High-Definition Link (MHL), Mobility Display Port (MyDP) switch, and USB 2.0 High-Speed (480 Mbps) switches in the same package. These configurations allow the system designer to save board space and eliminate multiple connectors buy using a common USB or Mico-USB connector for MHL/MyDP signals and two sets of USB data. The MHL/MyDP path supports the latest MHL Rev. 3.0 specification.

The TS3USB3031 has a V_{CC} range of 2.5 V to 4.3 V and supports overvoltage tolerance (OVT) feature, which allows the I/O pins to withstand overvoltage conditions (up to 5.5 V). The power-off protection feature forces all I/O pins to be in high impedance mode when power is not present, allowing full isolation of the signals lines under such condition without excessive leakage current. The select pins of TS3USB3031 are compatible with 1.8-V control voltage, allowing them to be directly interfaced with the General Purpose I/O (GPIO) from a mobile processor with out needing additional voltage level shifting circuitry.

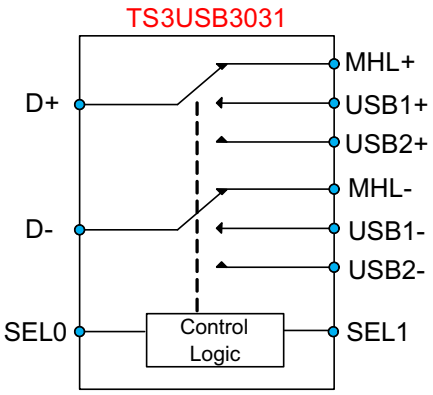
The TS3USB3031 comes with a small 12-pin VQFN package with only 1.8 mm × 1.8 mm in size, which makes it a perfect candidate to be used in mobile applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB3031	VQFN (12)	1.80 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Switch Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2016) to Revision C — **Page**

- Changed Feature From: 1.8-V Compatible Control Inputs (SEL, $\overline{OE}$) To: 1.8-V Compatible Control Inputs (SEL) ... 1
- Changed second pin D+ To: D- in the *Switch Diagram* ... 1
- Changed DIGITAL CONTROL INPUTS (SEL, $\overline{OE}$) To: DIGITAL CONTROL INPUTS (SEL) in the *Electrical Characteristics* table ... 5
- Changed second pin D+ To: D- in the *Functional Block Diagram* ... 10
- Deleted sentence: "The internal pulldown resistor on OE enables the switch when power is applied to VCC" from the *Design Requirements* section ... 12

Changes from Revision A (September 2013) to Revision B — **Page**

- Added *Applications* list, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the datasheet ... 1
- Moved Peak switch DC output current parameter From: *Absolute Maximum Ratings* To: *Recommended Operating Conditions* ... 4

Changes from Original (June 2013) to Revision A — **Page**

- Added TYPICAL CHARACTERISTICS section ... 6

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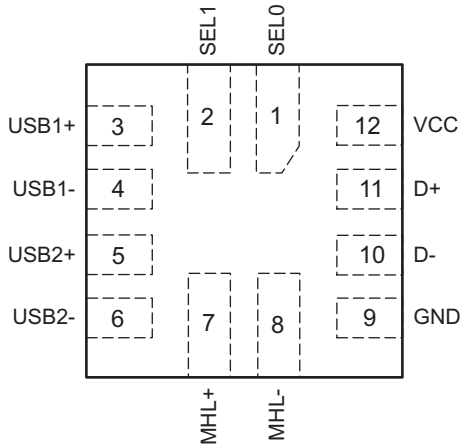
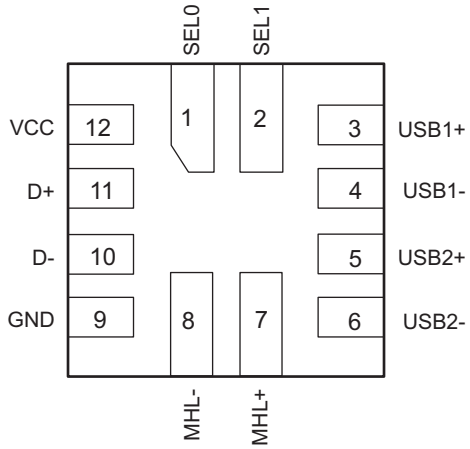
5 Pin Configuration and Functions

RMG Package
12-Pin VQFN
Top View



RMG Package
12-Pin VQFN
Bottom View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SEL0	I	Digital control Input
2	SEL1	I	Digital control Input
3	USB1+	I/O	Differential signal path 1
4	USB1–	I/O	Differential signal path 1
5	USB2+	I/O	Differential signal path 2
6	USB2–	I/O	Differential signal path 2
7	MHL+	I/O	Differential signal path 3
8	MHL–	I/O	Differential signal path 3
9	GND	G	Ground
10	D–	I/O	Common Differential signal path
11	D+	I/O	Common Differential signal path
12	VCC	P	Power Supply

(1) G = Ground, I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(3)	–0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage(3)	–0.3	5.5	V
I_K	Input/Output port diode current (VI/O < 0)	–50		mA
V_I	Digital input voltage (SEL0, SEL1)	–0.3	5.5	
I_{IK}	Digital logic input clamp current (VI < 0)(3)	–50		mA
$I_{I/O}$	Continuous switch DC output current (USB and MHL)		60	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	4.3	V
$V_{I/O\ (USB)}$, $V_{I/O\ (MHL)}$	Analog voltage	0	3.6	V
V_I	Digital input voltage (SEL0, SEL1)	0	V_{CC}	V
$T_{RAMP\ (VCC)}$	Power supply ramp time requirement (VCC)	100	1000	µs/V
$I_{I/O,\ PEAK}$	Peak switch DC output current (1-ms duration pulse at <10% duty cycle)		150	mA
T_A	Operating free-air temperature	–40	85	ºC

6.4 Thermal Information

THERMAL METRIC(1)		TS3USB3031 RMG (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MHL SWITCH						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5V, I_{ON} = –8 mA (see Figure 9)		5.5	7	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 1.5 V to 3.3 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$= 0 V (see Figure 10)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Power off, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$= NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{MHL+/MHL-}$ = 1.5 V to 3.3 V, $V_{D+/D-}$= NC	–2		2	µA
USB SWITCH (USB1 and USB2)						
R_{ON}	ON-state resistance	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA (see Figure 9)		4.5	6	Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.5 V, $V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.5 V, $V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V, Switch OFF, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$= 0 V (see Figure 10)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V, Switch ON or OFF, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$= NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V, Switch ON, $V_{USB+/USB-}$ = 0 V to 0.4 V, $V_{D+/D-}$= NC	–2		2	µA
DIGITAL CONTROL INPUTS (SEL)						
V_{IH}	Input logic high	V_{CC} = 2.5 V to 4.3 V	1.3			V
V_{IL}	Input logic low	V_{CC} = 2.5 V to 4.3 V			0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.3 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = 0 V to 4.3 V	–10		10	µA

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V		50		ps
t_{switch}	Switching time between USB/MHL channels in active modes	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			400	ns
t_{ON}	Switch turnon time (from disabled to active mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
t_{OFF}	Switch turnoff time (from active to disabled mode)	R_L = 50 Ω, CL = 5 pF, V_{CC} = 2.5 V to 4.3 V, $V_{I/O(USB)}$ = 0.4 V, $V_{I/O(MHL)}$ = 3.3 V			100	µs
$C_{ON(MHL)}$	MHL path, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1.3		pF
$C_{ON(USB)}$	USB1 and USB2 paths, ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch ON		1		pF
$C_{OFF(MHL)}$	MHL path, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		1		pF
$C_{OFF(USB)}$	USB1 and USB2 paths, OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 V or 3.3 V, f = 240 MHz, Switch OFF		0.8		pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 V or 2 V		2.2		pF
$O_{ISO\ (MHL)}$	MHL path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see Figure 11), Switch OFF		–38		dB
$O_{ISO\ (USB)}$	USB path, OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V RT = 50 Ω, f = 240 MHz (see Figure 11), Switch OFF		–38		dB
$X_{TALK\ (MHL)}$	MHL channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see Figure 12), Switch ON		–41		dB

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Dynamic Characteristics (continued)

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$X_{TALK\ (USB)}$	USB channel crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V, RT = 50 Ω, f = 240 MHz (see Figure 12), Switch ON		–38		dB
$BW_{(MHL)}$	MHL path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50 Ω (see Figure 13), Switch ON		6.5		GHz
$BW_{(USB)}$	USB path, –3-dB bandwidth	V_{CC} = 2.5 V to 4.3 V, R_L = 50Ω (See Figure 13), Switch ON		6.5		GHz
SUPPLY						
V_{CC}	Power supply voltage		2.5		4.3	V
I_{CC}	Positive supply current	V_{CC} = 4.3 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF		28	40	µA

6.7 Typical Characteristics

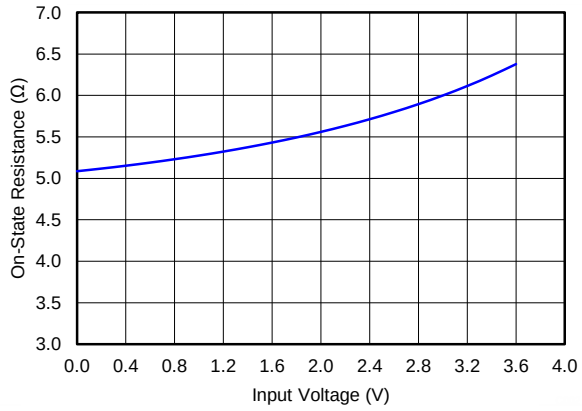

Figure 1. ON-Resistance vs $V_{I/O}$ for MHL Switch

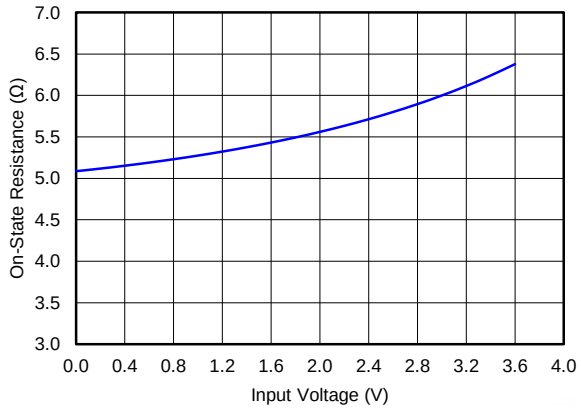

Figure 2. ON-Resistance vs $V_{I/O}$ for USB Switch

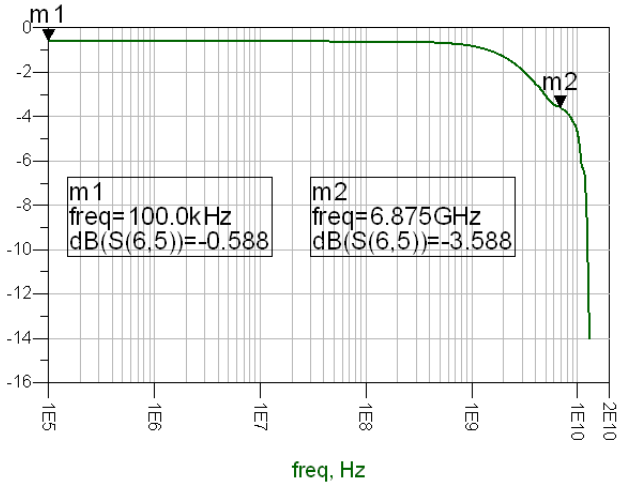

Figure 3. Bandwidth for MHL Switch

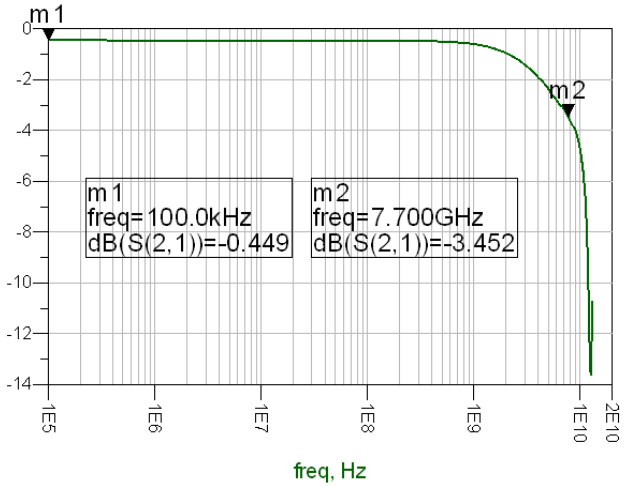

Figure 4. Bandwidth for USB Switch

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Typical Characteristics (continued)

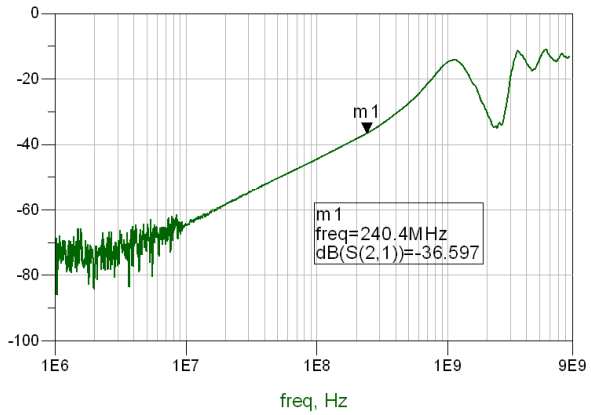

Figure 5. OFF Isolation vs Frequency for MHL Path

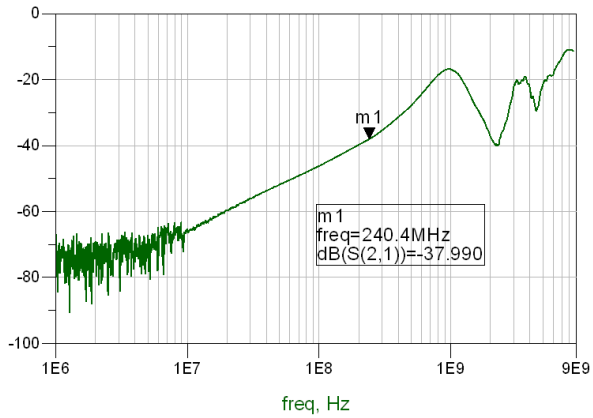

Figure 6. OFF Isolation vs Frequency for USB Path

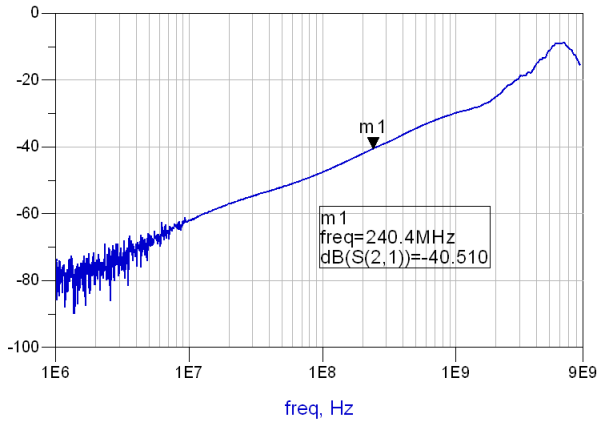

Figure 7. Cross Talk vs Frequency for MHL Path

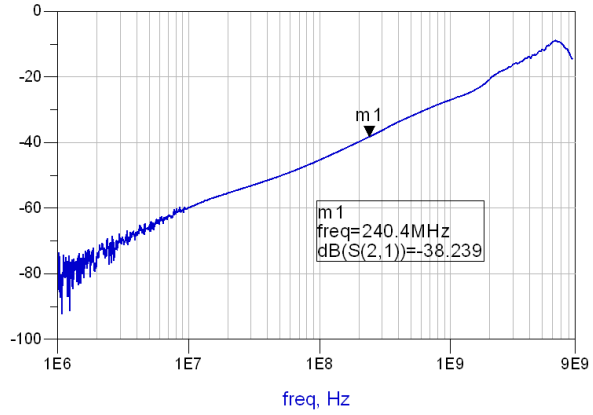

Figure 8. Cross Talk vs Frequency for USB Path

7 Parameter Measurement Information

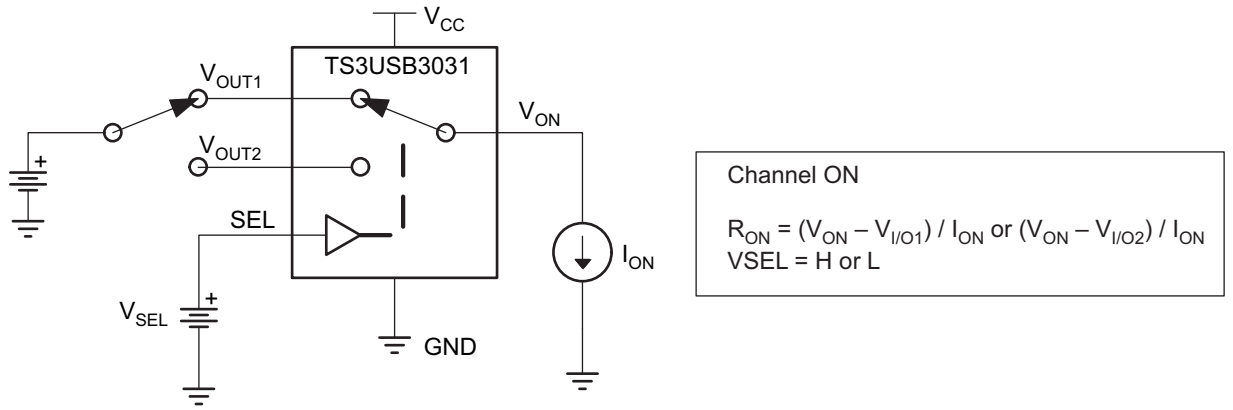

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Figure 9. ON-State Resistance (R_{ON})

Parameter Measurement Information (continued)

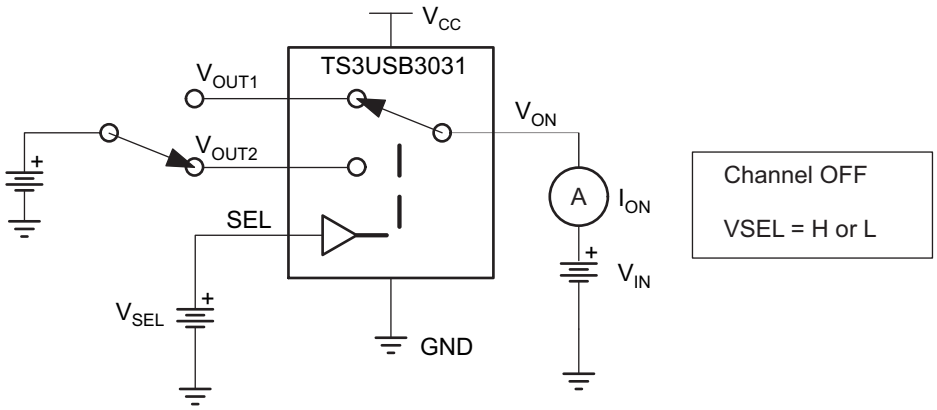

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Figure 10. OFF Leakage Current (I_{OZ})

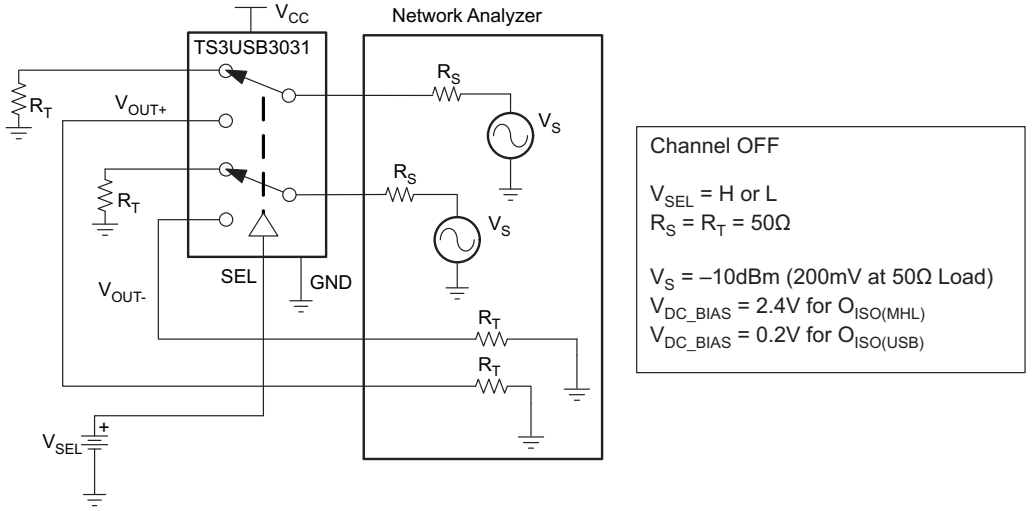

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Figure 11. Differential Off-Isolation (O_{ISO})

Parameter Measurement Information (continued)

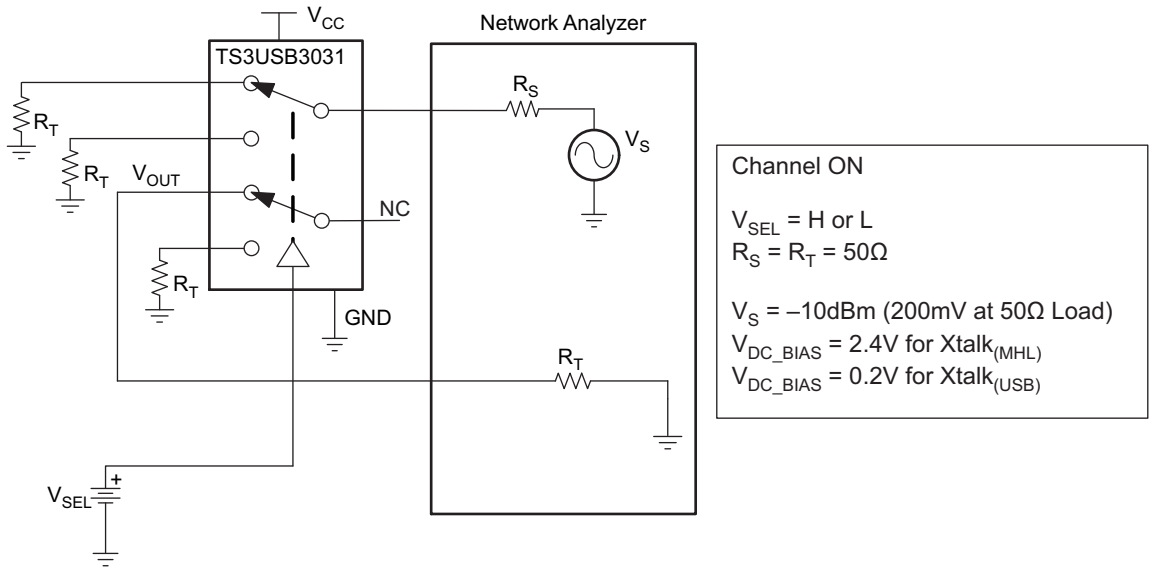

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Figure 12. Crosstalk (Xtalk)

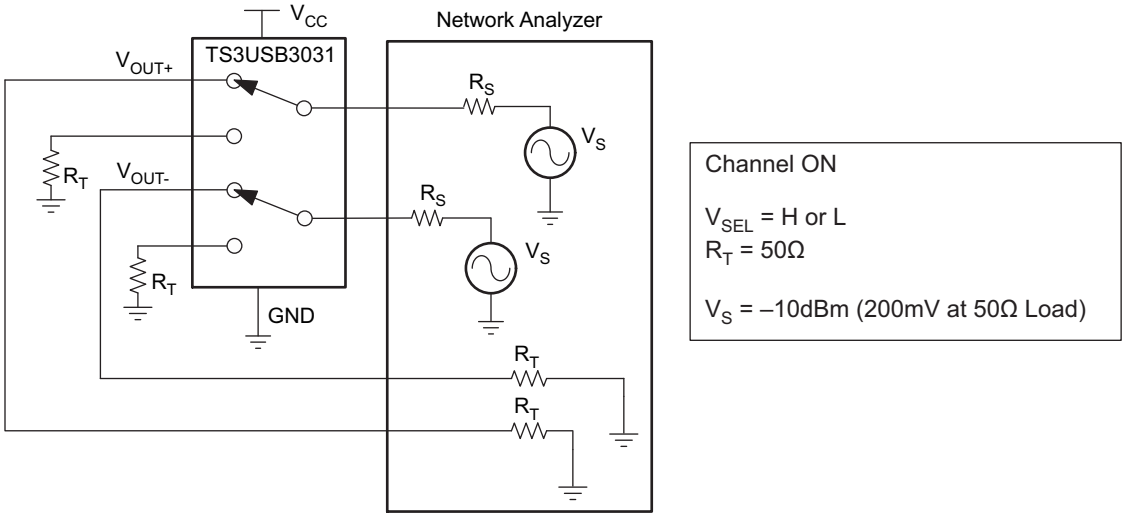

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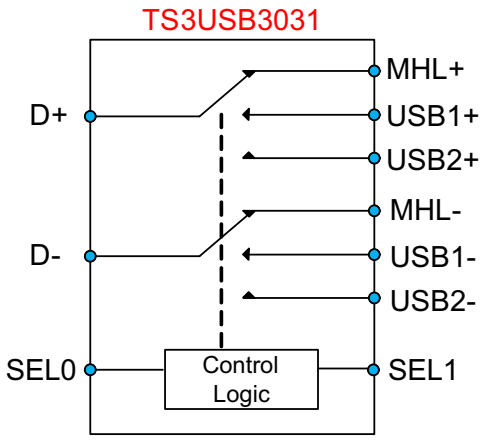
Figure 13. Differential Bandwidth (BW)

8 Detailed Description

8.1 Overview

The TS3USB3031 device is a 2-channel, 1:3 multiplexer that includes a high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switch and USB 2.0 High-Speed (480 Mbps) switches in the same package. This device is used in many high-speed differential 1:3 mux applications.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 I_{OFF} Protection

I_{OFF} protection precents current leakage through the device when V_{cc} = 0 V This allows signals to be present on the D± and USB/MHL± pins before the device is powered up without damaging the device or system.

8.3.2 1.8-V Compatible Logic

The TS3USB3031 device supports 1.8-V logic irrespective to the supply voltage applied to the IC.

8.3.3 Overvoltage Tolerant (OVT)

The D± and USB/MHL± pins of the device can support signals up to 5.5 V without damaging the device. This protects the TS3USB3031 in case the VBUS pin of the USB connector is shorted to the signal path without additional components added.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TS3USB3031.

Table 1. Function Table

SEL1	SEL0	SWITCH STATUS
Low	Low	D+/D– connected to USB1+/USB1–
Low	High	D+/D– connected to USB2+/USB2–
High	Low	D+/D– connected to MHL+/MHL–
High	High	USB and MHL switches in High-Z

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3USB3031 is a passive, bidirectional, 2-channel 1:3 switch which makes it versatile to be used in many high speed 1:3 switching applications. This device was designed originally for USB 2.0 and Mobile High-Definition Link applications but can be used for general signal switching applications such as I^2C, UART, LVDS, and so forth.

9.2 Typical Application

Figure 14 represents a typical application of the TS3USB3031 MHL switch. The TS3USB3031 is used to switch signals between the 2 sets of USB paths, which go to either the baseband or application processor, and the MHL path, which goes to the HDMI to MHL bridge. The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default. The TS5A3157 is a separate SPDT switch that is used to switch between MHL's CBUS and the USB ID line that is required for USB OTG (USB On-The-Go) application.

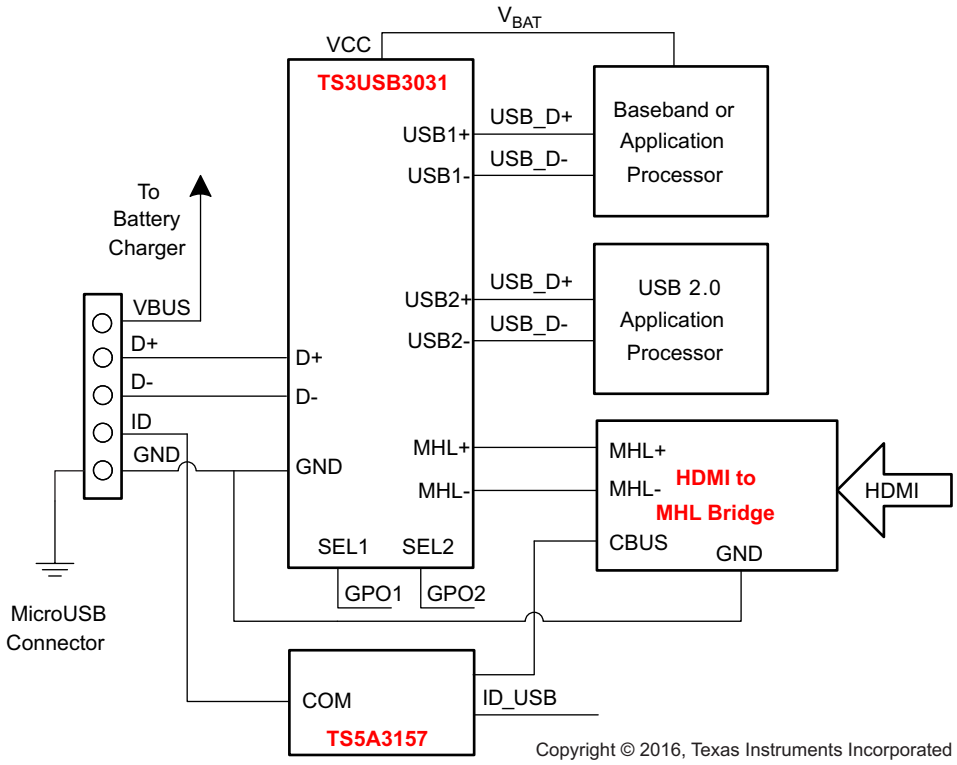

Figure 14. Typical TS3USB3031 Application

Typical Application (continued)

9.2.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed.

The TS3USB3031 has internal 6-MΩ pulldown resistors on SEL0 and SEL1 so no external resistors are required on the logic pins. The pulldown on SEL0 and SEL1 ensure the USB1 channel is selected by default.

The TS5A3157 is a separate SPDT switch that is used to switch between the CBUS of the MHL and the USB ID line that is required for USB OTG (USB On-The-Go) application.

9.2.2 Detailed Design Procedure

The TS3USB3031 can be properly operated without any external components. However, TI recommends that unused signal I/O pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

9.2.3 Application Curves

9.2.3.1 MHL Eye Pattern

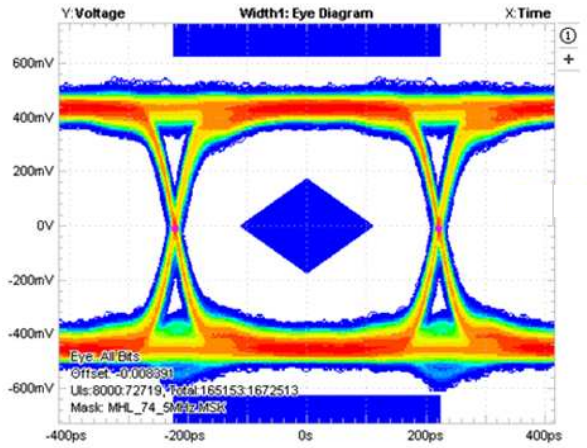

Figure 15. Eye Pattern Error Histogram: 2.25 Gbps With No Device

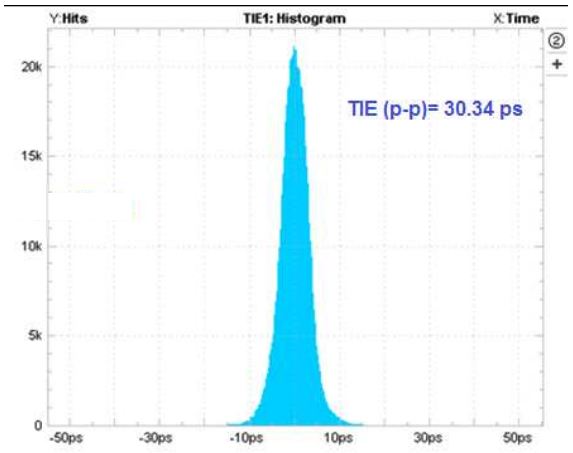

Figure 16. Time Interval Error Histogram: 2.25 Gbps With No Device

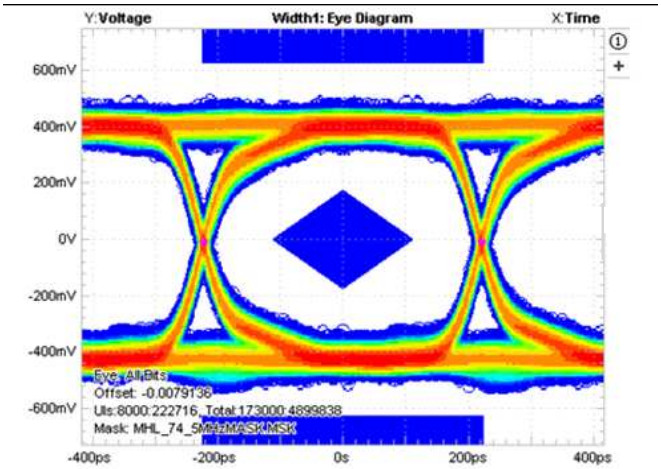

Figure 17. Eye Pattern Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

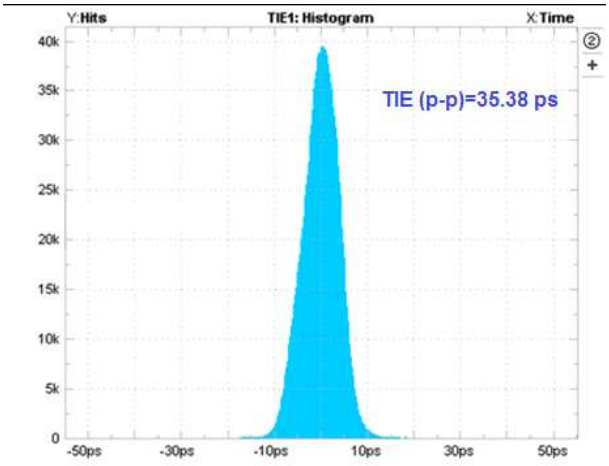

Figure 18. Time Interval Error Histogram: 2.25 Gbps With TS3USB3031 (Added Jitter = 5.04 ps)

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Typical Application (continued)

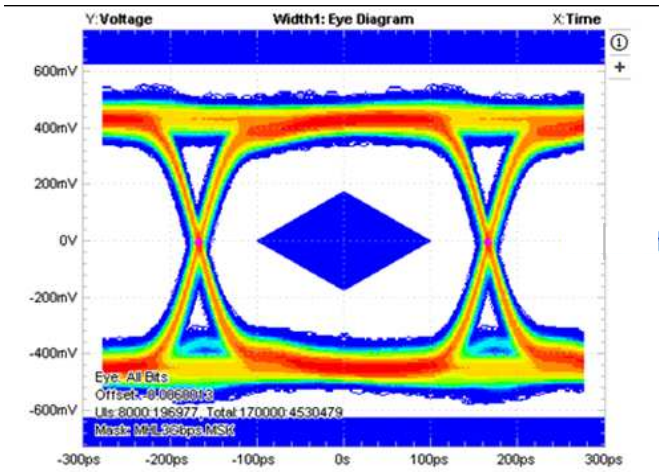

Figure 19. Eye Pattern Error Histogram: 3.0 Gbps With No Device

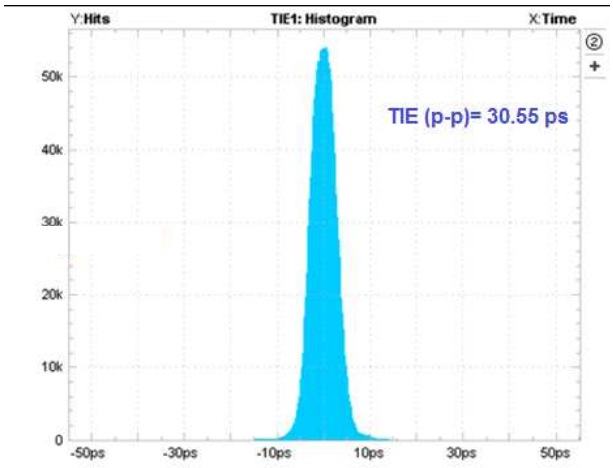

Figure 20. Time Interval Error Histogram: 3.0 Gbps With No Device

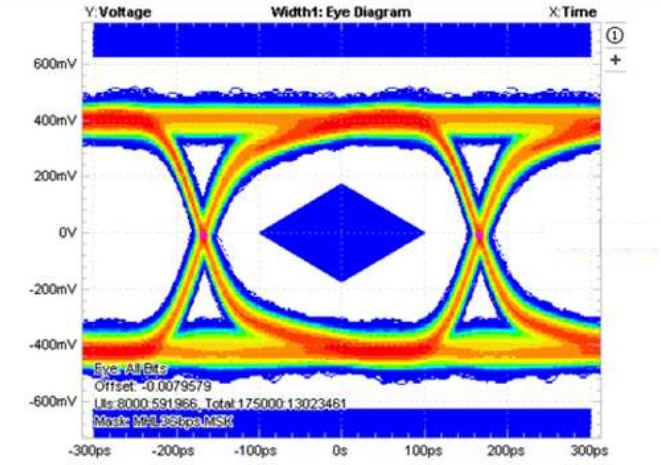

Figure 21. Eye Pattern Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

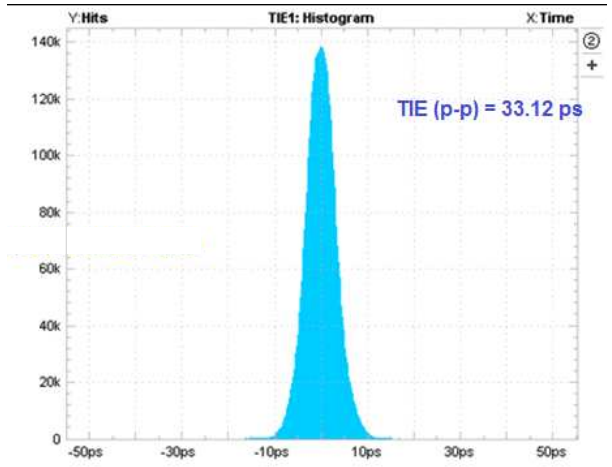

Figure 22. Time Interval Error Histogram: 3.0 Gbps With TS3USB3031 (Added Jitter = 2.57 ps)

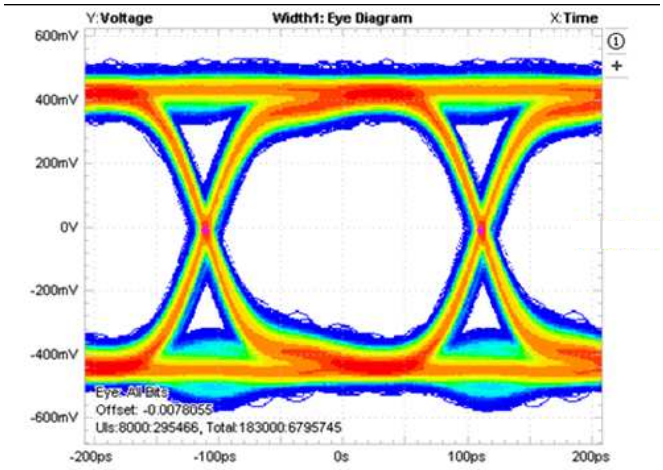

Figure 23. Eye Pattern Error Histogram: 4.5 Gbps With No Device

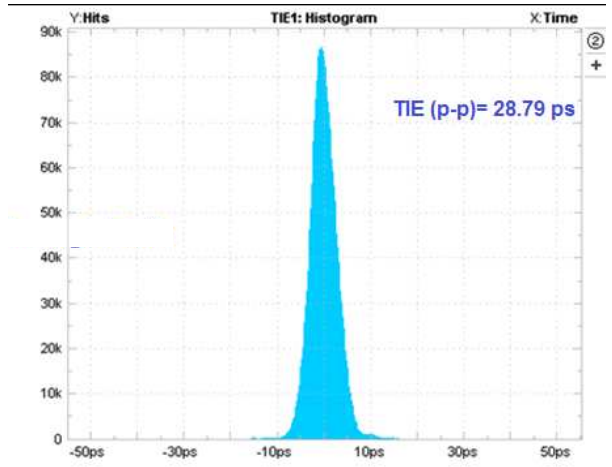

Figure 24. Time Interval Error Histogram: 4.5 Gbps With No Device

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Typical Application (continued)

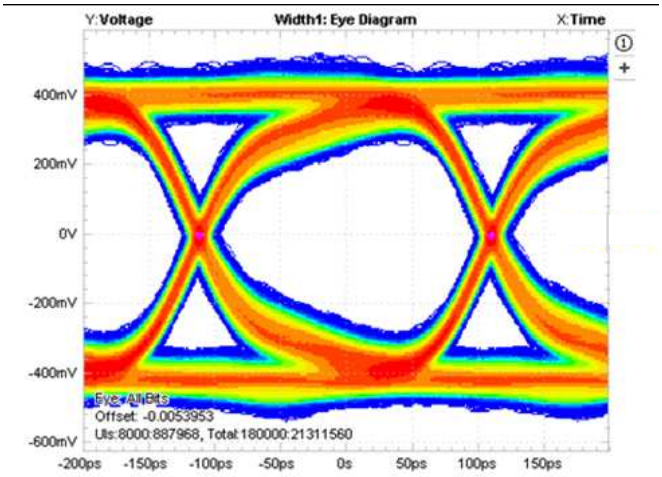

Figure 25. Eye Pattern Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

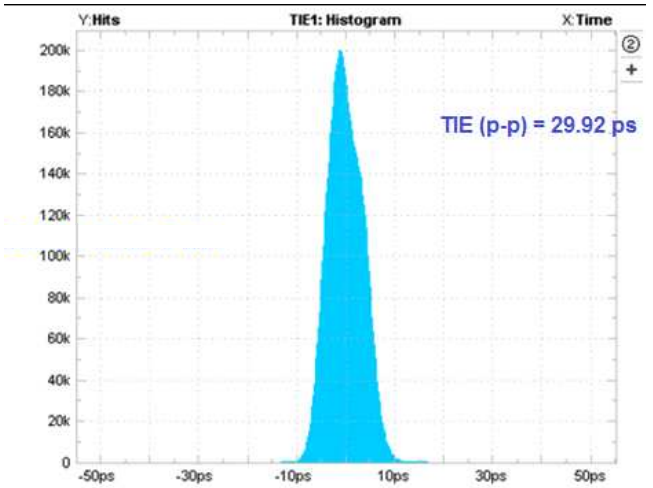

Figure 26. Time Interval Error Histogram: 4.5 Gbps With TS3USB3031 (Added Jitter = 1.13 ps)

9.2.3.2 USB EYE Pattern

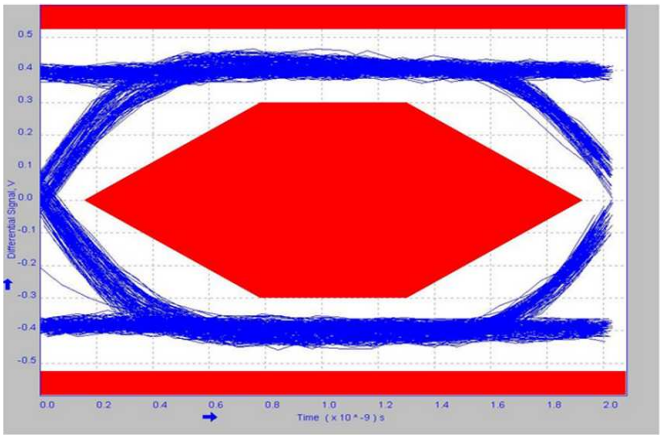

Figure 27. 480-Mbps USB 2.0 Eye Pattern With No Device

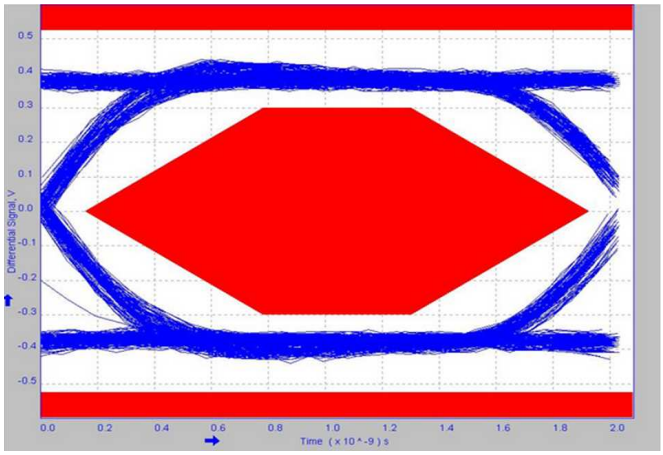

Figure 28. 480-Mbps USB 2.0 Eye Pattern for USB Switch

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10 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device does not require any power sequencing with respect to other devices in the system due to its power off isolation feature which allows signals to be present on the signal path pins before the device is powered up without damaging the device.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces must always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed-circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces must run on a single layer, preferably top layer. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

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11.2 Layout Example

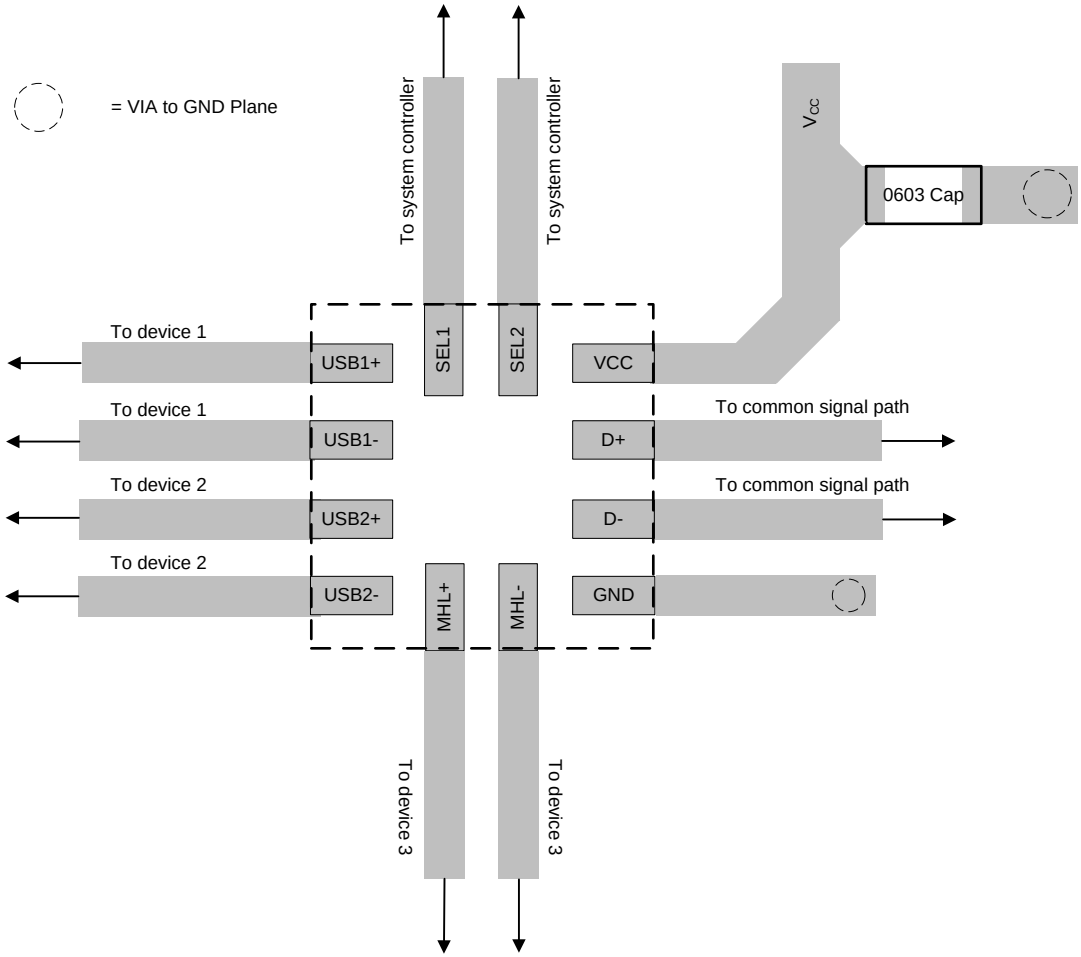

Figure 29. Layout Recommendation

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *High Speed Layout Guidelines* (SCAA082)
- *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB3031RMGR	ACTIVE	WQFN	RMG	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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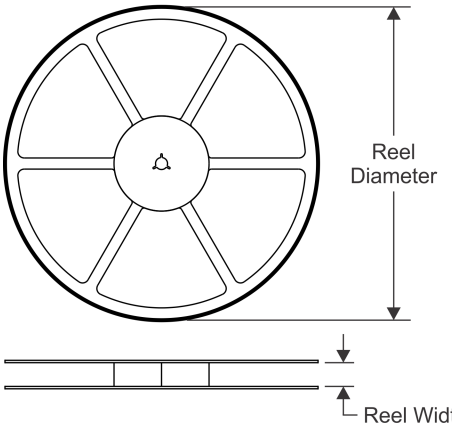
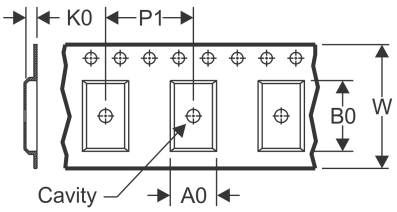
TAPE AND REEL INFORMATION

REEL DIMENSIONS

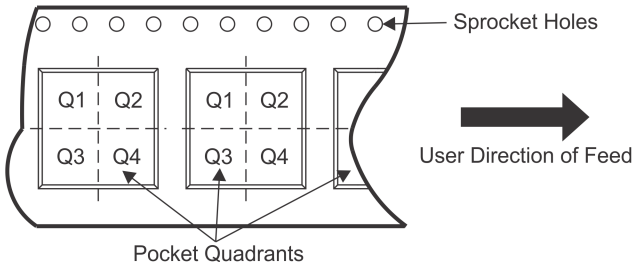


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

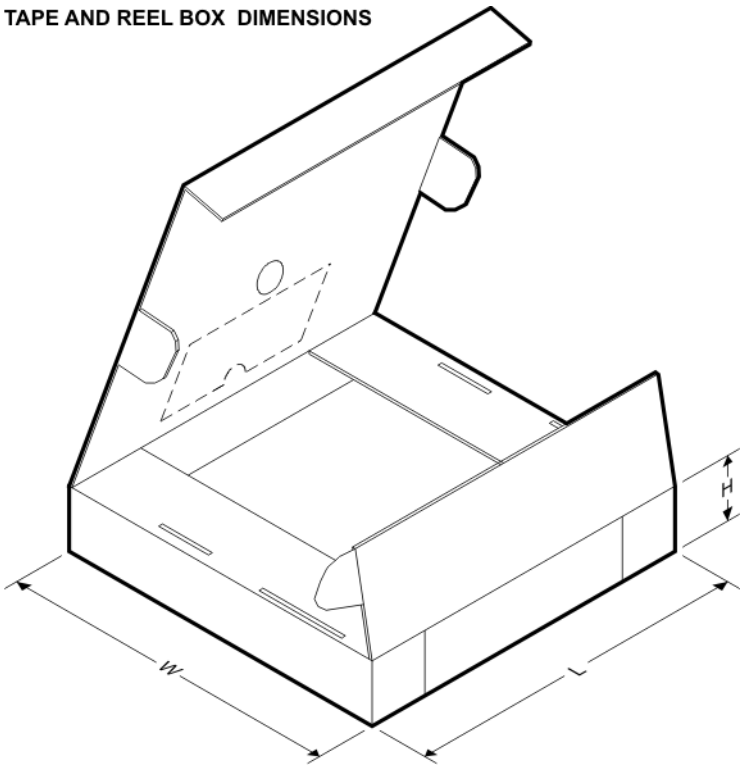
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB3031RMGR	WQFN	RMG	12	3000	180.0	8.4	2.05	2.05	1.0	4.0	8.0	Q1

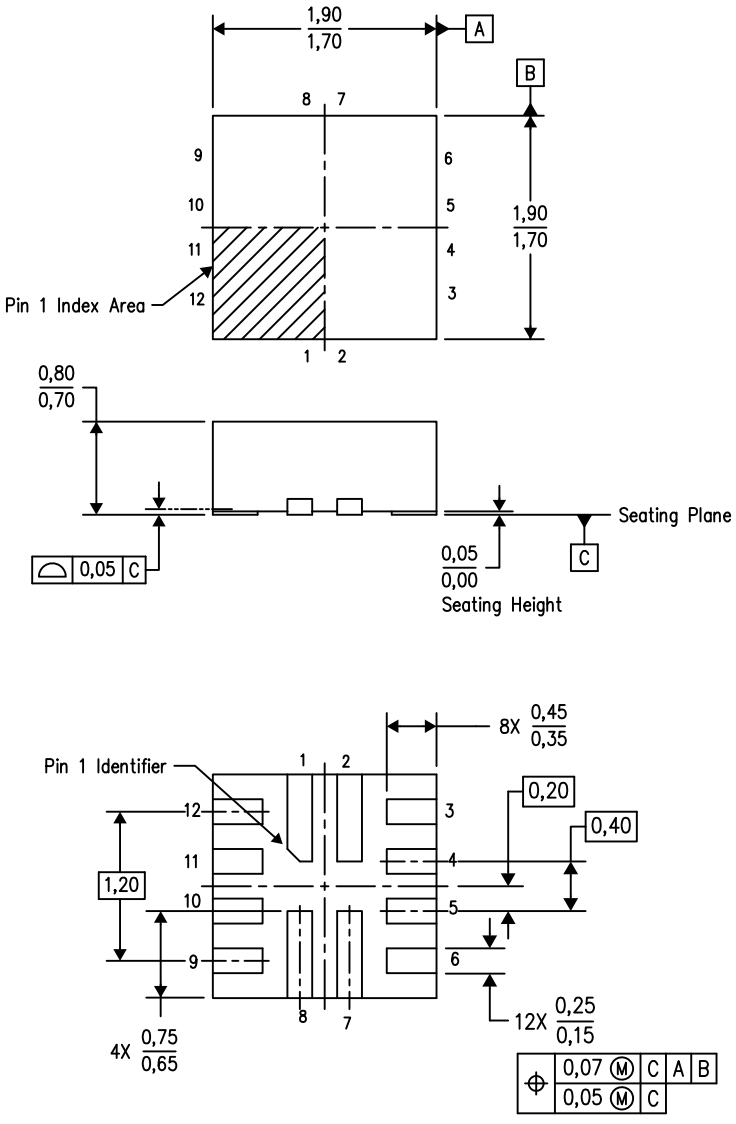
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB3031RMGR	WQFN	RMG	12	3000	210.0	185.0	35.0

RMG (S–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD

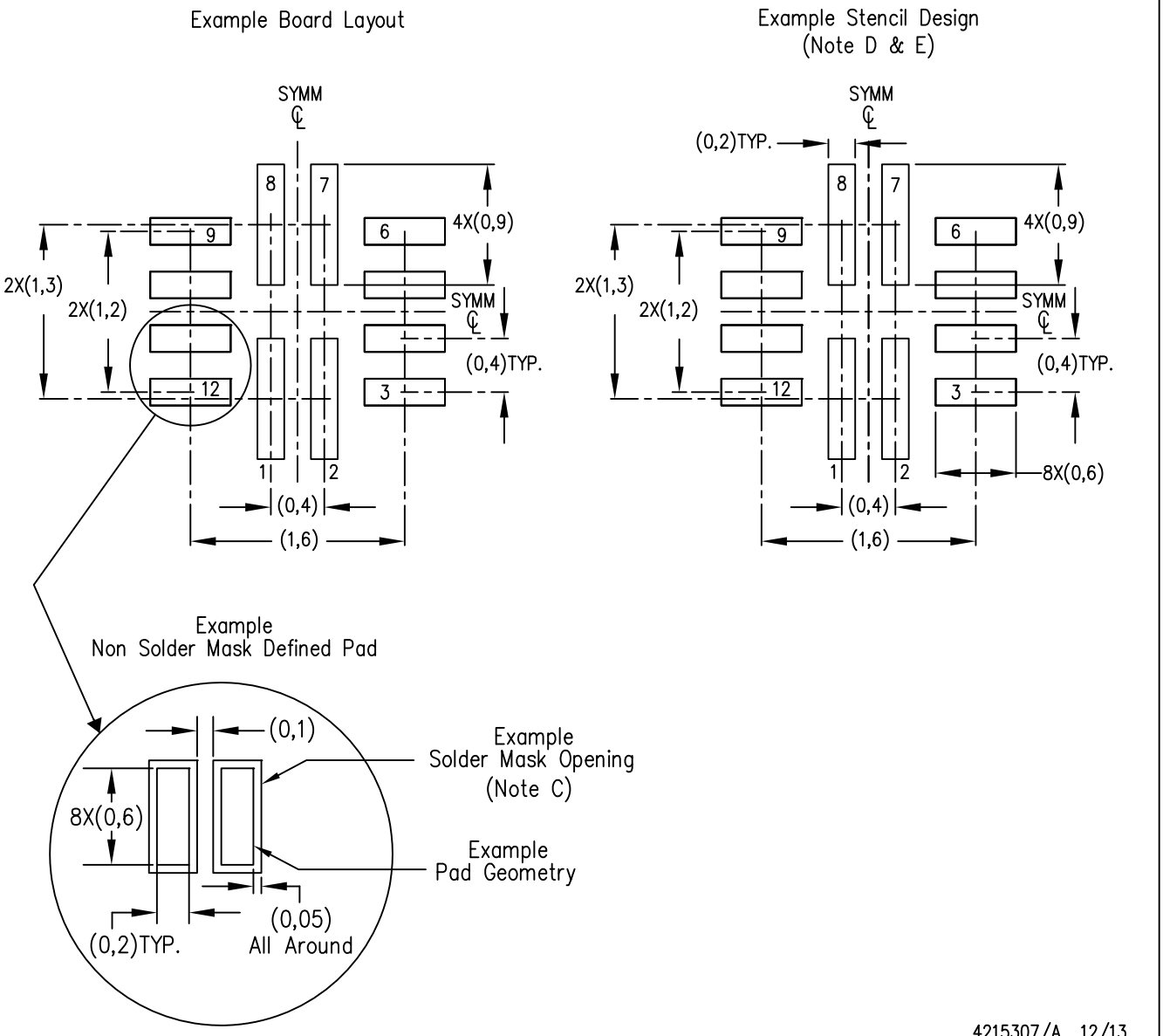


Bottom View

4218646/B 05/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.

RMG (S–PWQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
D. Maximum stencil thickness 0,1 mm (4 mils).
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

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