TPS65735 PMU for Active Shutter 3D Glasses

1 Device Overview

1.1 Features

- Linear Charger
  - Three Charger Phases: Pre-Charge, Fast Charge, and Charge Termination
  - Externally Set Charge Current Which Supports up to 100 mA
  - LED Current Sinks for Power Good and Charger Status Indication
- Low-Dropout Regulator (LDO) Supply for External Modules (Microcontroller, RF Module, IR Module)
  - LDO Continuous Output Current up to 30 mA
- Boost Converter
  - Adjustable Output Voltage: 8 V to 16 V
  - Boost Output Internally Connected to H-Bridge Analog Switches
- Full H-Bridge Analog Switches
  - Controlled by an External Microcontroller for System Operation
- Output Pin for Divided Down Battery Voltage Useful for ADC or Comparator Input of an MCU

1.2 Applications

Active Shutter 3D Glasses

1.3 Description

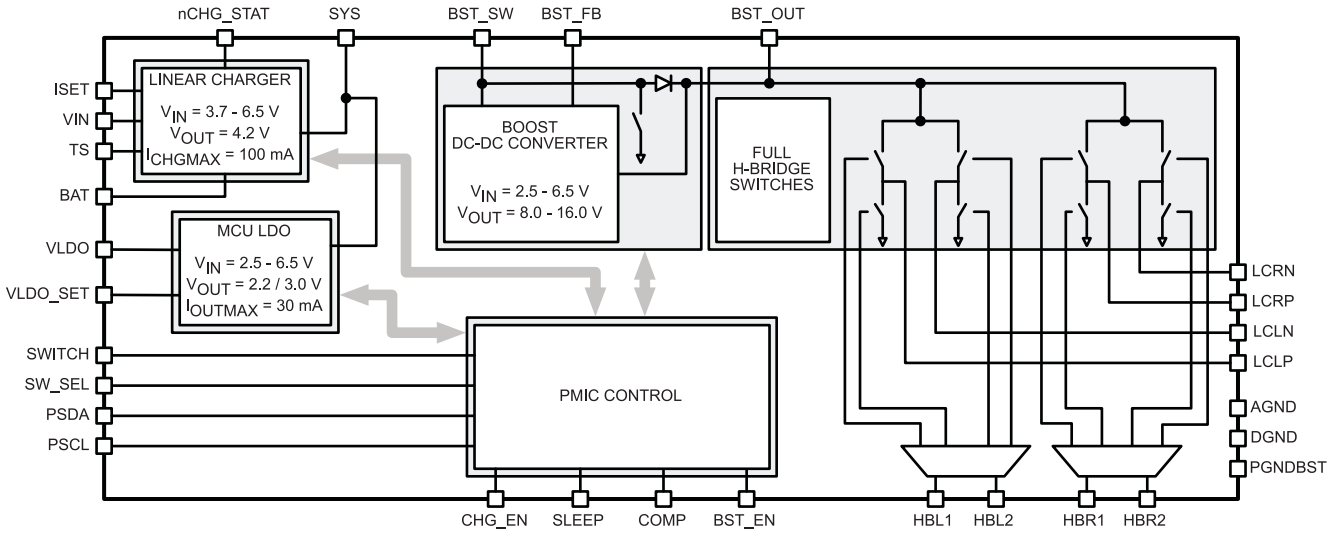
The TPS65735 device is a power management unit (PMU) for active shutter 3D glasses consisting of an integrated power path, linear charger, LDO, boost converter, and full H-bridge analog switches for left and right shutter operation in a pair of active shutter 3D glasses. In addition to the power devices, a typical 3D glasses system contains both a microcontroller and a communications front end (IR, RF, or other) in order to handle the communication and synchronous operation along with a 3D television.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65735	VSON (32)	4.00 mm x 4.00 mm

(1) For more information, see Section 10, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram



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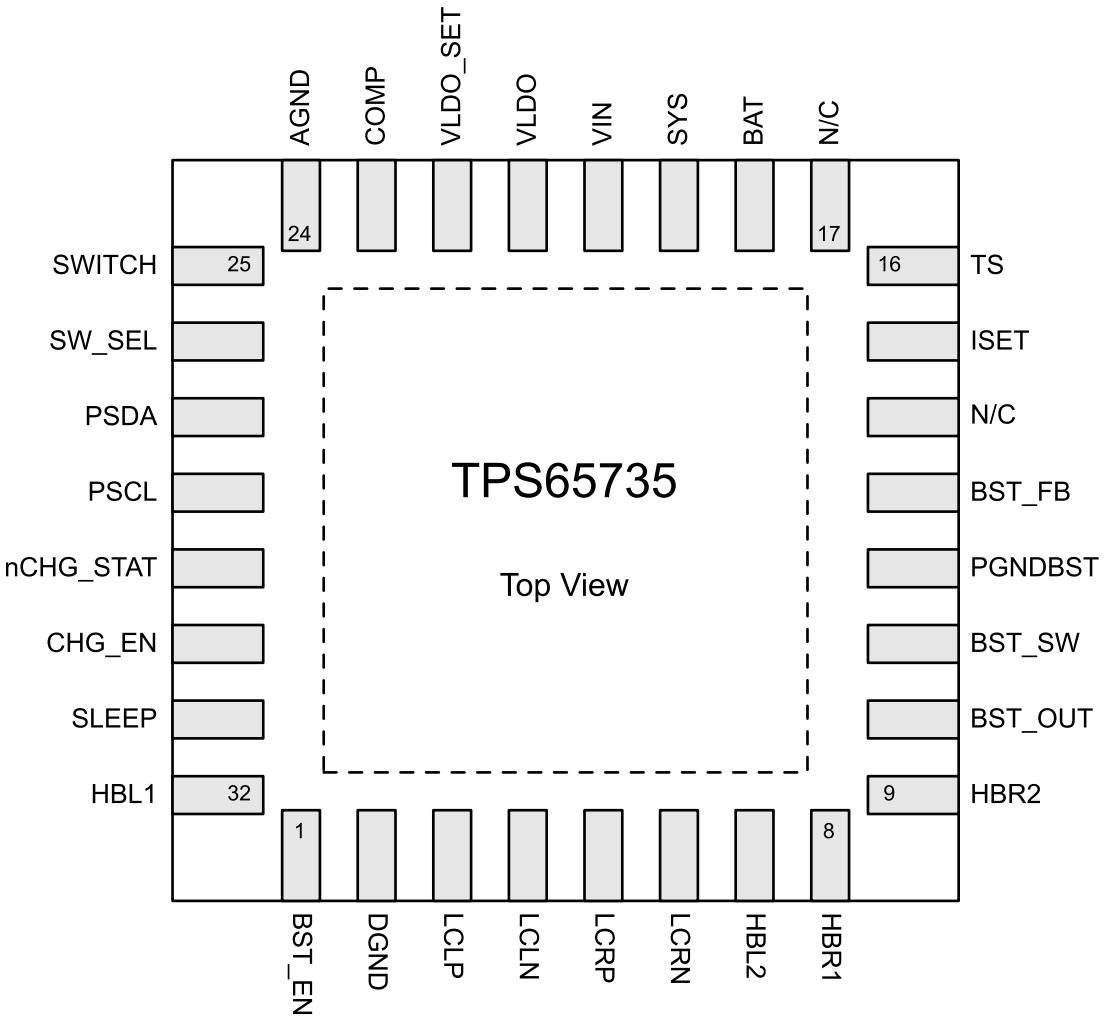
2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2011) to Revision A	Page
• Added *ESD Ratings* table, *Typical Characteristics* section, *Detailed Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

3 Terminal Configuration and Functions

3.1 Pin Diagram



A. Pins 14 and 17 = N/C. No internal connection; connect to main system ground.

Figure 3-1. 32-Pin RSN WQFN (Top View)

3.2 Pin Functions

Table 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
POWER MANAGEMENT CORE (PMIC)			
1	BST_EN	I	Boost Enable Input from an MCU, High = Boost Enabled
2	DGND	—	Digital Ground
3	LCLP	O	H-Bridge Output for Left LC Shutter, *Positive* Terminal
4	LCLN	O	H-Bridge Output for Left LC Shutter, *Negative* Terminal
5	LCRP	O	H-Bridge Output for Right LC Shutter, *Positive* Terminal
6	LCRN	O	H-Bridge Output for Right LC Shutter, *Negative* Terminal
7	HBL2	I	H-Bridge Input 2 for Left LC Shutter
8	HBR1	I	H-Bridge Input 1 for Right LC Shutter
9	HBR2	I	H-Bridge Input 2 for Right LC Shutter
10	BST_OUT	O	Boost Output
11	BST_SW	O	Boost Switch Node
12	PGNDBST	—	Boost Power Ground
13	BST_FB	I	Boost Feedback Node
15	ISET	I/O	Fast-Charge Current Setting Resistor
16	TS	I	Pin for 10-kΩ NTC Thermistor Connection **FLOAT IF THERMISTOR / TS FUNCTION IS NOT USED**
18	BAT	I/O	Charger Power Stage Output and Battery Voltage Sense Input
19	SYS	O	Output Terminal to System
20	VIN	I	AC or USB Adapter Input
21	VLDO	O	LDO Output
22	VLDO_SET	I	Sets LDO Output Voltage (see Table 5-2)
23	COMP	O	Scaled Battery Voltage for MCU Comparator or ADC Input (Battery Voltage Monitoring) **DO NOT CONNECT IF COMP FUNCTION IS NOT USED**
24	AGND	-	Analog Ground
25	SWITCH	I	Switch Input for Device Power On/Off
26	SW_SEL	I	Selects Type of Switch Connected to SWITCH Pin (see Table 5-6)
27	PSDA	I/O	I^2C Data Pin (only used for TI debug and test) **GROUND PIN IN APPLICATION**
28	PSCL	I/O	I^2C Clock Pin (only used for TI debug and test) **GROUND PIN IN APPLICATION**
29	nCHG_STAT	O	Open-drain Output, Charge Status Indication **CONNECT TO GROUND IF FUNCTION IS NOT USED**
30	CHG_EN	I	Charger Enable Input from an MCU, High = Boost Enabled
31	SLEEP	I/O	Sleep Enable Input from an MCU (edge triggered, only for system shutdown)
32	HBL1	I	H-Bridge Input 1 for Left LC Shutter
MISCELLANEOUS AND PACKAGE			
14, 17	N/C	—	All N/C should be connected to the main system ground.
33	Thermal PAD	—	There is an internal electrical connection between the exposed thermal pad and the AGND ground pin of the device. The thermal pad must be connected to the same potential as the AGND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. AGND pin must be connected to ground at all times.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Input voltage on all pins (except for VIN, BST_OUT, BST_SW, BST_FB, VLDO, LCLP, LCLN, LCRP, LCRN, AGND, DGND, and PGNDBST) with respect to AGND		–0.3	7	V
	VIN with respect to AGND		–0.3	28	V
	BST_OUT, BST_SW, LCLP, LCLN, LCRP, and LCRN with respect to PGNDBST		–0.3	18	V
	BST_FB with respect to PGNDBST, VLDO with respect to DGND		–0.3	3.6	V
T_A	Operating free-air temperature		0	60	°C
T_J	Junction temperature	Electrical characteristics ensured	0	85	°C
		Functionality ensured(3)	0	105	
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Device has a thermal shutdown feature implemented that shuts down at 105°C

4.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)	±1000	V
		Charged Device Model (CDM), per JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours (POH)

See (1)(2)(3)(4)

OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	JUNCTION TEMPERATURE (T_j)	LIFETIME POH(5)
100% OPP	1.1	–40 to 105 °C	100 K
120% OPP	1.2	–40 to 105 °C	100 K
166% OPP	1.35	–40 to 105 °C	49 K

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) To avoid significant degradation, the device power-on hours (POH) must be limited to those specified in this table.
(3) Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.
(4) Notations in this table cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.
(5) POH represent device operation under the specified nominal conditions continuously for the duration of the calculated lifetime.

4.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
CHARGER / POWER PATH					
V_{VIN}	Voltage at charger input pin	3.7		28 (1)	V
I_{VIN}	Input current at VIN pin			200	mA
C_{VIN}	Capacitor on VIN pin	0.1	2.2	10	µF
L_{VIN}	Inductance at VIN pin	0		2	µH
V_{SYS}	Voltage at SYS pin	2.5		6.4	V
$I_{SYS(OUT)}$	Output current at SYS pin			100	mA
C_{SYS}	Capacitor on SYS pin	0.1	4.7	10	µF
V_{BAT}	Voltage at BAT pin	2.5		6.4	V
C_{BAT}	Capacitor on BAT pin	4.7		10	µF
$R_{EXT(nCHG\_STAT)}$	Resistor connected to nCHG_STAT pin to limit current into pin	320			Ω
BOOST CONVERTER / H-BRIDGE SWITCHES					
$V_{IN(BST\_SW)}$	Input voltage for boost converter	2.5		6.5	V
V_{BST_OUT}	Output voltage for boost converter	8		16	V
C_{BST_OUT}	Boost output capacitor	3.3	4.7	10	µF
L_{BST_SW} (2)	Inductor connected between SYS and BST_SW pins	4.7		10 (3)	µH
LDO					
C_{VLDO}	External decoupling cap on pin VLDO	1		10	µF
POWER MANAGEMENT CORE CONTROL (LOGIC LEVELS FOR GPIOs)					
$V_{IL(PMIC)}$	GPIO low level (BST_EN, CHG_EN, SW_SEL, VLDO_SET and to switch H-Bridge inputs to a low, 0, level)			0.4	V
$V_{IH(PMIC)}$	GPIO high level (BST_EN, CHG_EN, SW_SEL, VLDO_SET and to switch H-Bridge inputs to a high, 1, level)	1.2			V

(1) VIN pin has 28 V ESD protection
(2) See Section 5.3.4 for information on boost converter inductor selection.
(3) Design optimized for boost operation with 10 µH inductor

4.5 Thermal Information

THERMAL METRIC		TPS65735 RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (3)	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter (4)	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter (5)	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (6)	3.5	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

4.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER POWER PATH						
$V_{UVLO(VIN)}$	Undervoltage lockout at power path input, VIN pin	V_{VIN}: 0 V → 4 V	3.2	3.3	3.45	V
$V_{HYS-UVLO(VIN)}$	Hysteresis on UVLO at power path input, VIN pin	V_{VIN}: 4 V → 0 V	200		300	mV
V_{IN-DT}	Input power detection threshold	Input power detected if: (V_{VIN} > V_{BAT} + V_{IN-DT}); V_{BAT} = 3.6 V V_{VIN}: 3.5 V → 4 V	40		140	mV
$V_{HYS-INDT}$	Hysteresis on V_{IN-DT}	V_{BAT} = 3.6 V V_{VIN}: 4 V → 3.5 V	20			mV
V_{OVP}	Input over-voltage protection threshold	V_{VIN}: 5 V → 7 V	6.4	6.6	6.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{VIN}: 11 V → 5 V		105		mV
$V_{DO(VIN-SYS)}$	VIN pin to SYS pin dropout voltage V_{VIN} – V_{SYS}	I_{SYS} = 150 mA (including I_{BAT}) V_{VIN} = 4.35 V V_{BAT} = 3.6 V			350	mV
$V_{DO(BAT-SYS)}$	BAT pin to SYS pin dropout voltage V_{BAT} – V_{SYS}	I_{SYS} = 100 mA V_{VIN} = 0 V V_{BAT} > 3 V			150	mV
$I_{VIN(MAX)}$	Maximum power path input current at pin VIN	V_{VIN} = 5 V		200		mA
$V_{SUP(ENT)}$	Enter battery supplement mode			V_{SYS} ≤ (V_{BAT} - 40 mV)		V
$V_{SUP(EXIT)}$	Exit battery supplement mode			V_{SYS} ≥ (V_{BAT} - 20 mV)		V
$V_{SUP(SC)}$	Output short-circuit limit in supplement mode			250		mV
$V_{O(SC)}$	Output short-circuit detection threshold, power-on			0.9		V
BATTERY CHARGER						
I_{CC}	Active supply current into VIN pin	V_{VIN} = 5 V No load on SYS pin V_{BAT} > $V_{BAT(REG)}$			2	mA
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection			1		mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold		1.6	1.8	2.0	V
$V_{BAT(REG)}$	Battery charger output voltage		–1%	4.20	1%	V
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.9	3.0	3.1	V
I_{CHG}	Charger fast charge current range I_{CHG} = K_{ISET} / R_{ISET}	V_{VIN} = 5 V $V_{BAT(REG)}$ > V_{BAT} > V_{LOWV}	5		100	mA
K_{ISET}	Battery fast charge current set factor I_{CHG} = K_{ISET} / R_{ISET}	V_{VIN} = 5 V $I_{VIN(MAX)}$ > I_{CHG} I_{CHG} = 100 mA No load on SYS pin, thermal loop not active.	–20%	450	20%	AΩ
I_{PRECHG}	Pre-charge current		0.07 × I_{CHG}	0.10 × I_{CHG}	0.15 × I_{CHG}	mA
I_{TERM}	Charge current value for termination detection threshold	I_{CHG} = 100 mA	7	10	15	mA

Electrical Characteristics *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RCH}	Recharge detection threshold	V_{BAT} below nominal charger voltage, $V_{BAT(REG)}$	55	100	170	mV
$I_{BAT(DET)}$	Sink current for battery detection			1		mA
t_{CHG}	Charge safety timer (18000 seconds = 5 hours)			18000		s
t_{PRECHG}	Pre-charge timer (1800 seconds = 30 minutes)			1800		s
V_{DPPM}	DPPM threshold			V_{BAT} + 100 mV		V
$I_{LEAK(nCHG)}$	Leakage current for nCHG_STAT pin	V_{nCHG_STAT} = 4.2 V CHG_EN = LOW (Charger disabled)			100	nA
$R_{DSON(nCHG)}$	On resistance for nCHG_STAT MOSFET switch			20	60	Ω
$I_{MAX(nCHG)}$	Maximum input current to nCHG_STAT pin				50	mA
BATTERY CHARGER NTC MONITOR						
I_{TSBIAS}	TS pin bias current			75		µA
V_{COLD}	0°C charge threshold for 10-kΩ NTC (β = 3490)			2100		mV
$V_{HYS(COLD)}$	Low temperature threshold hysteresis	Battery charging and battery / NTC temperature increasing		300		mV
V_{HOT}	50°C charge threshold for 10-kΩ NTC (β = 3490)			300		mV
$V_{HYS(HOT)}$	High temperature threshold hysteresis	Battery charging and battery / NTC temperature decreasing		30		mV
BATTERY CHARGER THERMAL REGULATION						
$T_{J(REG\_LOWER)}$	Charger lower thermal regulation limit			75		°C
$T_{J(REG\_UPPER)}$	Charger upper thermal regulation limit			95		°C
$T_{J(OFF)}$	Charger thermal shutdown temperature			105		°C
$T_{J(OFF-HYS)}$	Charger thermal shutdown hysteresis			20		°C
LDO						
$I_{MAX(LDO)}$	Maximum LDO output current, V_{VLDO} = 2.2 V	V_{SYS} = 4.2 V V_{VIN} = 0 V VLDO_SET = 0 V	30			mA
	Maximum LDO output current, V_{VLDO} = 3.0 V	V_{SYS} = 4.2 V V_{VIN} = 0 V VLDO_SET = V_{SYS}	30			mA
$I_{SC(LDO)}$	Short circuit current limit		30		100	mA
V_{VLDO}	LDO output voltage	VLDO_SET = LOW (VLDO_SET pin connected to DGND) 3.7 V ≤ V_{VIN} ≤ 6.5 V $I_{LOAD(LDO)}$ = –10 mA	2.13	2.2	2.27	V
V_{VLDO}	LDO output voltage	VLDO_SET = HIGH (V_{VLDO_SET} = V_{SYS}) 3.7 V ≤ V_{VIN} ≤ 6.5 V $I_{LOAD(LDO)}$ = –10 mA	2.91	3.0	3.09	V
$V_{DO(LDO)}$	LDO Dropout voltage	V_{VIN} - V_{LDO} when in dropout $I_{LOAD(LDO)}$ = –10 mA			200	mV

Electrical Characteristics *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Line regulation	3.7 V ≤ V_{VIN} ≤ 6.5 V $I_{LOAD(LDO)}$ = –10 mA	–1%		1%	
	Load regulation	V_{VIN} = 3.5 V 0.1 mA ≤ $I_{LOAD(LDO)}$ ≤ –10 mA	–2%		2%	
PSRR	Power supply rejection ratio	at 20 KHz, $I_{LOAD(LDO)}$ = 10 mA $V_{DO(LDO)}$ = 0.5 V C_{VLDO} = 10 µF		45		dB
BOOST CONVERTER						
$I_{Q(BST)}$	Boost operating quiescent current	Boost Enabled, BST_EN = High $I_{OUT(BST)}$ = 0 mA (boost is not switching) V_{BAT} = 3.6 V		2	4.5	µA
$R_{DSON(BST)}$	Boost MOSFET switch on-resistance	$V_{IN(BST)}$ = 2.5 V $I_{SW(MAIN)}$ = 200 mA		0.8	1.2	Ω
$I_{LKG(BST\_SW)}$	Leakage into BST_SW pin (includes leakage into analog h-bridge switches)	BST_EN signal = LOW (Boost disabled) V_{BST_SW} = 4.2 V No load on BST_OUT pin			90	nA
$I_{SWLIM(BST)}$	Boost MOSFET switch current limit		100	150	200	mA
$V_{DIODE(BST)}$	Voltage across integrated boost diode during normal operation	BST_EN signal = HIGH V_{BST_SW} = 16.0 V I_{BST_OUT} = –2 mA			1.0	V
$V_{REF(BST)}$	Boost reference voltage on BST_FB pin		1.17	1.2	1.23	V
$V_{REFHYS(BST)}$	Boost reference voltage hysteresis on BST_FB pin		2%	2.5%	3.2%	
$T_{ON(BST)}$	Maximum on time detection threshold		5	6.5	8	µs
$T_{OFF(BST)}$	Minimum off time detection threshold		1.4	1.75	2.1	µs
$T_{SHUT(BST)}$	Boost thermal shutdown threshold			105		°C
$T_{SHUT-HYS(BST)}$	Boost thermal shutdown threshold hysteresis			20		°C
FULL H-BRIDGE ANALOG SWITCHES						
$I_{Q(HSW)}$	Operating quiescent current for h-bridge switches				5	µA
$R_{DSON(HSW)}$	H-bridge switches on resistance			20	40	Ω
$T_{DELAY(HSW-H)}$	H-bridge switch propagation delay, input switched from low to high state.	V_{HBxy} = 0 V → V_{VLDO}		100		ns
$T_{DELAY(HSW-L)}$	H-bridge switch propagation delay, input switched from high to low state.	V_{HBxy} = V_{VLDO} → 0 V		100		ns
POWER MANAGEMENT CORE CONTROLLER						
$V_{IL(PMIC)}$	Low logic level for logic signals on power management core (BST_EN, CHG_EN, SLEEP, HBR1, HBR2, HBL1, HBL2)	IO logic level decreasing: V_{SYS} → 0 V I_{IN} = 1 mA			0.4	V
$V_{IH(PMIC)}$	High logic level for signals on power management core (BST_EN, CHG_EN, SLEEP, HBR1, HBR2, HBL1, HBL2)	IO logic level increasing: 0 V → V_{SYS} I_{IN} = 1 mA	1.2			V

Electrical Characteristics *(continued)*

over operating free-air temperature range (unless otherwise noted)

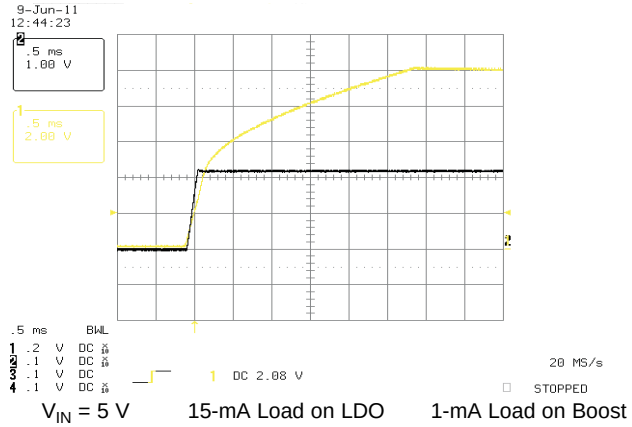
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{GOOD(LDO)}$	Power fault detection threshold	V_{VLDO} decreasing			1.96	V
$V_{GOOD\_HYS(LDO)}$	Power fault detection hysteresis	V_{VLDO} increasing		50		mV
$V_{BATCOMP}$	COMP pin voltage (scaled down battery voltage)	V_{BAT} = 4.2 V V_{VLDO} = 2.2 V		1.85		V
		V_{BAT} = 2.5 V V_{VLDO} = 2.2 V		1.10		
		V_{BAT} = 4.2 V V_{VLDO} = 3.0 V		1.90		
		V_{BAT} = 3.3 V V_{VLDO} = 3.0 V		1.50		

4.7 Quiescent Current

over operating free-air temperature range (unless otherwise noted)

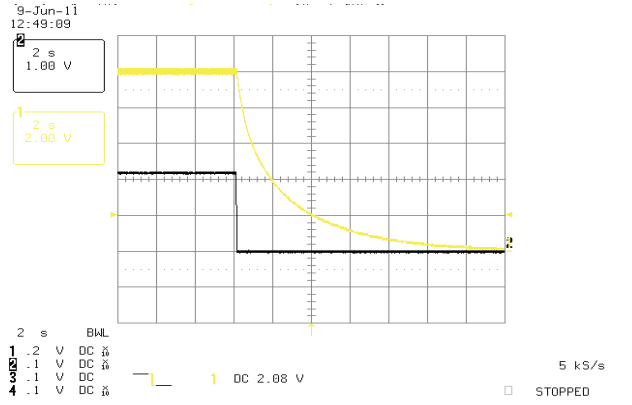
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q(SLEEP)}$	Power management core quiescent current in sleep mode	at 25° C V_{BAT} = 3.6 V V_{VIN} = 0 V No load on LDO CHG_EN, BST_EN grounded BST_FB = 300 mV Power management core in sleep mode / device 'off'		8.6	10.5	µA
$I_{Q(ACTIVE)}$	Power management core quiescent current in active mode	at 25° C V_{BAT} = 3.6 V V_{VIN} = 0 V Boost enabled but not switching, H-bridge in grounded state No load on LDO Power management core in active mode		39	53.5	µA

4.8 Typical Characteristics



V_{IN} = 5 V 15-mA Load on LDO 1-mA Load on Boost

Figure 4-1. Startup



V_{IN} = 5 V 15-mA Load on LDO 1-mA Load on Boost

Figure 4-2. Shutdown

5 Detailed Description

5.1 Overview

The TPS65735 integrates a linear charger and a Boost Converter to create a PMIC for active shutter 3D glasses.

5.2 Functional Block Diagram

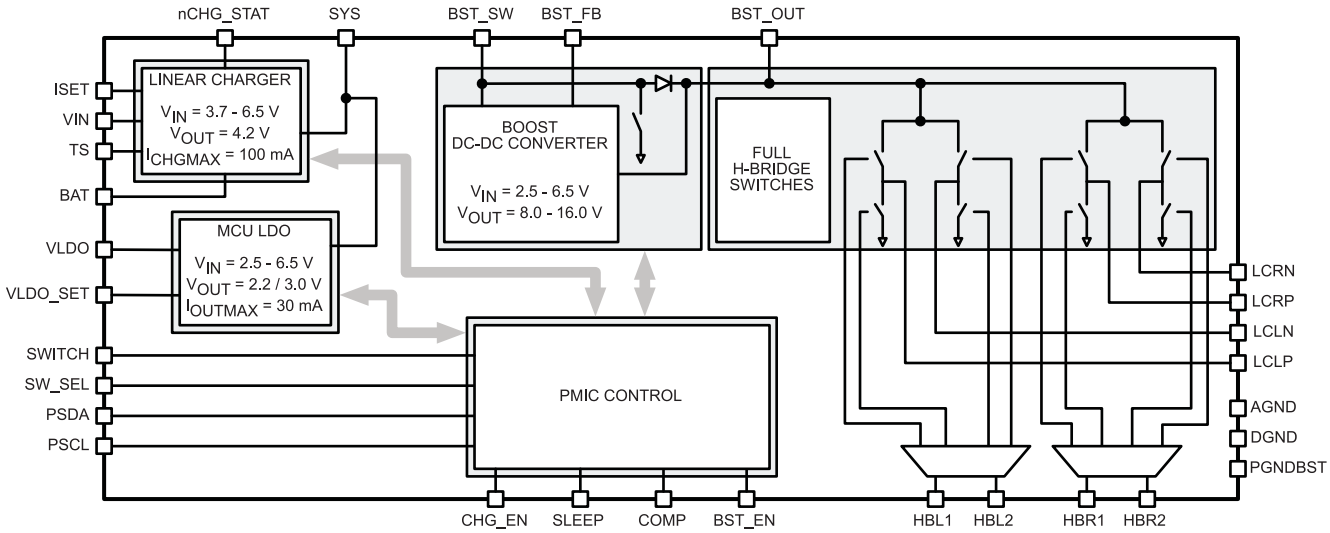


Figure 5-1. TPS65735 Simplified Functional Block Diagram

5.3 Feature Description

5.3.1 System Operation

The system must complete the power up routine before it enters normal operating mode. The specific system operation depends on the setting defined by the state of the SW_SEL pin. The details of the system operation for each configuration of the SW_SEL pin are contained in this section.

5.3.1.1 System Power Up

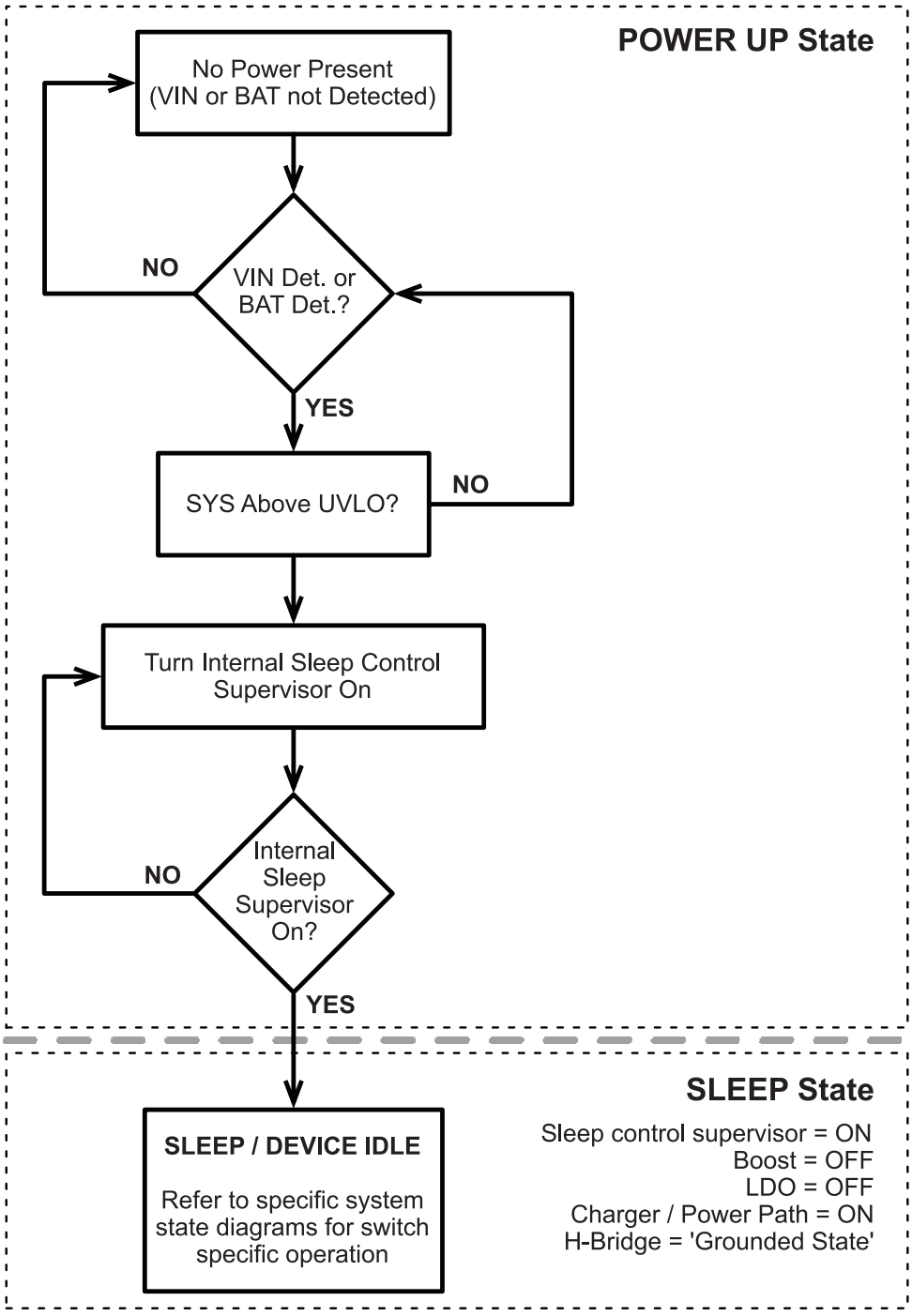


Figure 5-2. System Power Up State Diagram

5.3.1.2 System Operation Using Push Button Switch

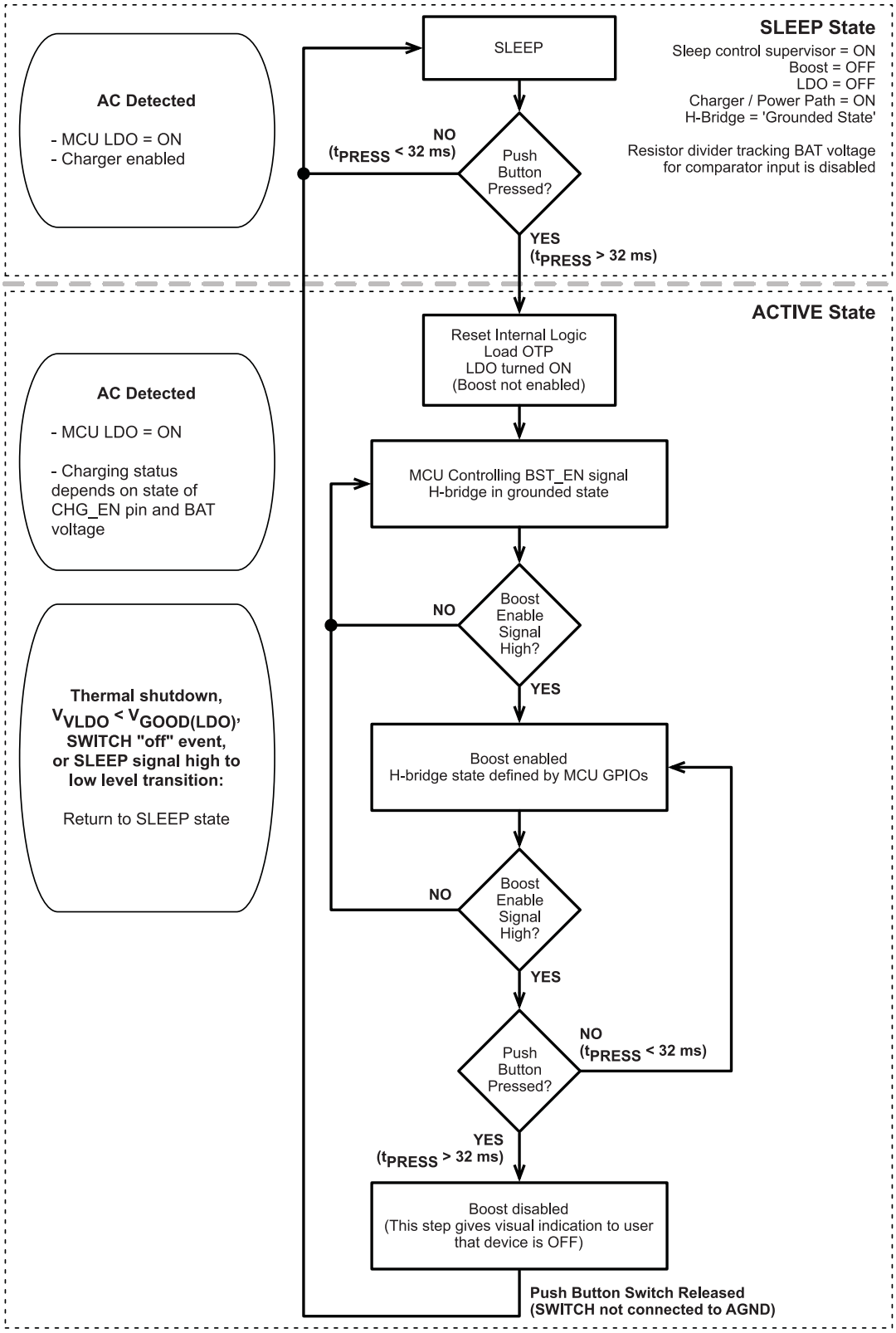


Figure 5-3. Push Button State Diagram

5.3.1.3 System Operation Using Slider Switch

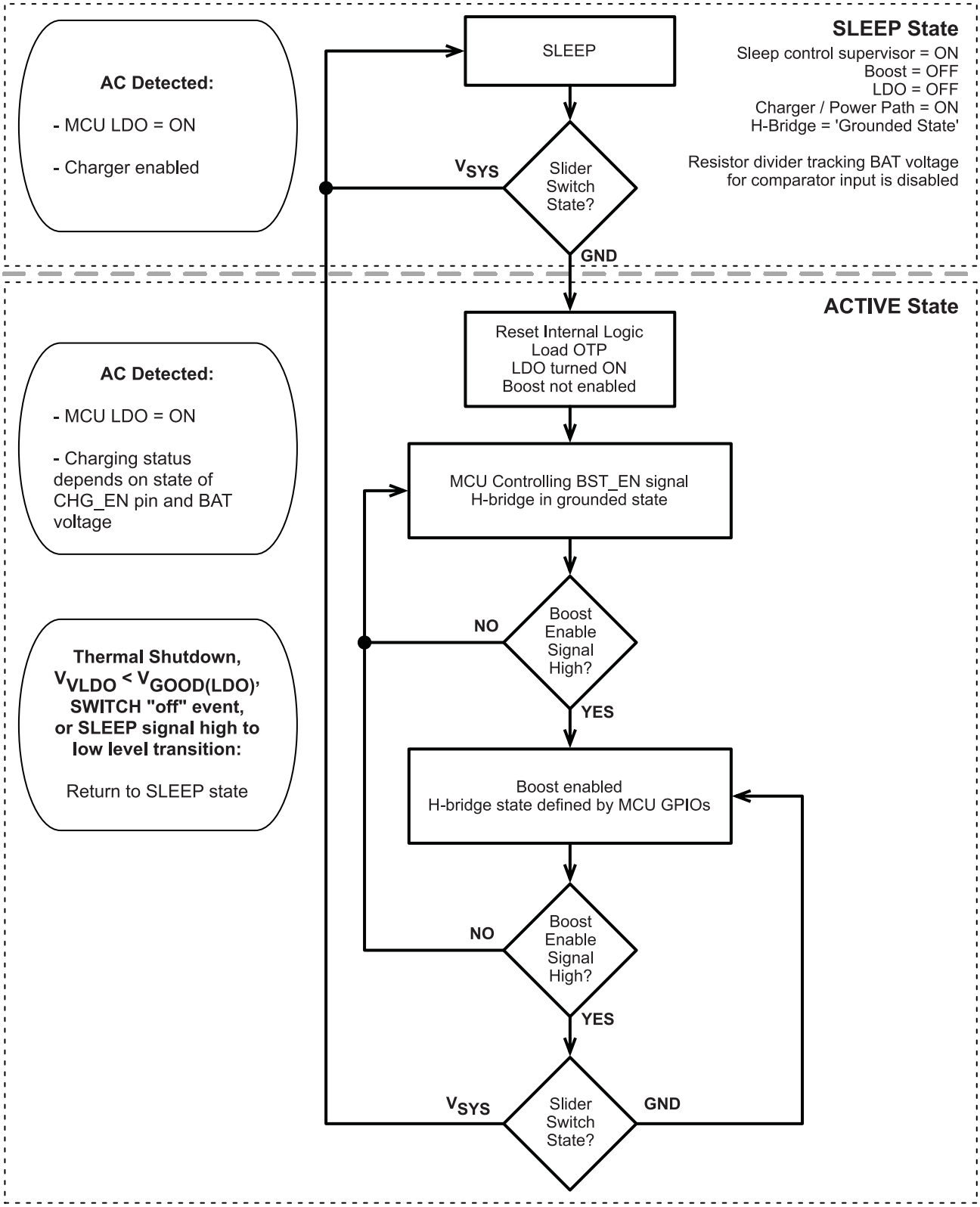


Figure 5-4. System Operation Using Slider Switch

5.3.2 Linear Charger Operation

This device has an integrated Li-Ion battery charger and system power path management feature targeted at space-limited portable applications. The architecture powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination, and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery.

The input power source for charging the battery and running the system can be an AC adapter or USB port connected to the VIN pin as long as the input meets the device operating conditions outlined in this datasheet. The power-path management feature automatically reduces the charging current if the system load increases. Note that the charger input, VIN, has voltage protection up to 28 V.

5.3.2.1 Battery and TS Detection

To detect and determine between a good or damaged battery, the device checks for a short circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage on the BAT pin. While sourcing this current if the BAT pin voltage exceeds $V_{BAT(SC)}$, a battery has been detected. If the voltage stays below the $V_{BAT(SC)}$ level, the battery is presumed to be damaged and not safe to charge.

The device will also check for the presence of a 10-kΩ NTC thermistor attached to the TS pin of the device. The check for the NTC thermistor on the TS pin is done much like the battery detection feature described previously. The voltage on the TS pin is compared against a defined level and if it is found to be above the threshold, the NTC thermistor is assumed to be disconnected or not used in the system. To reduce the system quiescent current, the NTC thermistor temperature sensing function is only enabled when the device is charging and when the thermistor has been detected.

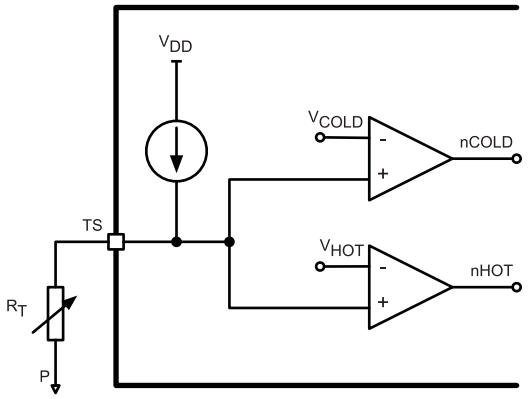


Figure 5-5. Thermistor Detection and Circuit

5.3.2.2 Battery Charging

The battery is charged in three phases: conditioning pre-charge, constant-current fast charge (current regulation), and a constant-voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. Figure 5-6 shows what happens in each of the three charge phases:

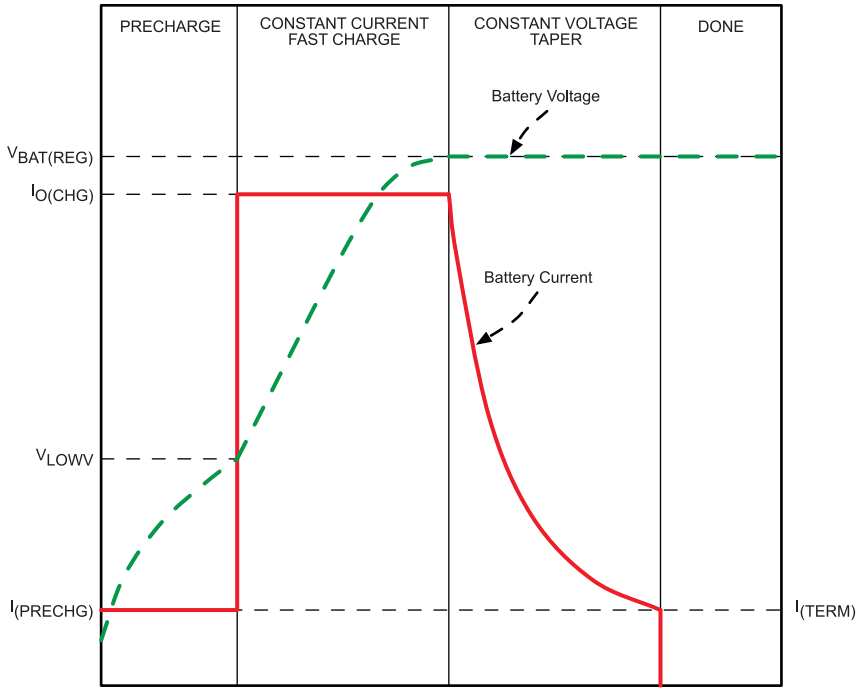


Figure 5-6. Battery Charge Phases

In the pre-charge phase, the battery is charged with the pre-charge current that is scaled to be 10% of the fast-charge current set by the resistor connected to the ISET pin. Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the charger indicates charging is done by making the nCHG_STAT pin high impedance. Note that termination detection is disabled whenever the charge rate is reduced from the set point because of the actions of the thermal loop, the DPM loop, or the $V_{IN(LOWV)}$ loop.

5.3.2.2.1 Pre-charge

The value for the pre-charge current is set to be 10% of the charge current that is set by the external resistor, R_{ISET}. Pre-charge current is scaled to lower currents when the charger is in thermal regulation.

5.3.2.2.2 Charge Termination

In the fast charge state, once $V_{BAT} \geq V_{BAT(REG)}$, the charger enters constant voltage mode. In constant voltage mode, the charge current will taper until termination when the charge current falls below the $I_{(TERM)}$ threshold (typically 10% of the programmed fast charge current). Termination current is not scaled when the charger is in thermal regulation. When the charging is terminated, the nCHG_STAT pin will be high impedance (effectively turning off any LED that is connected to this pin).

5.3.2.2.3 Recharge

Once a charge cycle is complete and termination is reached, the battery voltage is monitored. If $V_{BAT} < V_{BAT(REG)} - V_{RCH}$, the device determines if the battery has been removed. If the battery is still present, then the recharge cycle begins and will end when $V_{BAT} \geq V_{BAT(REG)}$.

5.3.2.2.4 Charge Timers

The charger in this device has internal safety timers for the pre-charge and fast charge phases to prevent potential damage to either the battery or the system. The default values for these timers are found as follows: Pre-charge timer = 0.5 hours (30 minutes) and Fast charge timer = 5 hours (300 minutes).

During the fast charge phase, the following events may increase the timer durations:

1. The system load current activates the DPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current.

If the pre-charge timer expires before the battery voltage reaches V_{LOWV}, the charger indicates a fault condition.

5.3.2.3 Charger Status (nCHG_STAT Pin)

The nCHG_STAT pin is used to indicate the charger status by an externally connected resistor and LED circuit. The pin is an open drain input and the internal switch is controlled by the logic inside of the charger. This pin may also be connected to a GPIO of the system MCU to indicate charging status. The table below details the status of the nCHG_STAT pin for various operating states of the charger.

Table 5-1. nCHG_STAT Functionality

CHARGING STATUS	nCHG_STAT FET / LED
Pre-charge / Fast Charge / Charge Termination	ON
Recharge	OFF
OVP	OFF
SLEEP	OFF

5.3.3 LDO Operation

The power management core has a low dropout linear regulator (LDO) with variable output voltage capability. This LDO is used for supplying the microcontroller and may be used to supply either an external IR or RF module, depending on system requirements. The LDO can supply a continuous current of up to 30 mA.

The output voltage (V_{VLDO}) of the LDO is set by the state of the VLDO_SET pin. See Table 5-2 for details on setting the LDO output voltage.

Table 5-2. VLDO_SET Functionality

VLDO_SET STATE	VLDO OUTPUT VOLTAGE (V_{VLDO})
Low (VLDO_SET < $V_{IL(PMIC)}$)	2.2 V
High (VLDO_SET > $V_{IH(PMIC)}$)	3.0 V

5.3.3.1 LDO Internal Current Limit

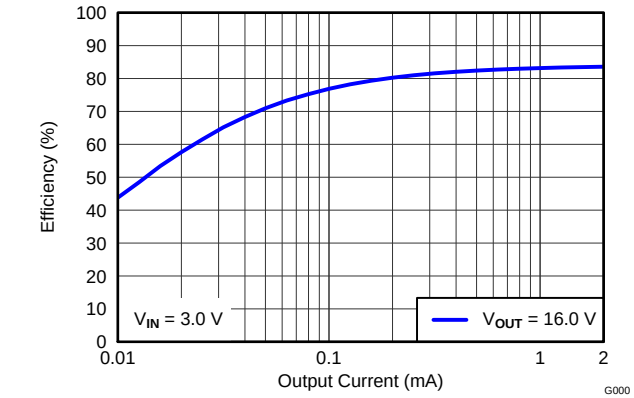
The internal current limit feature helps protect the LDO regulator during fault conditions. During current limit, the output sources a fixed amount of current, defined in the Electrical Characteristics table. The voltage on the output in this stage can not be regulated and will be $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The pass transistor integrated into the LDO will dissipate power, $(V_{IN} - V_{OUT}) \times I_{LIMIT}$, until the device enters thermal shutdown. In thermal shutdown the device will enter the *SLEEP / POWER OFF* state which means that the LDO will then be disabled and shut off.

5.3.4 Boost Converter Operation

The boost converter in this device is designed for active shutter 3D glasses. This load is typically a light load where the average current is 2 mA or lower and the peak current out of a battery is limited in operation. This asynchronous boost converter operates with a minimum off time / maximum on time for the integrated low side switch, these values are specified in the Electrical Characteristics table of this datasheet.

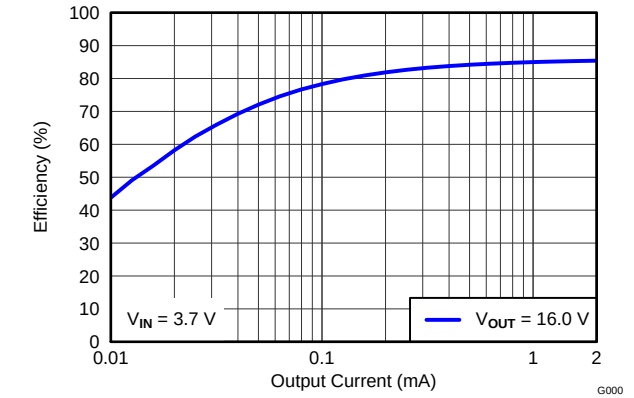
The peak output voltage from the boost converter is adjustable and set by using an external resistor divider connected between BST_OUT pin, BST_FB pin, and ground. The peak output voltage is set by choosing resistors for the feedback network such that the voltage on the BST_FB pin is $V_{REF(BST)}$ = 1.2 V. See Section 6.2.1.2.2 for more information on calculating resistance values for this feedback network.

The efficiency curves for various input voltages over the typical 3D glasses load range (2 mA and lower) are shown below. All curves are for a target V_{OUT} of 16 V. For output voltages less than 16 V, a higher efficiency at each operating input voltage should be expected. Note that efficiency is dependent upon the external boost feedback network resistance, the inductor used, and the type of load connected.



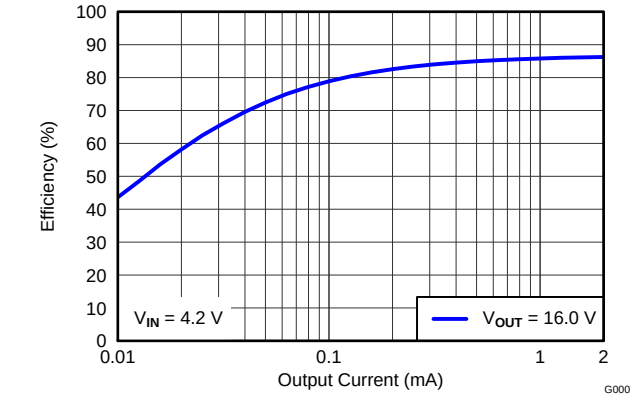
V_{IN} = 3.0 V V_{OUT} = 16 V

Figure 5-7. Boost Efficiency vs I_{OUT}



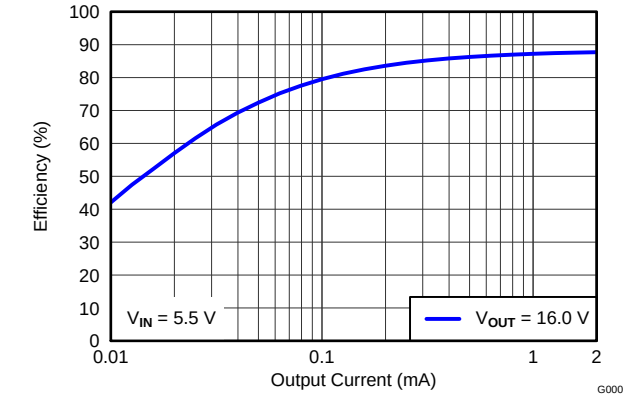
V_{IN} = 3.7 V V_{OUT} = 16 V

Figure 5-8. Boost Efficiency vs I_{OUT}



V_{IN} = 4.2 V V_{OUT} = 16 V

Figure 5-9. Boost Efficiency vs I_{OUT}



V_{IN} = 5.5 V V_{OUT} = 16 V

Figure 5-10. Boost Efficiency vs I_{OUT}

5.3.4.1 Boost Thermal Shutdown

An internal thermal shutdown mode is implemented in the boost converter that shuts down the device if the typical junction temperature of 105°C is exceeded. If the device is in thermal shutdown mode, the main switch of the boost is open and the device enters the *SLEEP / POWER OFF* state.

5.3.4.2 Boost Load Disconnect

When the boost is disabled (BST_EN = LOW), the H-bridge is automatically placed into the OFF state. In the OFF state the high side H-bridge switches are open and the low side switches of the H-bridge are closed. The OFF state grounds and discharges the load, potentially prolonging the life of the LC shutters by eliminating any DC content (see Section 5.3.5.1 for more information regarding the H-bridge states). The disconnection of the load is done with the H-Bridge and can be seen in the next figure (Figure 5-11).

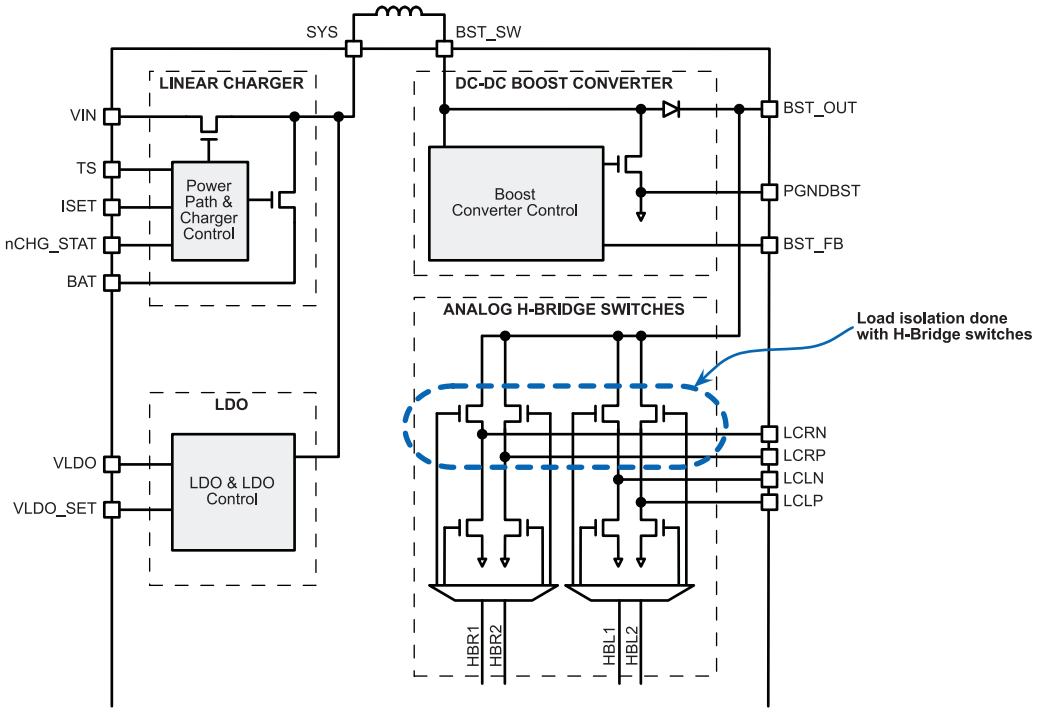


Figure 5-11. Boost Load Disconnect

An advantage to this topology for disconnecting the load is that the boost output capacitor is charged to approximately the SYS voltage level, specifically V_{SYS} - $V_{DIODE(BST)}$, when the boost is disabled. This design ensures that there is not a large in-rush current into the boost output capacitor when the boost is enabled. The boost operation efficiency is also increased because there is no load disconnect switch in the boost output path. A load disconnect switch would decrease efficiency because of the resistance that it would introduce.

5.3.5 Full H-Bridge Analog Switches

The TPS65735 has two integrated full H-bridge analog switches that can be connected to GPIOs of a host microcontroller. There is an internal level shifter that manages the input signals to the H-Bridge switches.

5.3.5.1 H-Bridge Switch Control

The H-Bridge switches are controlled by an external microcontroller for system operation - specifically to control charge polarity on the LCD shutters. Depending on the state of the signals from the microcontroller, the H-Bridge will be put into 4 different states. These states are:

- **OPEN**: All Switches Opened
- **CHARGE+**: Boost Output Voltage Present on Pins LCLP or LCRP
- **CHARGE-**: Boost Output Voltage Present on Pins LCLN or LCRN
- **GROUNDED**: High Side Switches are Opened and Low Side Switches are Closed

If CHARGE+ state is followed by the CHARGE- state, the voltage across the capacitor connected to the H-Bridge output terminals will be reversed. The system automatically switches to the GROUNDED state when the boost is disabled by the BST_EN pin - for more details see Section 5.3.1.

Table 5-3. H-Bridge States from Inputs

HBx2 [HBL2 & HBR2]	HBx1 [HBL1 & HBR1]	H-Bridge STATE
0	0	OPEN
0	1	CHARGE +
1	0	CHARGE -
1	1	GROUNDED

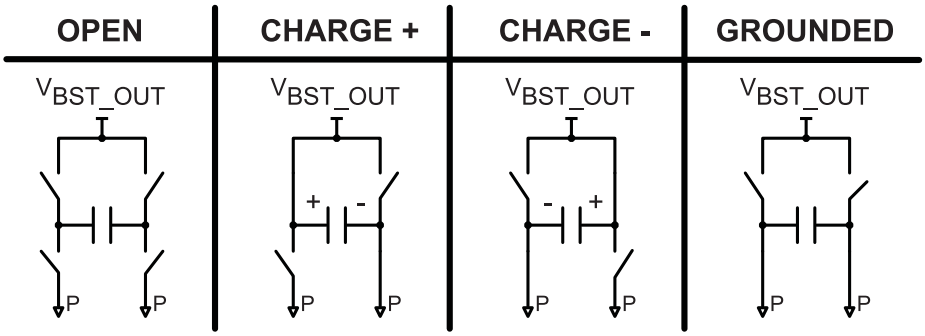


Figure 5-12. H-Bridge States

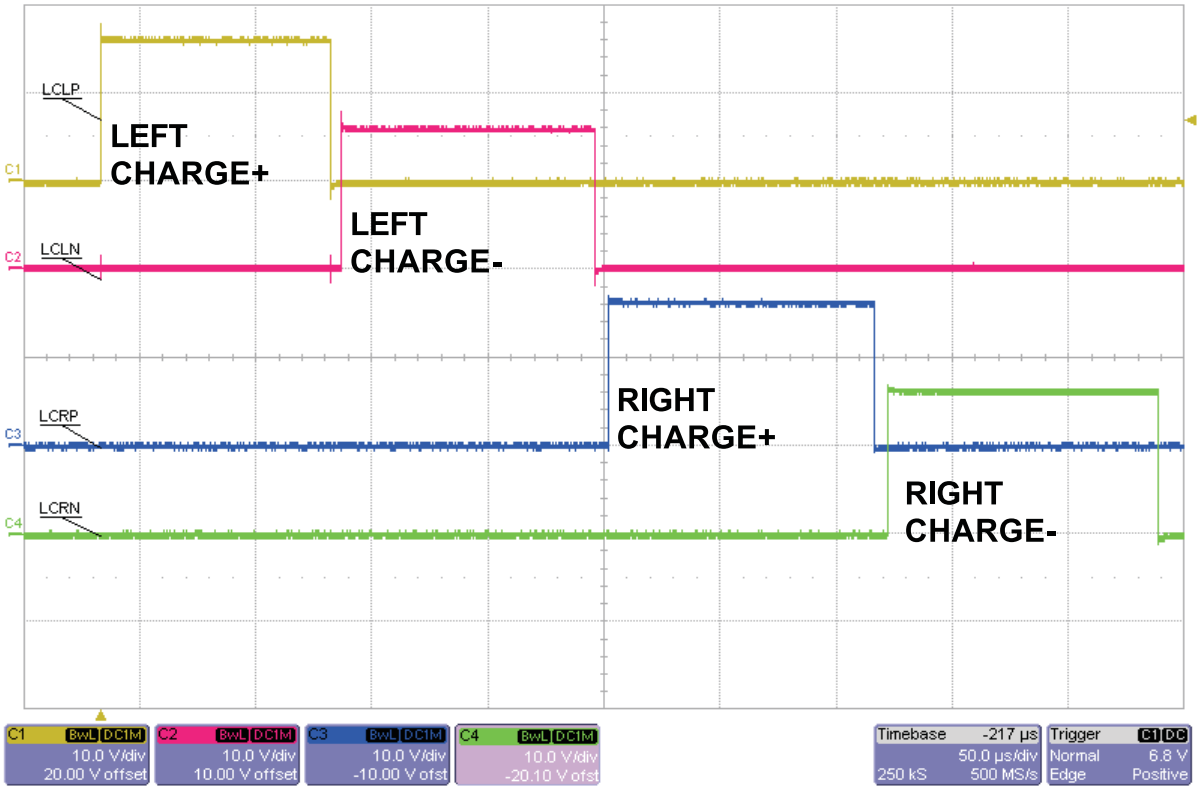


Figure 5-13. H-Bridge States from Oscilloscope

5.3.6 Power Management Core Control

Various functions of the power management core can be controlled by GPIOs of an external MCU or by setting the default state by connecting these function pins to a logic high or low level on the PCB.

5.3.6.1 SLEEP / Power Control Pin Function

The internal SLEEP signal between the power management device and the MSP430 can be used to control the power down behavior of the device. This has multiple practical applications such as a watchdog implementation for the communication between the sender (TV) and the receiver (3D glasses) or different required system on and off times; typically when the push-button press timing for an off event is a few seconds in length, programmable by software in the system MCU.

If there is a requirement that the push-button press for system on and off events are different, the SLEEP signal must be set to a logic high value ($V_{SLEEP} > V_{IH(PMIC)}$) upon system startup. This implementation allows the device to power down the system on the falling edge of the SLEEP signal (when: $V_{SLEEP} < V_{IL(PMIC)}$).

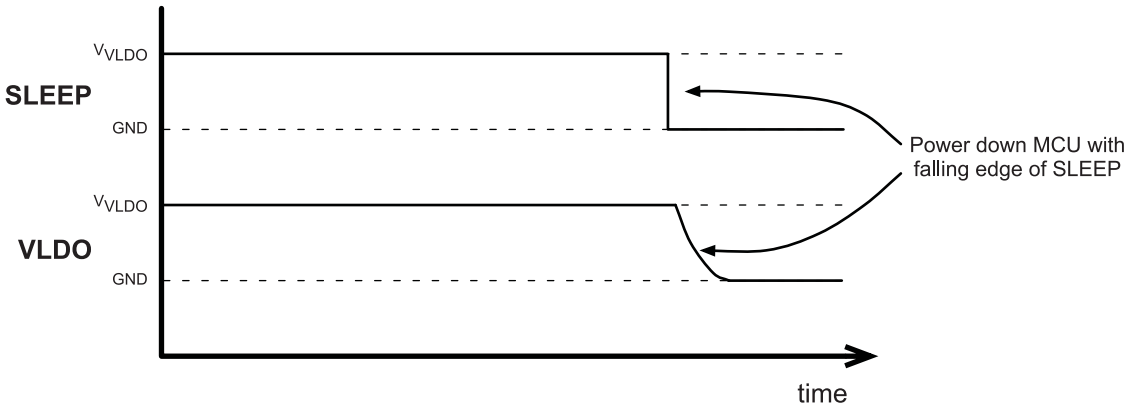


Figure 5-14. SLEEP Signal to Force System Power Off

5.3.6.2 COMP Pin Functionality

The COMP pin is used to output a scaled down voltage level related to the battery voltage for input to a comparator of a microcontroller. Applications for this COMP feature could be to generate an interrupt on the microcontroller when battery voltage drops under a threshold and the device can then be shut down or indicate to the end user with an LED that the battery requires charging.

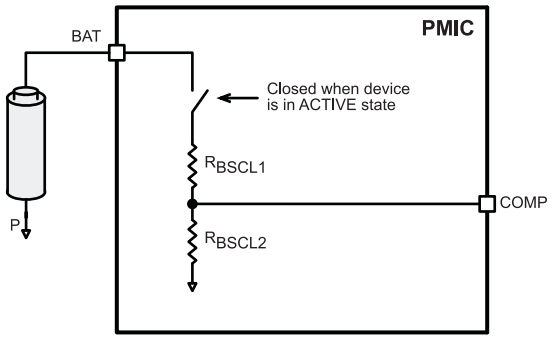


Figure 5-15. COMP Pin Internal Connection

Table 5-4. Scaling Resistors for COMP Pin Function (V_{VLDO} = 2.2 V)

SCALING RESISTORS FOR COMP PIN FUNCTION	VALUE
R_{BSCL1}	3.0 MΩ
R_{BSCL2}	2.36 MΩ

Table 5-5. Scaling Resistors for COMP Pin Function (V_{VLDO} = 3.0 V)

SCALING RESISTORS FOR COMP PIN FUNCTION	VALUE
R_{BSCL1}	3.0 MΩ
R_{BSCL2}	2.48 MΩ

Using the designed values in Table 5-4 or Table 5-5, the voltage on the COMP pin will be: V_{COMP} = 0.5 × V_{VLDO} + 300 mV. This ensures that the COMP pin voltage will be close to half of the LDO output voltage plus the LDO dropout voltage of the device. The COMP pin can also be used as the input to an ADC channel of an external microcontroller if additional accuracy or functionality is desired over a simple comparison.

5.3.6.3 SW_SEL Pin Functionality

The SW_SEL pin is used to select what type of switch is connected to the SWITCH pin of the device. Selection between a push-button and a slider switch can be made based on the state of this pin.

Table 5-6. SW_SEL Settings

SW_SEL STATE	TYPE OF SWITCH SELECTED
Low ($V_{SW\_SEL} < V_{IL(PMIC)}$)	Slider Switch
High ($V_{SW\_SEL} > V_{IH(PMIC)}$)	Push-button

When the push button switch type is selected, the device will debounce the SWITCH input with a 32-ms timer for both the ON and OFF events and either power on or off the device. Using the push-button switch function, the ON and OFF timings are equal; $t_{ON} = t_{OFF}$. If the system requirements are such that the on and off timings should be different, $t_{ON} \neq t_{OFF}$, then refer to the following section for the correct system setup: Section 6.2.1.2.3.When the slider switch operation is selected, the SWITCH pin must be externally pulled up to the SYS voltage with a resistor and the output connected to the slider switch. When the SWITCH pin is pulled to ground, the device will turn on and enter the power up sequence.

5.3.6.4 SWITCH Pin

The SWITCH pin behavior is defined by the SW_SEL pin (Section 5.3.6.3) which defines the type of switch that is connected to the system; either a slider switch or push-button.

5.3.6.5 Slider Switch Behavior

If a slider switch is connected in the system then the system power state and VLDO output (which can power an external MCU) is defined by the state of the slider switch. If the slider is in the *off* position than the SWITCH pin should be connected to the SYS pin. If the slider is in the *on* position than the SWITCH pin should be connected to ground. Figure 5-16 details the system operation using the slider switch configuration.

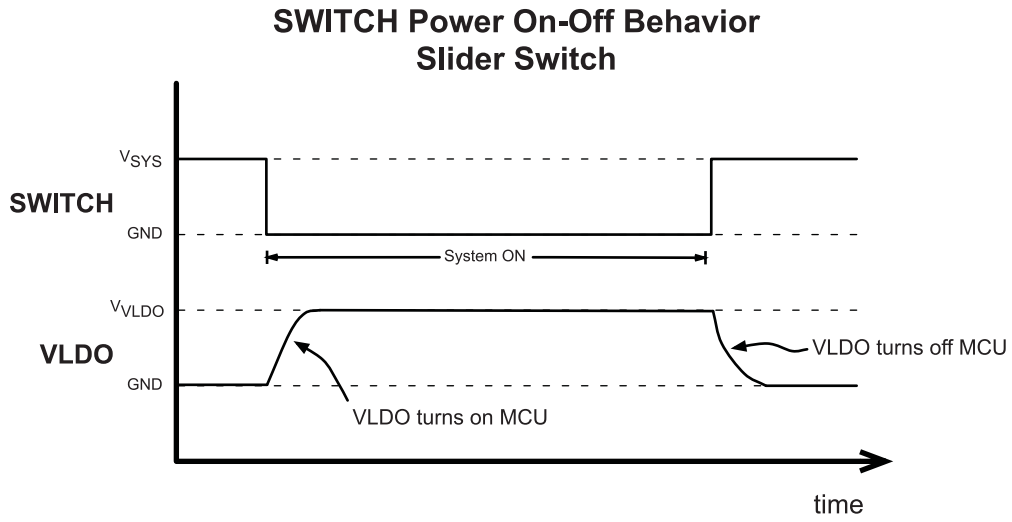


Figure 5-16. SWITCH, Slider Power On-Off Behavior

5.3.6.6 Push-Button Switch Behavior

The system is powered on or off by a push-button press after a press that is greater than 32 ms. The following figures (Figure 5-17 and Figure 5-18) show the system behavior and the expected VLDO output during the normal push-button operation where the ON and OFF press timings are the same value, $t_{ON} = t_{OFF}$.

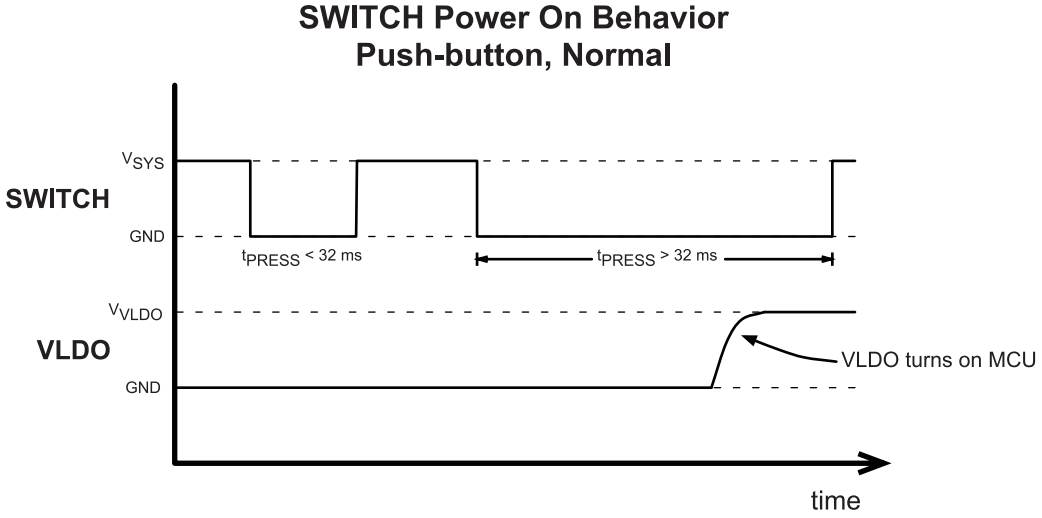


Figure 5-17. SWITCH, Push-button Power On Behavior

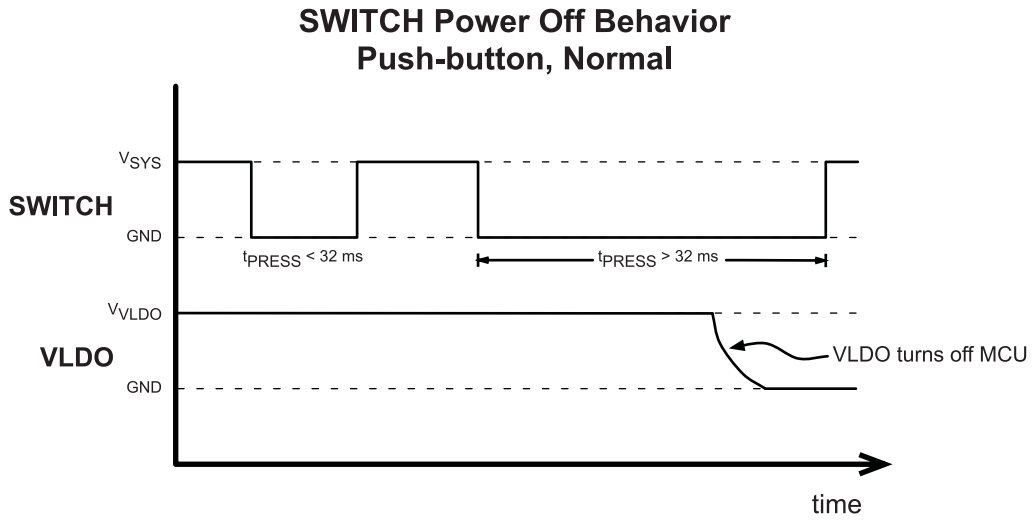


Figure 5-18. SWITCH, Push-Button Power Off Behavior

5.4 Device Functional Modes

5.4.1 SLEEP State

If the device is in the SLEEP State or Device IDLE mode, the Sleep control supervisor and the battery charger/power path remain active. The Boost and LDO are disabled.

5.4.2 NORMAL Operating Mode

Once the system completes the power up routine, it enters the normal operating mode. The specific system operation is set by the SW_SEL pin.

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

This PMIC is designed specifically for active shutter 3D glasses.

6.2 Typical Application

6.2.1 Active Shutter 3D Glasses

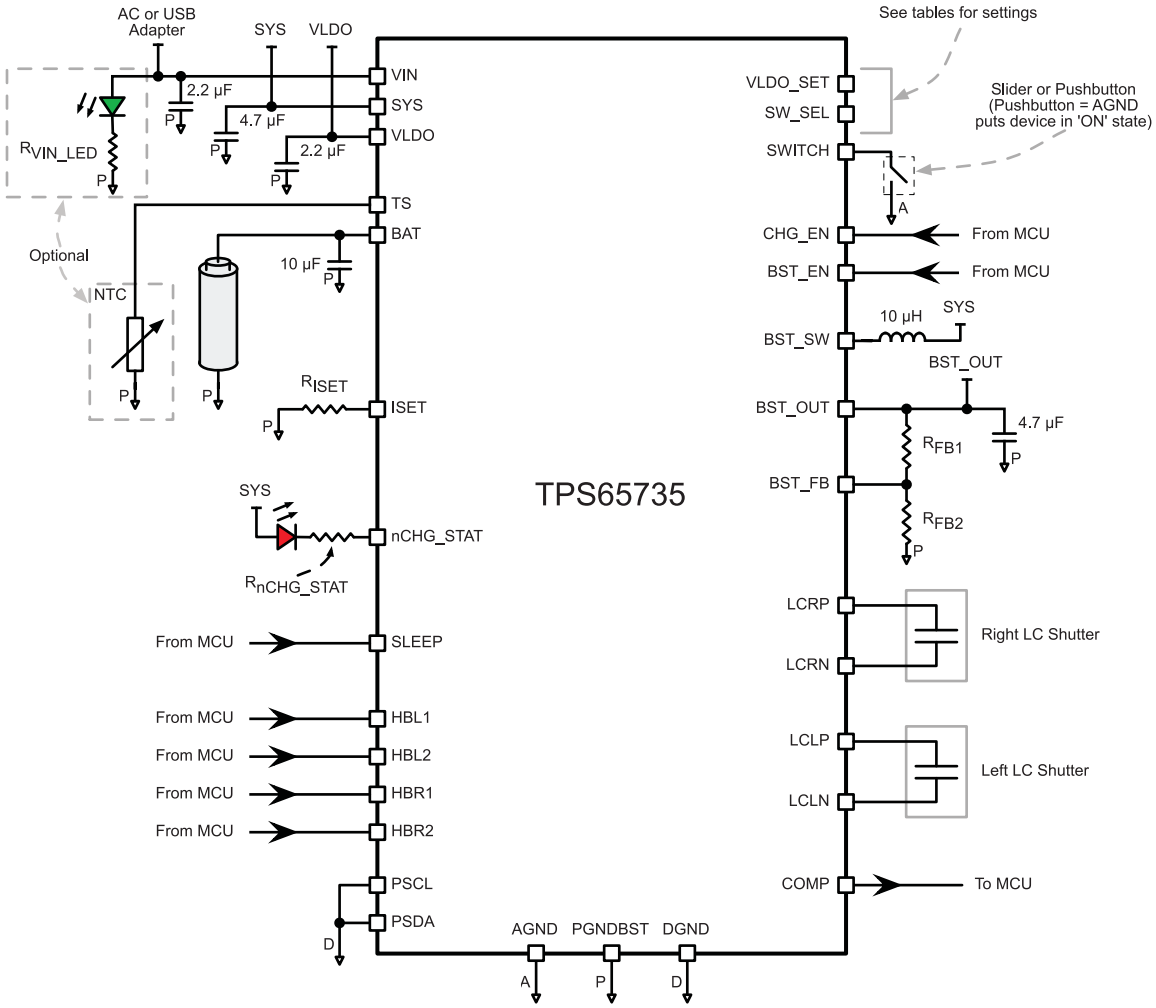


Figure 6-1. TPS65735 Applications Schematic

6.2.1.1 Design Requirements

The design parameters are located in Table 6-1.

Table 6-1. Design Parameters

PARAMETER	EXAMPLE
Input Voltage, V_{IN}	3.7 to 6.4 V
Input Voltage, Vbat BAT	2.5 to 6.4 V
Output Voltage, LDO VLDO	2.2 (default) or 3.0 V
Output Voltage Boost, BST_OUT	8 to 16 V, 10 V default
Charge Current Ichg=Kiset/Riset	5 to 100 mA, 70 mA default
Input Voltage Low V_{IL} (BST_EN, CHG_EN, SW_SEL, VLDO, HBRx, HBLx)	0.4 V
Input Voltage High V_{IH} (BST_EN, CHG_EN, SW_SEL, VLDO, HBRx, HBLx)	1.2 V

6.2.1.2 Detailed Design Procedure

6.2.1.2.1 Reducing System Quiescent Current (I_Q)

This PMU device has been optimized for low power applications. If an even lower quiescent current is desired, the following circuit and configuration can be utilized to reduce system off / sleep quiescent current further. Please note that this will cause a slight efficiency drop to the overall system due to the addition of the resistance of the FET that has been added. With this circuit, achieving an I_Q of less than 1 µA is possible. Please refer to the datasheet of the MCU used in the system to determine the system I_Q that is possible.

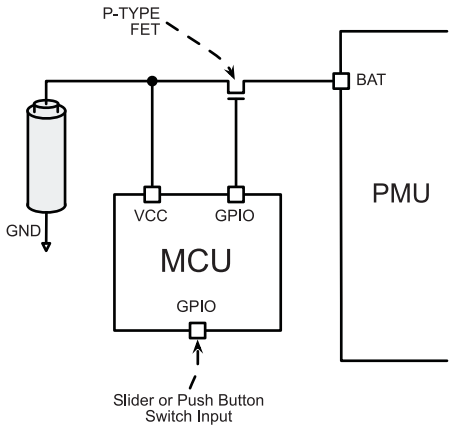


Figure 6-2. Reducing System I_Q with Addition of a FET

Along with this system configuration, the MCU code must be written such that the MCU sits in the lowest power state that can support an interrupt on a GPIO from a switch (slider or push button). After a valid button press or switch action, the device can begin the power on sequence and open the FET in the previous figure (Figure 6-2). This will allow power flow into the PMU and the system can then operate normally.

6.2.1.2.2 Boost Converter Application Information

6.2.1.2.2.1 Setting Boost Output Voltage

To set the boost converter output voltage of this device, two external resistors that form a feedback network are required. The values recommended below (in Table 6-2) are given for a desired quiescent current of 5 µA when the boost is enabled and switching. See Figure 6-3 for the detail of the applications schematic that shows the boost feedback network and the resistor names used in the table below.

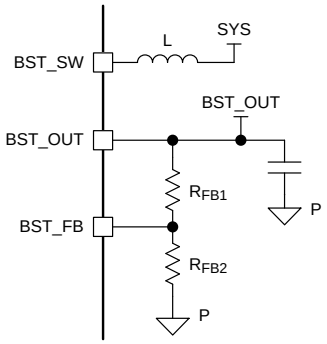


Figure 6-3. Boost Feedback Network Schematic

Table 6-2. Recommended R_{FB1} and R_{FB2} Values (for $I_{Q(FB)}$ = 5 µA)

TARGETED V_{BST_OUT}	R_{FB1} (1)	R_{FB2} (1)
8 V	1.3 MΩ	240 kΩ
10 V	1.8 MΩ	240 kΩ
12 V	2.2 MΩ	240 kΩ
14 V	2.4 MΩ	240 kΩ
16 V	3.0 MΩ	240 kΩ

(1) Resistance values given in closest standard value (5% tolerance, E24 grouping).

These resistance values can also be calculated using the following information. To start, it is helpful to target a quiescent current through the boost feedback network while the device is operating ($I_{Q(FB)}$). When the boost output voltage and this targeted quiescent current is known, the total feedback network resistance can be found.

The value for R_{FB2} can be found by using the boost feedback pin voltage (V_{FB} = 1.2 V, see *Section 4.6*) and $I_{Q(FB)}$ using Equation 1:

$$R_{FB1} + R_{FB2} = V_{BST\_OUT} / I_{Q(FB)} \quad (1)$$

$$R_{FB2} = (1.2\ V) / I_{Q(FB)} \quad (2)$$

To find R_{FB1}, simply subtract the R_{FB2} from $R_{FB(TOT)}$ as shown in Equation 3.

$$R_{FB1} = R_{FB(TOT)} - R_{FB2} \quad (3)$$

6.2.1.2.2.2 Boost Inductor Selection

The selection of the boost inductor and output capacitor is very important to the performance of the boost converter. The boost has been designed for optimized operation when a 10 µH inductor is used. Smaller inductors, down to 4.7 µH, may be used but there will be a slight loss in overall operating efficiency. A few inductors that have been tested and found to give good performance can be found in the following list.

Recommended 10-µH inductors:

- TDK VLS201612ET-100M (10 µH, I_{MAX} = 0.53 A, R_{DC} = 0.85 Ω)
- Taiyo Yuden CBC2016B100M (10 µH, I_{MAX} = 0.41 A, R_{DC} = 0.82 Ω)

6.2.1.2.2.3 Boost Capacitor Selection

The recommended minimum value for the capacitor on the boost output, BST_OUT pin, is 4.7 µF. Values that are larger can be used with the measurable impact being a slight reduction in the boost converter output voltage ripple while values smaller than this will result in an increased boost output voltage ripple. Note that the voltage rating of the capacitor should be sized for the maximum expected voltage at the BST_OUT pin.

6.2.1.2.3 Bypassing Default Push-Button SWITCH Functionality

If the SWITCH pin functionality is not required to power on and off the device because of different system requirements (when the SWITCH timing requirements of system will be controlled by an external microcontroller), then the feature can be bypassed. The following diagram shows the connections required for this configuration, note that INT. I/O refers to an interruptible I/O on the microcontroller.

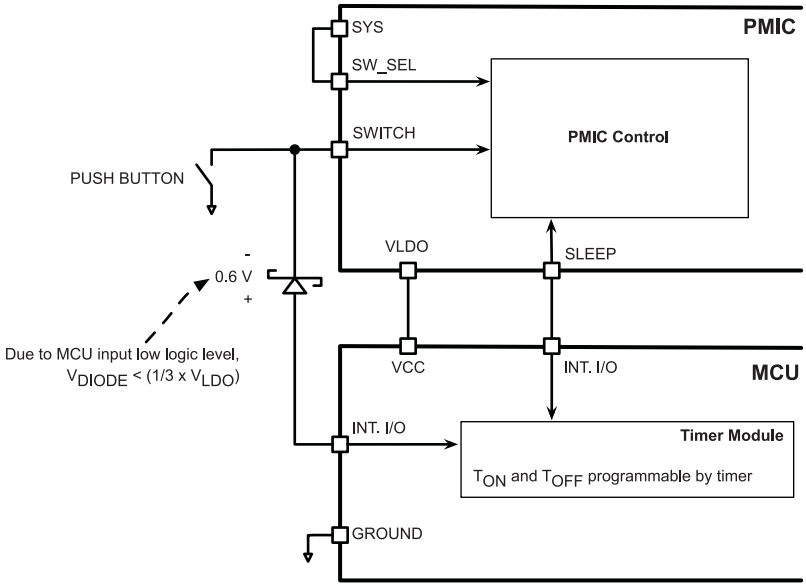


Figure 6-4. Bypassing Default TPS65735 Push Button SWITCH Timing

In a system where a different push-button SWITCH off timing is required, the SLEEP pin is used to control the power off of the device. After system power up, the MCU must force the SLEEP pin to a high state (V_{SLEEP} > $V_{IH(PMIC)}$). Once the SWITCH push-button is pressed to shut the system down, a timer in the MCU should be active and counting the desired t_{OFF} time of the device. Once this t_{OFF} time is detected, the MCU can assert the SLEEP signal to a logic low level (V_{SLEEP} < $V_{IL(PMIC)}$). It is on the falling edge of the SLEEP signal where the system will be powered off (see Figure 6-5).

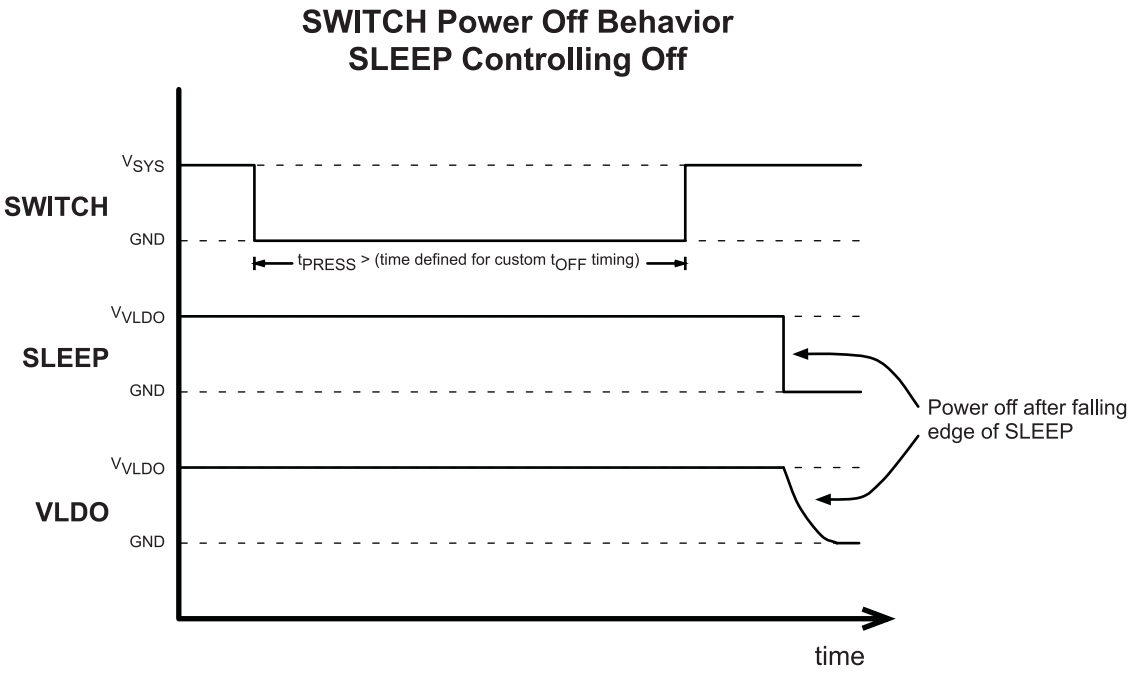
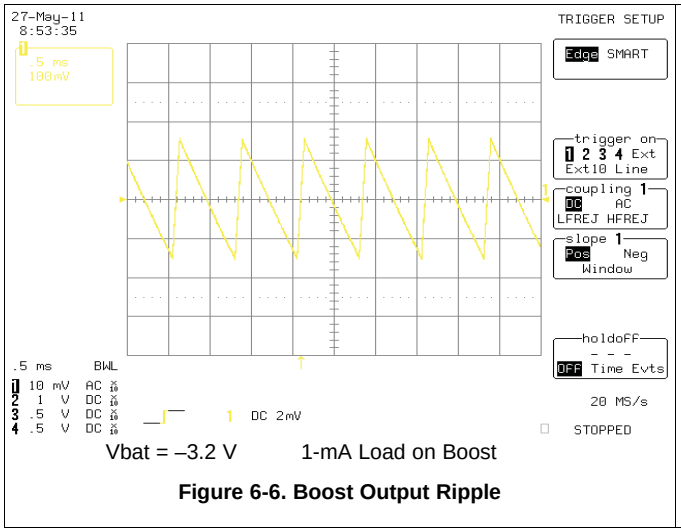


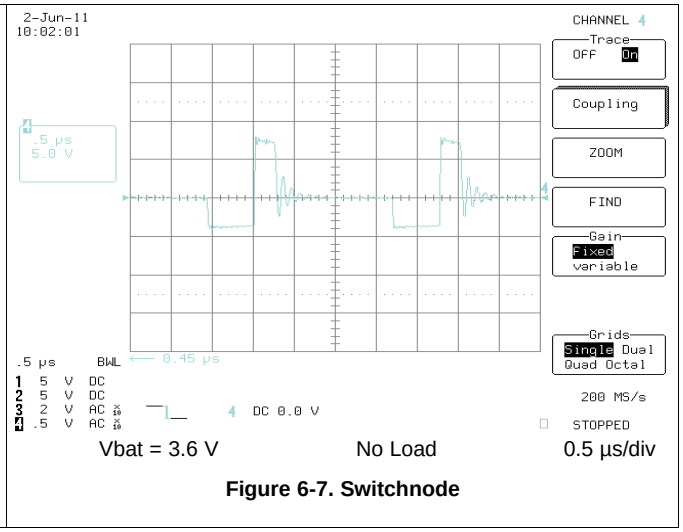
Figure 6-5. SWITCH Press and SLEEP Signal to Control System Power Off

6.2.1.3 Application Curves



Vbat = –3.2 V 1-mA Load on Boost

Figure 6-6. Boost Output Ripple



Vbat = 3.6 V No Load 0.5 µs/div

Figure 6-7. Switchnode

7 Power Supply Recommendations

An DC Input Voltage range of 3.7 to 6.4 V is required on V_{IN} and a range of 2.5 V to 6.4 V is required on BAT.

V_{IN} requires a 2.2-µF capacitor.

SYS requires a 4.7-µF capacitor.

BAT requires a 10-µF capacitor.

VLDO requires a 2.2-µF capacitor.

8 Layout

8.1 Layout Guidelines

The layout is an important step in the design process. Proper function of the device demands careful attention to the PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor performance including stability issues as well as EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Keep the common path to the ground pins which return the small signal components and the high current of the output capacitors as short as possible in order to avoid ground noise.

8.2 Layout Example

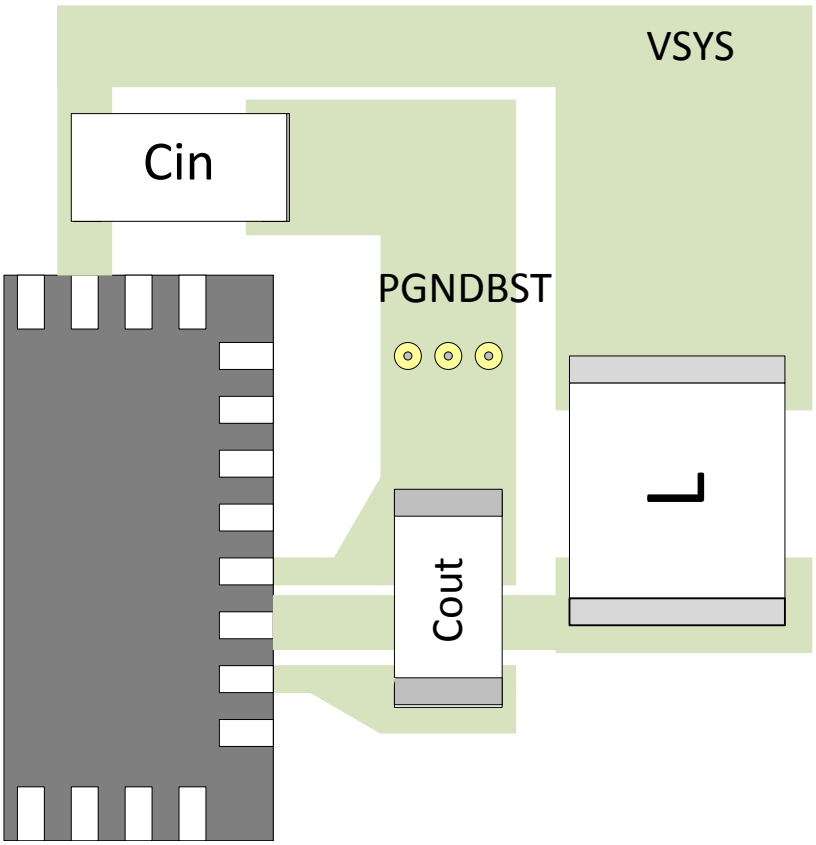


Figure 8-1. Boost Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65735RSNR	NRND	QFN	RSN	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65735	
TPS65735RSNT	PREVIEW	QFN	RSN	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65735	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

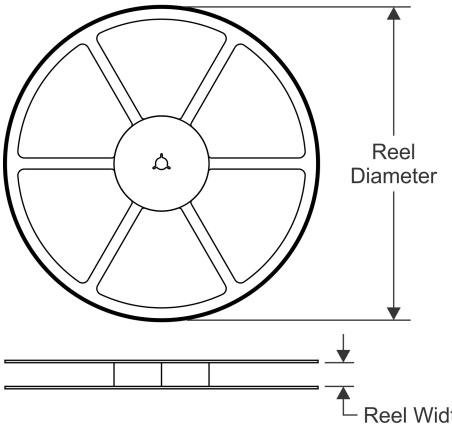
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

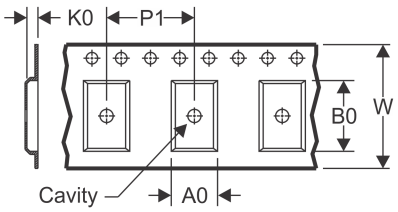
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

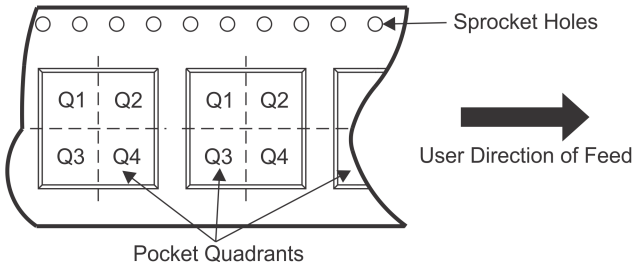


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

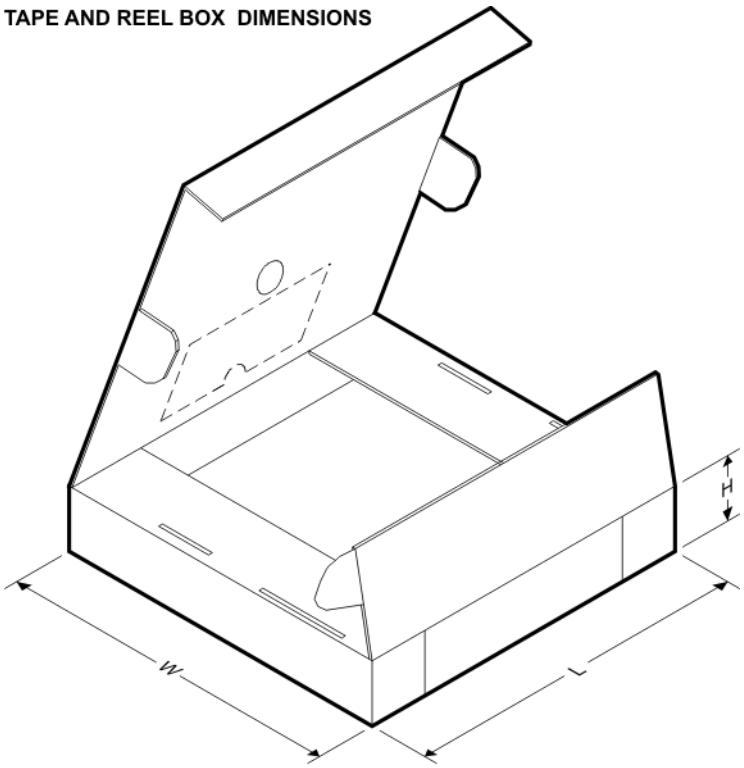
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65735RSNR	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

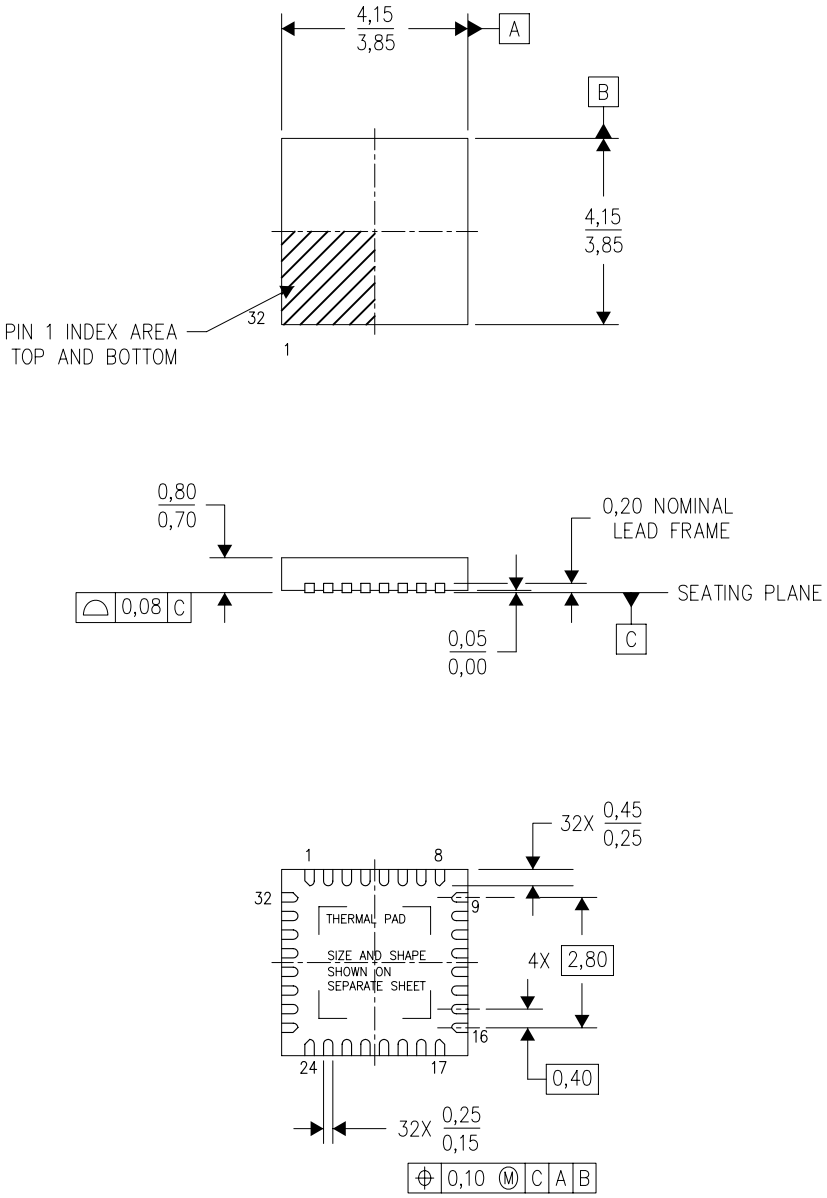
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65735RSNR	QFN	RSN	32	3000	552.0	367.0	36.0

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207561/C 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

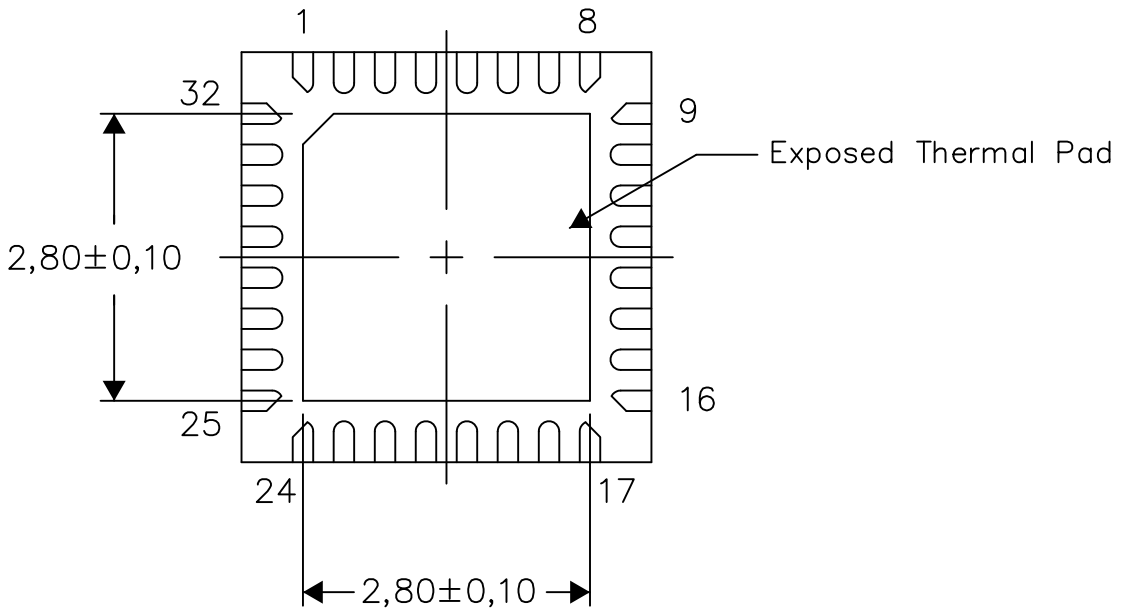
RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



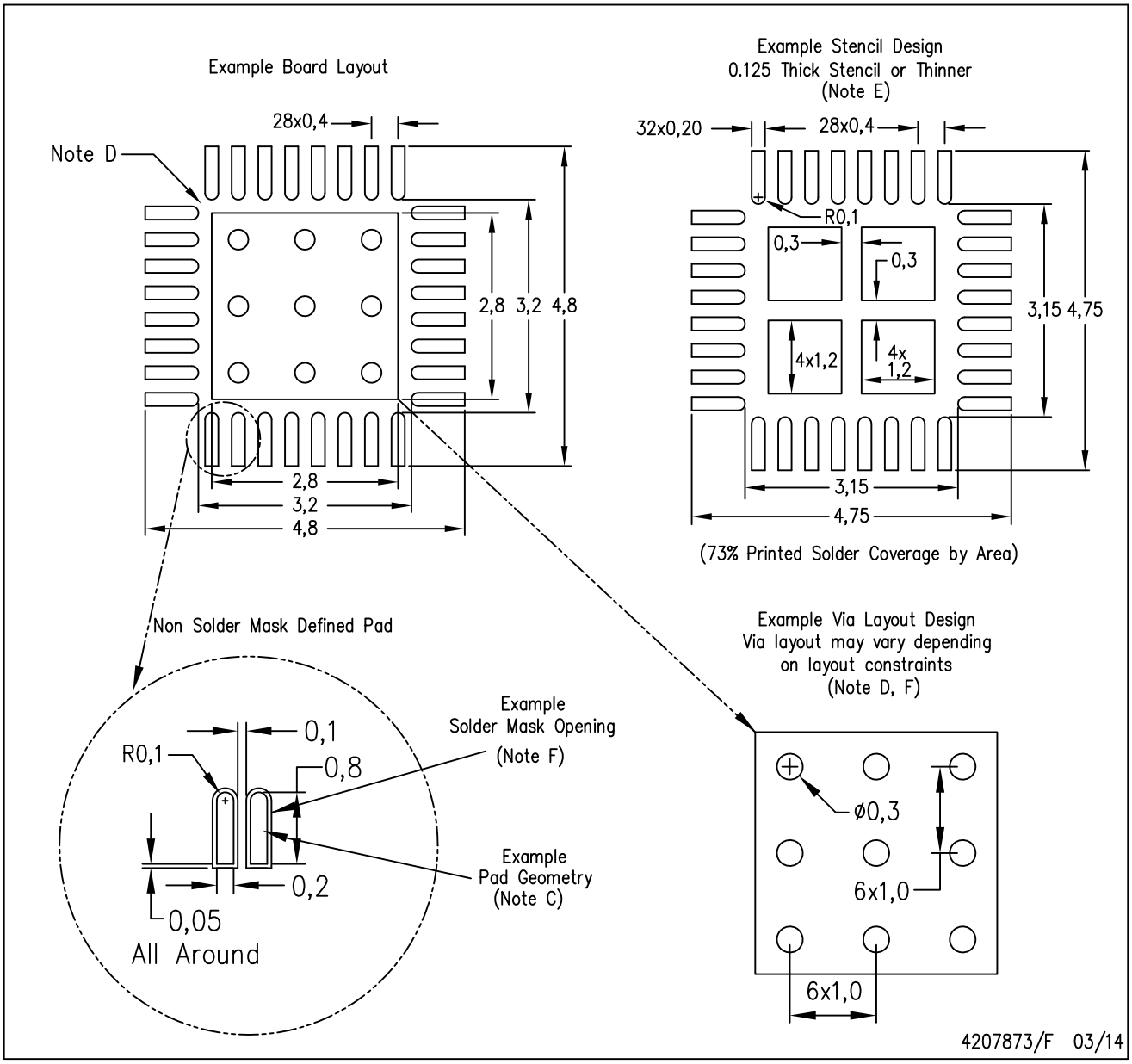
Bottom View

Exposed Thermal Pad Dimensions

4209775–2/F 03/14

NOTE: All linear dimensions are in millimeters

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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