TPS51200-Q1 Sink and Source DDR Termination Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Input Voltage: Supports 2.5-V Rail and 3.3-V Rail
- VLDOIN Voltage Range: 1.1 V to 3.5 V
- Sink/Source Termination Regulator Includes Droop Compensation
- Requires Minimum Output Capacitance of 20-µF (typically 3 × 10-µF MLCCs) for Memory Termination Applications (DDR)
- PGOOD to Monitor Output Regulation
- EN Input
- REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Remote Sensing (VOSNS)
- ±10-mA Buffered Reference (REFOUT)
- Built-in Soft Start, UVLO and OCL
- Thermal Shutdown
- Meets DDR, DDR2 JEDEC Specifications; Supports DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT Applications
- VSON-10 Package With Exposed Thermal Pad

2 Applications

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low Power DDR3 and DDR4
- Notebook, Desktop, Server
- Telecom and Datacom, GSM Base Station, LCD-TV and PDP-TV, Copier and Printer, Set-Top Box

3 Description

The TPS51200-Q1 device is a sink and source double-data-rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The TPS51200-Q1 device maintains a fast transient response and only requires a minimum output capacitance of 20 µF. The TPS51200-Q1 device supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low Power DDR3 and DDR4 VTT bus termination.

In addition, the TPS51200-Q1 device provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The TPS51200-Q1 device is available in the thermally-efficient VSON-10 package, and is rated both green and Pb-free. The device is specified from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51200-Q1	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Standard DDR Application

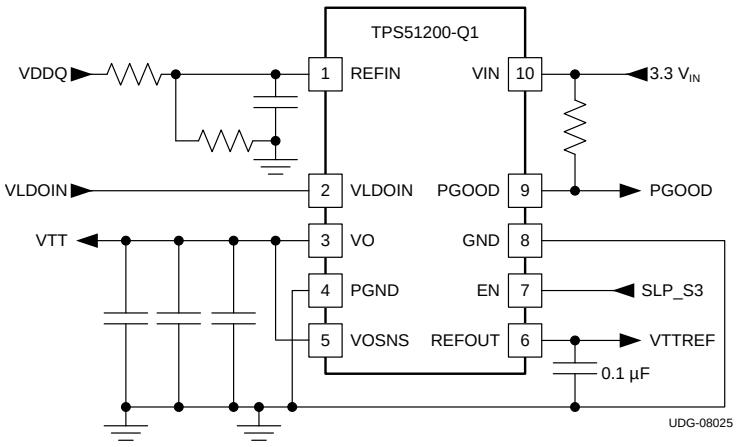


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2015) to Revision C — **Page**

- Changed pinout diagram for compatibility with HTML versioin of the data sheet ... 3
- Added REFOUT specification for –1 mA ≤ I_{REFOUT} ≤ 1 mA, condition ... 5
- Corrected Typical Characteristics condition statement ... 7
- Added Figure 4 ... 7
- Added Figure 9 ... 8
- Added *Receiving Notification of Documentation Updates* sectiion ... 29

Changes from Revision A (April 2012) to Revision B — **Page**

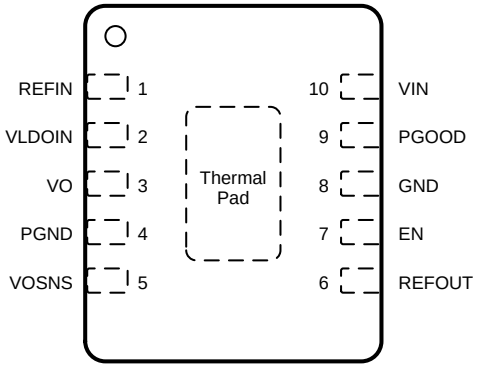
- Added AEC-Q100 test guidance results for temperature grade and HBM and CDM classifications to *Features* list ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Replaced references to PowerPAD with thermal pad ... 1
- Deleted *ORDERING INFORMATION* table ... 3
- Deleted *DISSIPATION RATINGS TABLE* ... 4
- Changed the thermal metric parameters in the *Thermal Information* table ... 4
- Changed the test conditions for REFOUT source and sink current limits in the *Electrical Characteristics* table ... 5
- Added -Q1 to device name throughout text of document ... 24

Changes from Original (November 2009) to Revision A — **Page**

- Added thermal table information for DRC package. ... 4

5 Pin Configuration and Functions

DRC Package
10-Pin VSON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	7	I	For DDR VTT application, connect EN to SLP_S3. For any other applications, use EN as the ON/OFF function. Keep EN voltage equal or lower than VIN voltage at all times.
GND	8	—	Ground. Signal ground. Connect to negative pin of the output capacitor.
PGND(1)	4	—	Power ground output for the LDO
PGOOD	9	O	PGOOD output. Open drain pin. Indicates regulation.
REFIN	1	I	Reference input
REFOUT	6	O	Reference output. Connect to GND through 0.1-μF ceramic capacitor. If there is REFOUT capacitor at DDR side, keep the total capacitance on REFOUT pin below 1 μF. The REFOUT pin can not be open.
VIN	10	I	2.5-V or 3.3-V power supply A ceramic decoupling capacitor with a value between 1-μF and 4.7-μF is required.
VLDOIN	2	I	Supply voltage for the LDO
VO	3	O	Power output for the LDO. Minimum 20-μF capacitance is required. No maximum capacitance limit.
VOSNS	5	I	Voltage sense output for the LDO. Connect to positive pin of the output capacitor or the load.

(1) Thermal pad connection. See Figure 34 in the *Thermal Considerations* section for additional information.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Input voltage(2)	VIN, VLDOIN, VOSNS, REFIN	–0.3	3.6	V
	EN	–0.3	6.5	
	PGND to GND	–0.3	0.3	
Output voltage(2)	VO, REFOUT	–0.3	3.6	V
	PGOOD	–0.3	6.5	
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin unless otherwise noted.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply voltage	VIN	2.375	3.500	V
Voltage range	EN, VLDOIN, VOSNS	–0.1	3.5	
	REFIN	0.5	1.8	
	VO, PGOOD	–0.1	3.5	
	REFOUT	–0.1	1.8	
	PGND	–0.1	0.1	
Operating free-air temperature, T_A		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS51200-Q1 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	63.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	16.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended free-air temperature range, V_{VIN} = 3.3 V, V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in the *Standard DDR Application* section (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	Supply current	T_A = 25 °C, V_{EN} = 3.3 V, No Load		0.7	1	mA
$I_{IN(SDN)}$	Shutdown current	T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} = 0, No Load		65	80	µA
		T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} > 0.4 V, No Load		200	400	
I_{LDOIN}	Supply current ofVLDOIN	T_A = 25 °C, V_{EN} = 3.3 V, No Load		1	50	µA
$I_{LDOIN(SDN)}$	Shutdown current of VLDOIN	T_A = 25 °C, V_{EN} = 0 V, No Load		0.1	50	µA
INPUT CURRENT						
I_{REFIN}	Input current, REFIN	V_{EN} = 3.3 V			1	µA
VO OUTPUT						
V_{VOSNS}	Output DC voltage, VO	V_{REFOUT} = 1.25 V (DDR1), I_O = 0 A		1.25		V
			–15		15	mV
		V_{REFOUT} = 0.9 V (DDR2), I_O = 0 A		0.9		V
			–15		15	mV
		V_{REFOUT} = 0.75 V (DDR3), I_O = 0 A		0.75		V
			–15		15	mV
		V_{REFOUT} = 0.675 V (DDR3L), I_O = 0 A		0.675		V
			-15		15	mV
		V_{REFOUT} = 0.6 V (DDR4), I_O = 0 A		0.6		V
			-15		15	mV
V_{VOTOL}	Output voltage tolerance to REFOUT	–2A < I_{VO} < 2A	–25		25	mV
I_{VOSRCL}	VO source vurrent Limit	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}	3		4.5	A
I_{VOSNCL}	VO sink current Limit	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}	3.5		5.5	A
I_{DSCHRG}	Discharge current, VO	V_{REFIN} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V, T_A = 25°C		18	25	Ω
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	VO PGOOD threshold	PGOOD window lower threshold with respect to REFOUT	–23.5%	–20%	–17.5%	
		PGOOD window upper threshold with respect to REFOUT	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA			0.4	V
$I_{PGOODLK}$	Leakage current(1)	V_{OSNS} = V_{REFIN} (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V			1	µA
REFIN AND REFOUT						
V_{REFIN}	REFIN voltage range		0.5		1.8	V
$V_{REFINUVLO}$	REFIN undervoltage lockout	REFIN rising	360	390	420	mV
$V_{REFINUVHYS}$	REFIN undervoltage lockout hysteresis			20		mV
V_{REFOUT}	REFOUT voltage			REFIN		V
$V_{REFOUTTOL}$	REFOUT voltage tolerance to V_{REFIN}	–10 mA ≤ I_{REFOUT} ≤ 10 mA, 0.6 V ≤ V_{REFIN} ≤ 1.25 V	–15		15	mV
		–1 mA ≤ I_{REFOUT} ≤ 1 mA, 0.6 V ≤ V_{REFIN} ≤ 1.25 V	–12		12	
$I_{REFOUTSRCL}$	REFOUT source current limit	V_{REFOUT} = 0.5 V	10	40		mA
$I_{REFOUTSNCL}$	REFOUT sink current limit	V_{REFOUT} = 1.5 V	10	40		mA
UVLO / EN LOGIC THRESHOLD						
$V_{VINUVVIN}$	UVLO threshold	Wake up, T_A = 25°C	2.2	2.3	2.375	V
		Hysteresis		50		mV
V_{ENIH}	High-level input voltage	Enable	1.7			V
V_{ENIL}	Low-level input voltage	Enable			0.3	V
V_{ENYST}	Hysteresis voltage	Enable		0.5		V
I_{ENLEAK}	Logic input leakage current	EN, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SON}	Thermal shutdown threshold(1)	Shutdown temperature		150		°C
		Hysteresis		25		

(1) Ensured by design. Not production tested.

6.6 Switching Characteristics

Over recommended free-air temperature range, V_{VIN} = 3.3 V,V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in the *Standard DDR Application* section (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWERGOOD COMPARATOR						
$T_{PGSTUPDLY}$	PGOOD startup delay	Startup rising edge, VOSNS within 15% of REFOUT		2		ms
$T_{PBADDLY}$	PGOOD bad delay	VOSNS is outside of the ±20% PGOOD window		10		µs

6.7 Typical Characteristics

For Figure 1 through Figure 18, 3 × 10-µF MLCCs (0805) are used on the output.

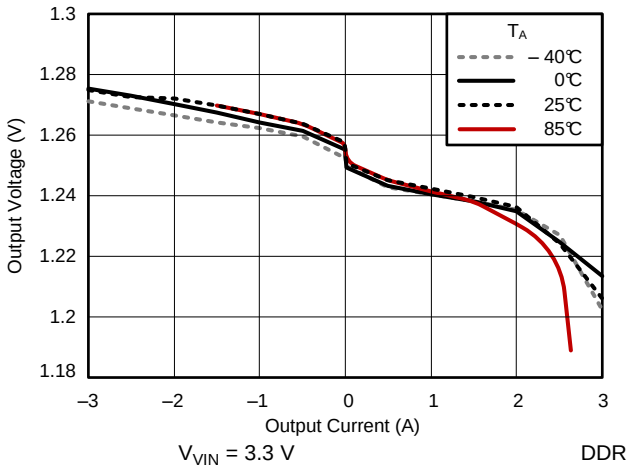


Figure 1. Output Voltage vs Output Current

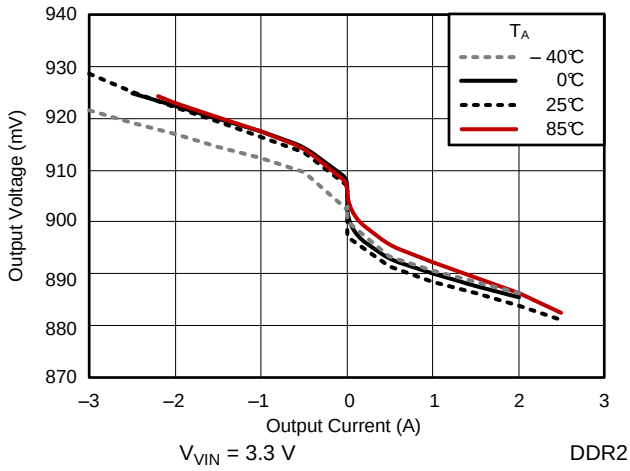


Figure 2. Output Voltage vs Output Current

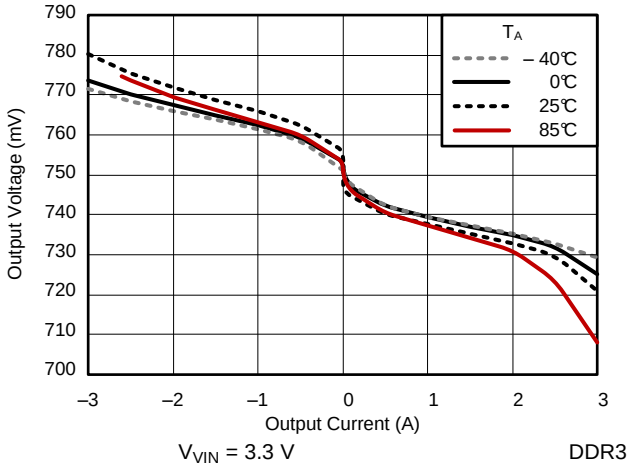


Figure 3. Output Voltage vs Output Current

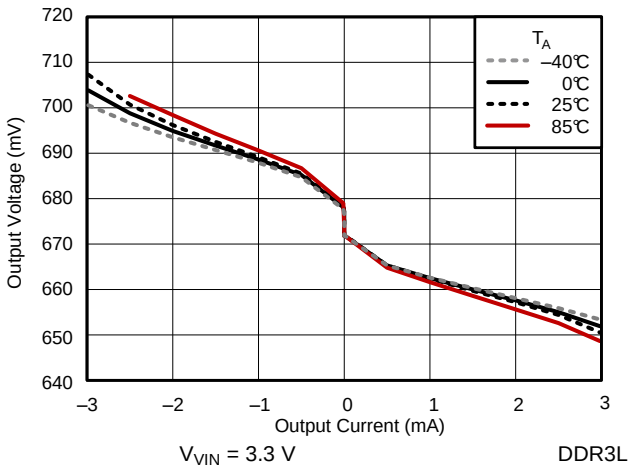


Figure 4. Output Voltage vs Output Current

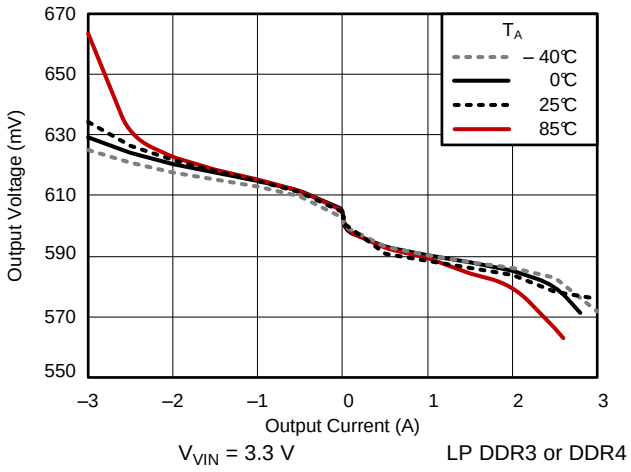


Figure 5. Output Voltage vs Output Current

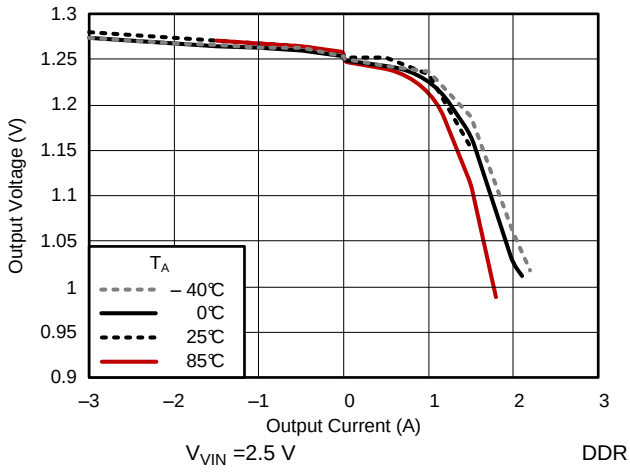


Figure 6. Output Voltage vs Output Current

Typical Characteristics (continued)

For Figure 1 through Figure 18, 3 × 10-µF MLCCs (0805) are used on the output.

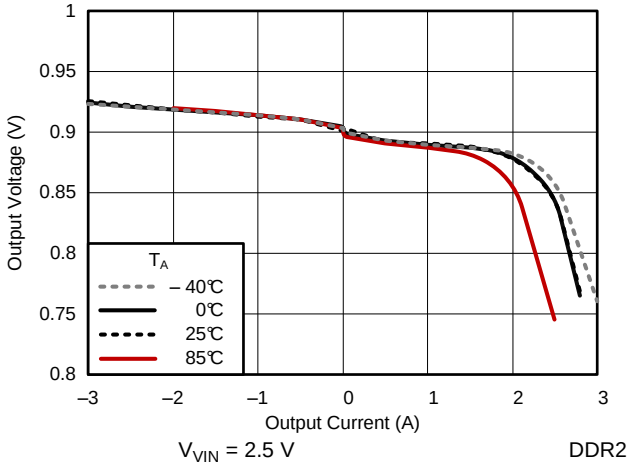


Figure 7. Output Voltage vs Output Current

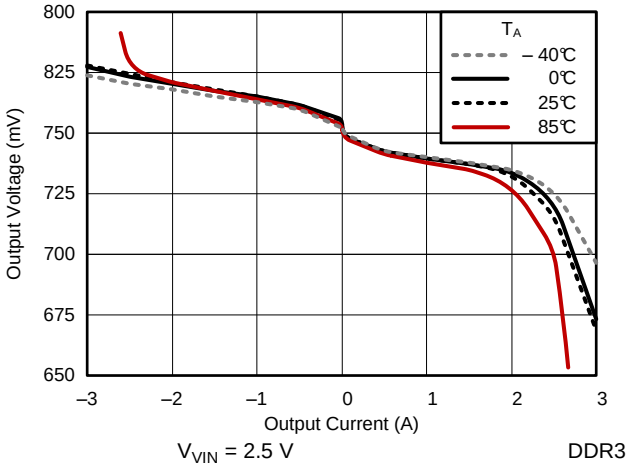


Figure 8. Output Voltage vs Output Current

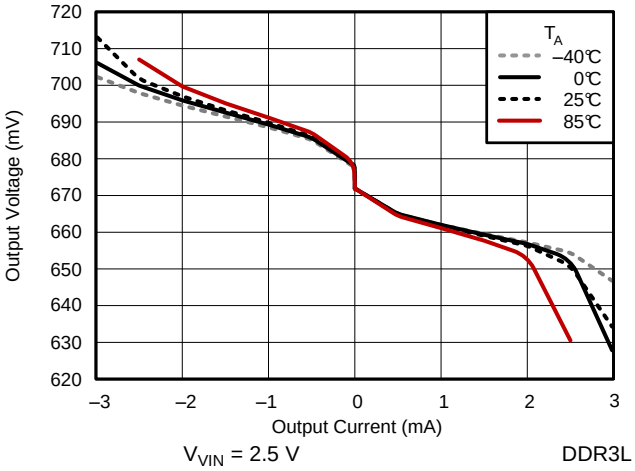


Figure 9. Output Voltage vs Output Current

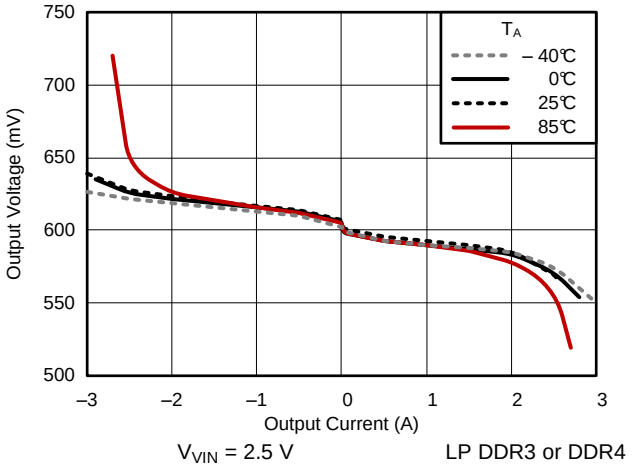


Figure 10. Output Voltage vs Output Current

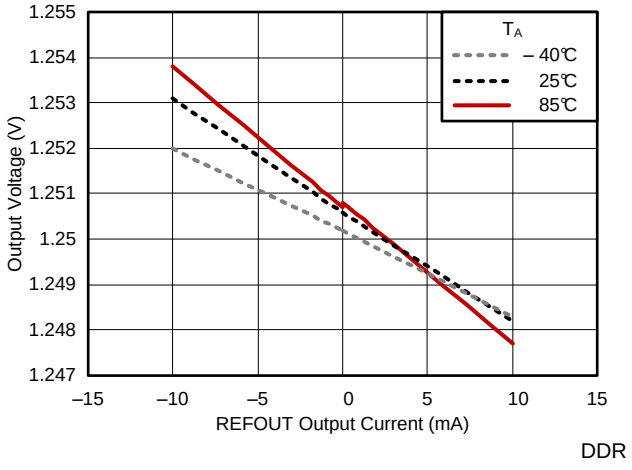


Figure 11. REFOUT Line Regulation

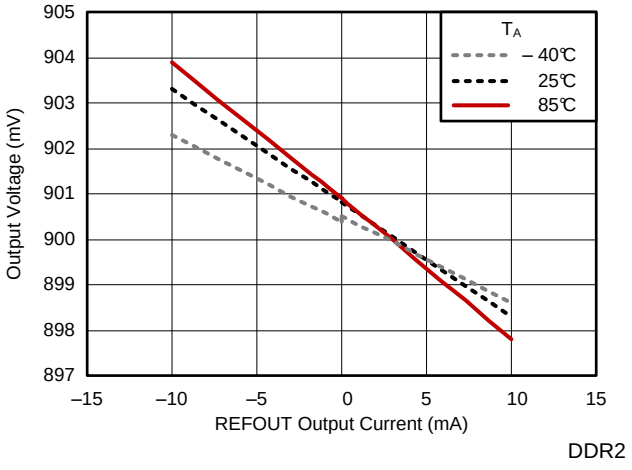


Figure 12. REFOUT Line Regulation

Typical Characteristics (continued)

For Figure 1 through Figure 18, 3 × 10-µF MLCCs (0805) are used on the output.

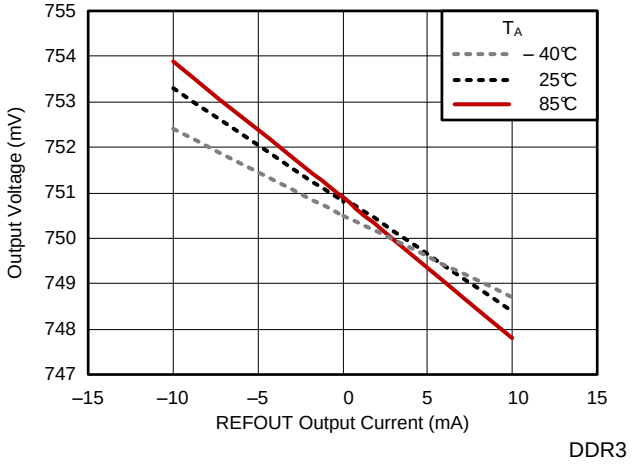


Figure 13. REFOUT Line Regulation

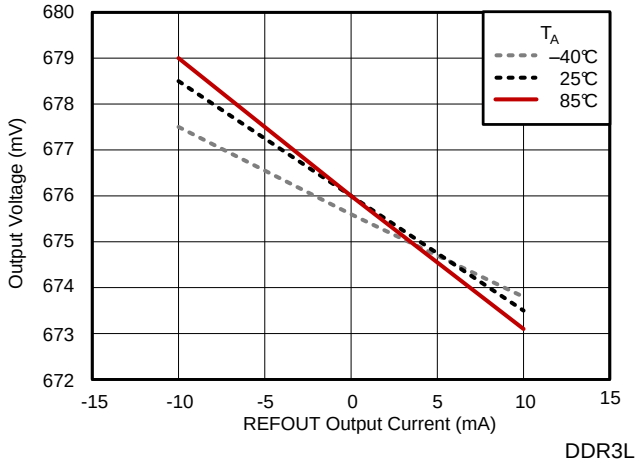


Figure 14. REFOUT Line Regulation

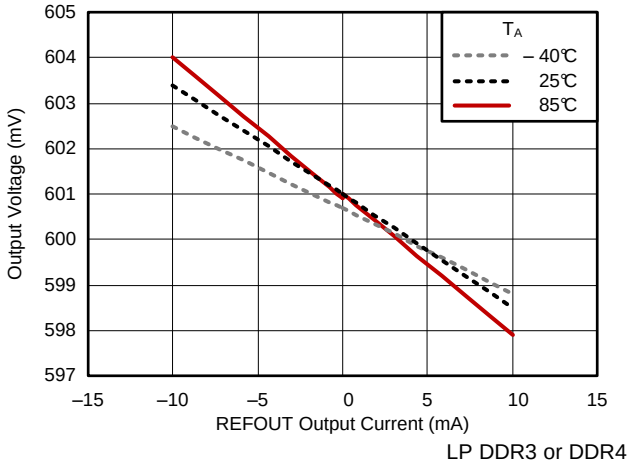


Figure 15. REFOUT Line Regulation

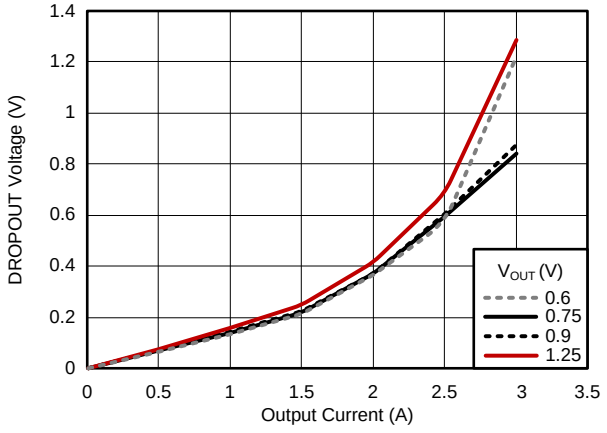


Figure 16. DROPOUT Voltage vs Output Current

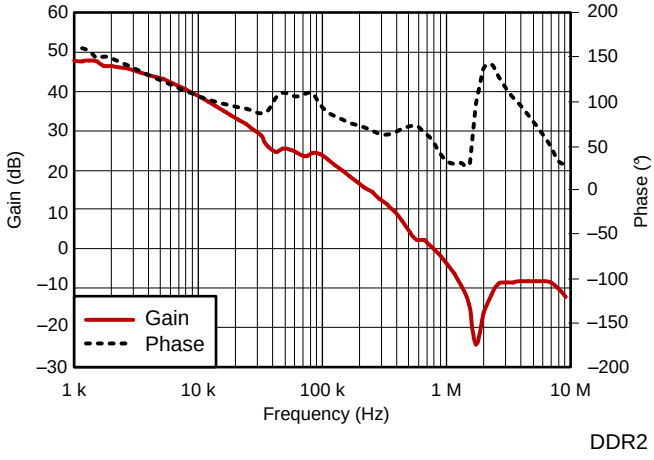


Figure 17. Gain and Phase vs Frequency

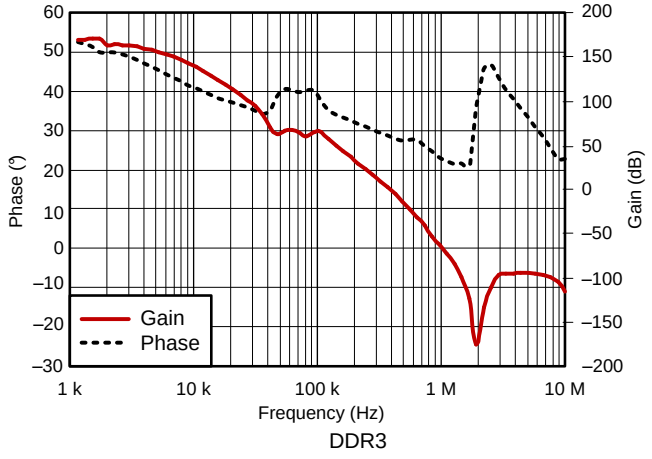


Figure 18. Gain and Phase vs Frequency

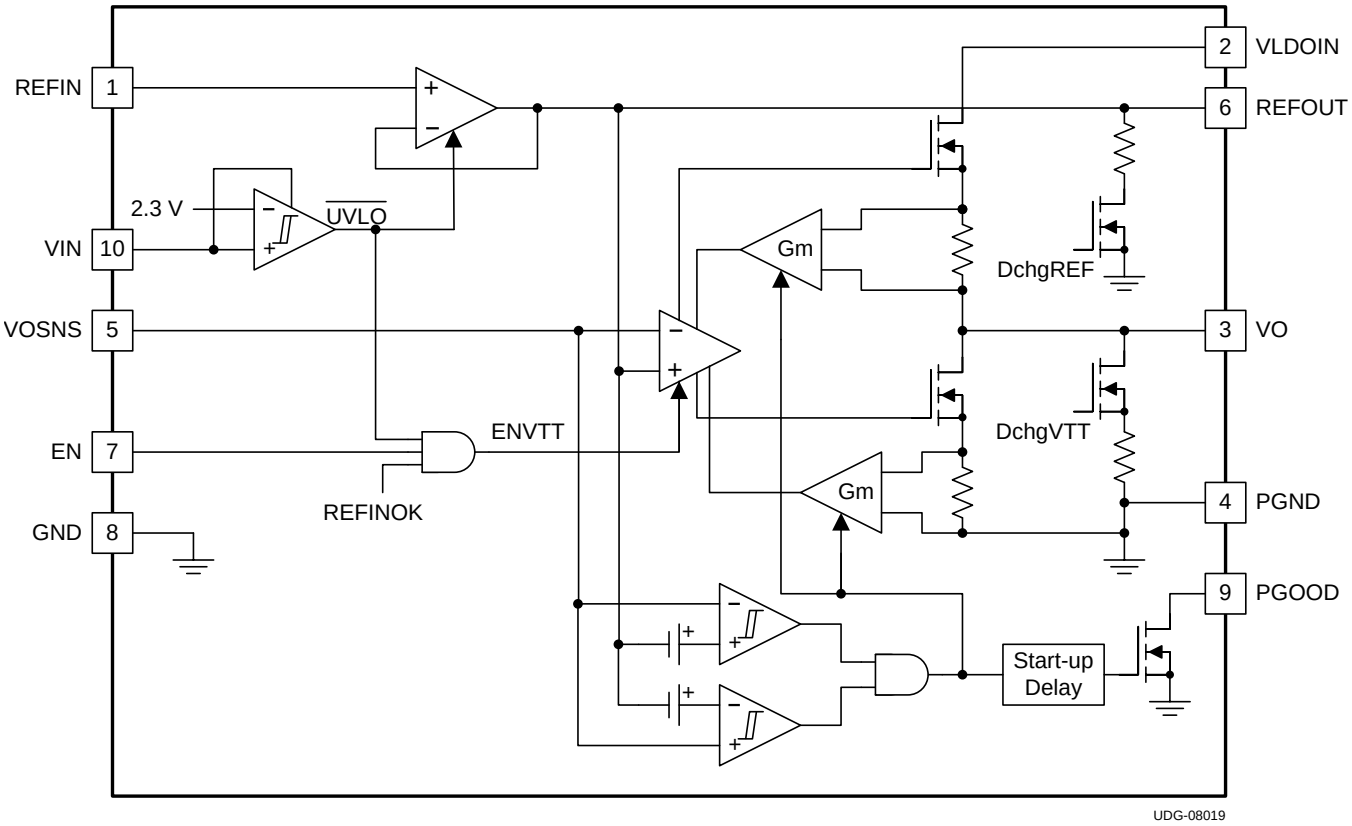
7 Detailed Description

7.1 Overview

The TPS51200-Q1 device is a sink and source, double data-rate (DDR) termination regulator specifically designed for low-input voltage, low-cost, and low-noise systems where space is a key consideration.

The TPS51200-Q1 device is designed to provide proper termination voltage and a 10-mA buffered reference voltage for DDR memory which includes the following DDR specifications (core voltage, reference voltage) with minimal external components: DDR (2.5 V, 1.25 V), DDR2 (1.8 V, 0.9 V), DDR3 (1.5 V, 0.75 V), DDR3L (1.35 V, 0.675 V), LP DDR3 and DDR4 (1.2 V, 0.6 V).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Sink and Source Regulator (VO Pin)

The TPS51200-Q1 device is a sink and source (sink/source) tracking termination regulator specifically designed for low input voltage, low-cost, and low external-component count systems where space is a key application parameter. The TPS51200-Q1 device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin, VOSNS, must be connected to the positive pin of the output capacitors as a separate trace from the high current path from the VO pin.

7.3.2 Reference Input (REFIN Pin)

The output voltage, V_O, is regulated to the REFOUT pin. When the REFIN pin is configured for standard DDR termination applications, the REFIN pin can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The TPS51200-Q1 device supports the REFIN voltage from 0.5 V to 1.8 V, making the device versatile and ideal for many types of low-power LDO applications.

Feature Description (continued)

7.3.3 Reference Output (REFOUT Pin)

When the device is configured for DDR termination applications, the REFOUT pin generates the DDR VTT reference voltage for the memory application. The device is capable of supporting both a sourcing and sinking load of 10 mA. The REFOUT pin becomes active when the REFIN voltage rises to 0.390 V and the VIN pin is above the UVLO threshold. When the REFOUT pin is less than 0.375 V, it is disabled and subsequently discharges to the GND pin through an internal 10-kΩ MOSFET. The REFOUT pin is independent of the EN pin state.

7.3.4 Soft-Start Sequencing

The soft-start function of the VO pin is achieved through a current clamp. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When the VO pin is outside of the powergood window, the current clamp level is one-half of the full overcurrent limit (OCL) level. When the VO pin rises or falls within the PGOOD window, the current clamp level switches to the full OCL level. The soft-start function is completely symmetrical and works not only from GND to the REFOUT voltage, but also from the VLDOIN pin to the REFOUT voltage.

7.3.5 Enable Control (EN Pin)

When the EN pin is driven high, the TPS51200-Q1 VO-regulator begins normal operation. When the EN pin is driven low, the VO pin discharges to the GND pin through an internal 18-Ω MOSFET. The REFOUT pin remains on when the EN pin is driven low.

7.3.6 Powergood Function (PGOOD Pin)

The TPS51200-Q1 device provides an open-drain PGOOD output that goes high when the VO output is within ±20% of the REFOUT pin. The PGOOD pin deasserts within 10 μs after the output exceeds the size of the powergood window. During initial VO startup, the PGOOD pin asserts high 2 ms (typ) after the VO pin enters power good window. Because the PGOOD pin is an open-drain output, a 100-kΩ, pullup resistor between the PGOOD pin and a stable active supply voltage rail is required.

7.3.7 Current Protection (VO Pin)

The LDO has a constant overcurrent limit (OCL). Note that the OCL level reduces by one-half when the output voltage is not within the powergood window. This reduction is a non-latch protection.

7.3.8 UVLO Protection (VIN Pin)

For the VIN undervoltage-lockout (UVLO) protection, the TPS51200-Q1 device monitors the VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

7.3.9 Thermal Shutdown

The TPS51200-Q1 device monitors the junction temperature. If the device junction temperature exceeds the threshold value, (typically 150°C), the VO and REFOUT regulators are both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

7.4 Device Functional Modes

The TPS51200-Q1 device can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. The TPS51200-Q1 minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

7.4.1 S3 and Pseudo-S5 Support

The TPS51200-Q1 device provides S3 support by an EN function. The EN pin can be connected to an SLP_S3 signal in the end application. Both the REFOUT and VO pin are on when EN = high (S0 state). The REFOUT pin is maintained while the VO pin is turned off and discharged through an internal discharge MOSFET when EN = low (S3 state). When EN = low and the REFIN voltage is less than 0.390 V, the TPS51200-Q1 device enters pseudo-S5 state. Both the VO and REFOUT outputs are turned off and discharged to the GND pin through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). Figure 19 shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support. It is also allowed to turn on VLDOIN earlier than VIN during power on, and turn off VIN earlier than VLDOIN during power off.

7.4.2 Tracking Startup and Shutdown

The TPS51200-Q1 device also supports tracking startup and shutdown when the EN pin is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, the VO pin follows the REFOUT pin when the REFIN voltage is greater than 0.39 V. The REFIN pin follows the rise of the VDDQ rail though a voltage divider. The typical soft-start time for the VDDQ rail is approximately 3 ms, however this soft-star time can vary depending on the system configuration. The SS time of the VO output no longer depends on the OCL setting, but is a function of the SS time of the VDDQ rail. PGOOD is asserted 2 ms after the VO pin is within ±20% of the REFOUT pin. During tracking shutdown, the VO pin falls following the REFOUT pin until the REFOUT pin reaches 0.37 V. When the REFOUT pin falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both the REFOUT and VO pins to GND. The PGOOD pin is deasserted when the VO pin is beyond the ±20% range of the REFOUT pin. Figure 20 shows the typical timing diagram for an application that uses tracking startup and shutdown.

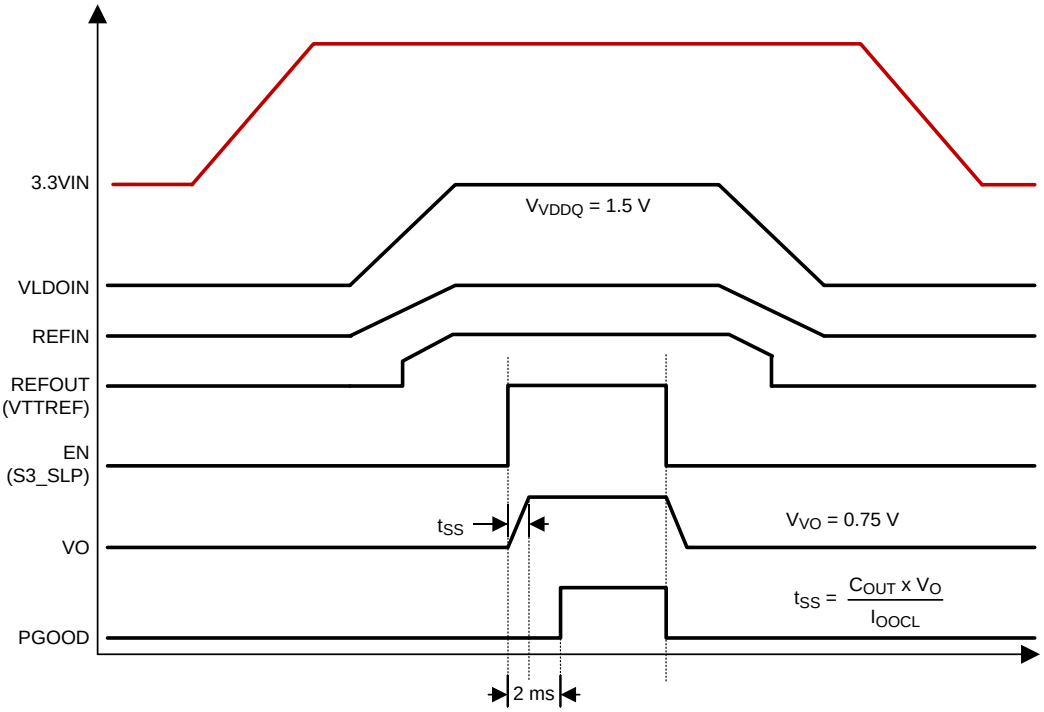


Figure 19. Typical Timing Diagram for S3 and Pseudo-S5 Support

Device Functional Modes (continued)

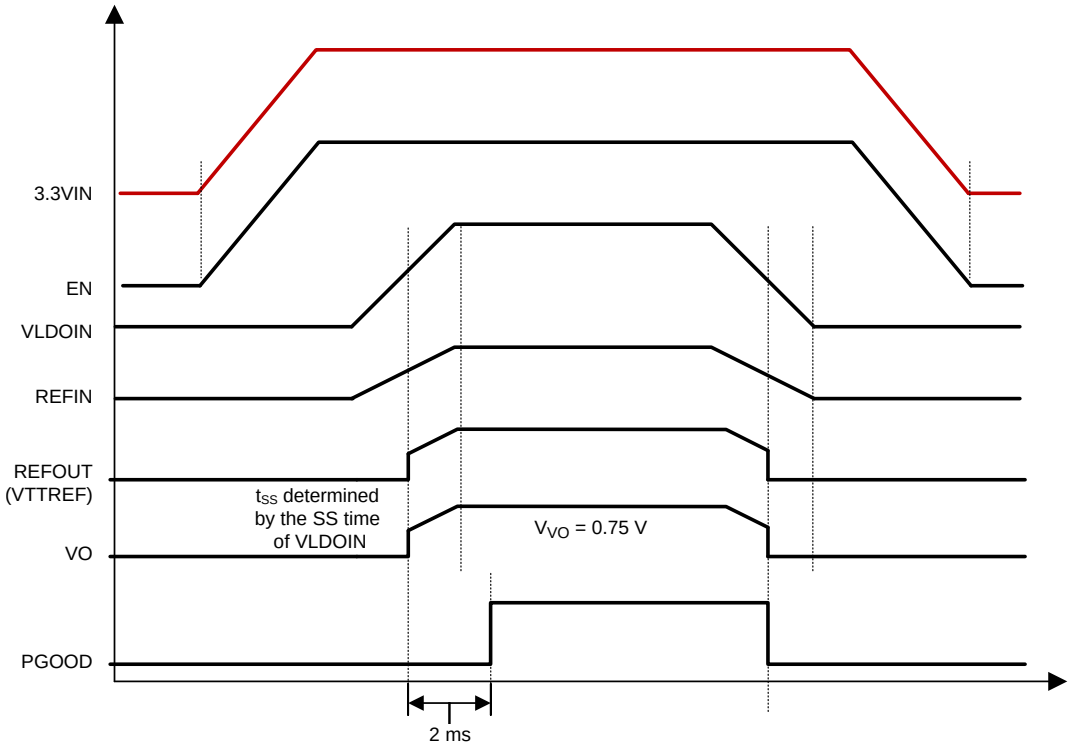


Figure 20. Typical Timing Diagram of Tracking Startup and Shutdown

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS51200-Q1 device is specifically designed to power up the memory termination rail (as shown in Figure 21). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 22 for typical characteristics for a single memory cell.

8.2 Typical Application

8.2.1 VTT DIMM Applications

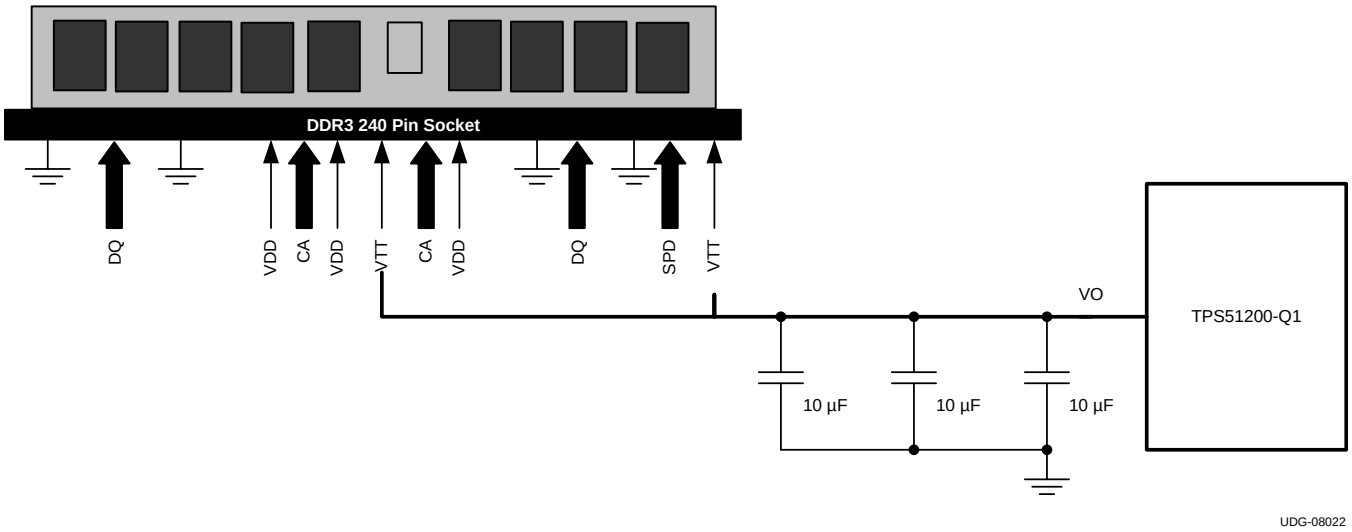


Figure 21. Typical Application Diagram for DDR3 VTT DIMM using TPS51200-Q1

8.2.1.1 Design Parameters

Use the information listed in Table 1 as the design parameters.

Table 1. DDR, DDR2, DDR3, LP DDR3 and DDR4 Termination Technology and Differences

PARAMETER	DDR	DDR2	DR3	LP DDR3 or DDR4
FSB Data Rates	200, 266, 333 and 400 MHz	400, 533, 677 and 800 MHz	800, 1066, 1330 and 1600 MHz	Same as DDR3
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	Same as DDR3
Termination Current Demand	Max source/sink transient currents of up to 2.6 A to 2.9 A	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1 A of burst current	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1A of burst current	Same as DDR3
Voltage Level	2.5-V Core and I/O 1.25-V VTT	1.8-V Core and I/O 0.9-V VTT	1.5-V Core and I/O 0.75-V VTT	1.2-V Core and I/O 0.6-V VTT

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 VIN Capacitor

Add a ceramic capacitor, with a value between 1-μF and 4.7-μF, placed close to the VIN pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

8.2.1.2.2 VLDO Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-μF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at the VO pin. In general, use one-half of the C_{OUT} value for input.

8.2.1.2.3 Output Capacitor

For stable operation, the total capacitance of the VO output pin must be greater than 20 μF. Attach three, 10-μF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VOSNS input to achieve loop stability. The R-C filter time constant must be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

8.2.1.2.4 Output Tolerance Consideration for VTT DIMM Applications

Figure 22 shows the typical characteristics for a single memory cell.

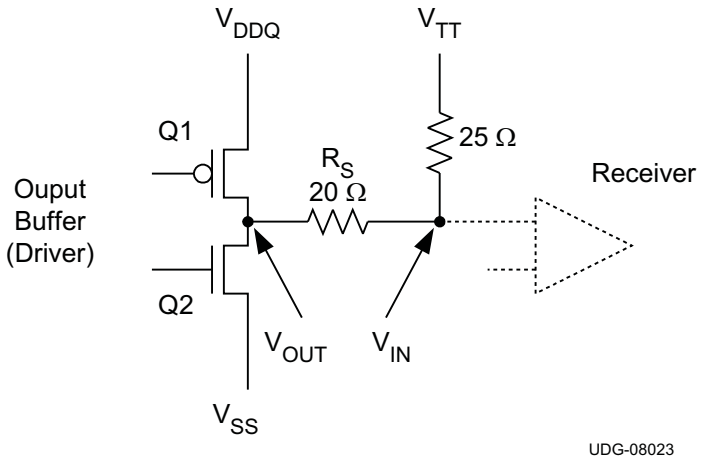


Figure 22. DDR Physical Signal System Bi-Directional SSTL Signaling

In Figure 22, when Q1 is on and Q2 is off:

- The current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

In Figure 22, when Q2 is on and Q1 is off:

- The current flows from VTT via the termination resistor to GND
- VTT sources current

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

VTTREF – 40 mV < VTT < VTTREF + 40 mV, for both dc and ac conditions

The specification indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS51200-Q1 device ensures the regulator output voltage to be:

VTTREF –25 mV < VTT < VTTREF + 25 mV, for both DC and AC conditions and –2 A < I_{VTT} < 2 A

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3, DDR3L, low-power DDR3 and DDR4 applications (see Table 1 for detailed information). To meet the stability requirement, a minimum output capacitance of 20 μF is needed. Considering the actual tolerance on the MLCC capacitors, three 10-μF ceramic capacitors are sufficient to meet the above requirement.

The TPS51200-Q1 device is designed as a Gm driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 2 A and changes with respect to the load to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm (see Equation 1).

$$F_{UGBW} = \frac{Gm}{2 \times \pi \times C_{OUT}} \quad (1)$$

where

- F_{UGBW} is the unity gain bandwidth
- Gm is transconductance
- C_{OUT} is the output capacitance

This type of regulator has two limitations on the output bulk capacitor requirement. To maintain stability, the zero location contributed by the ESR of the output capacitors must be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors must not be used in the design. In addition, the impedance characteristics of the ceramic capacitor must be well understood to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor and parasitic inductance of the VO trace.

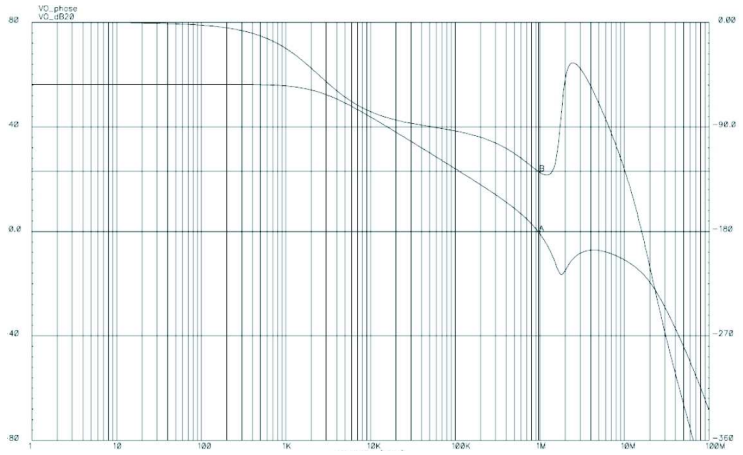


Figure 23. Bode Plot for a Typical DDR3 Configuration

Figure 23 shows the bode plot simulation for a typical DDR3 configuration of the TPS51200-Q1 device, where:

- V_{IN} = 3.3 V
- V_{VLDOIN} = 1.5 V
- V_{VO} = 0.75 V
- I_{IO} = 2 A
- 3 × 10-μF capacitors included
- ESR = 2.5 mΩ
- ESL = 800 pH

The unity-gain bandwidth is approximately 1 MHz and the phase margin is 52°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

shows the load regulation and Figure 25 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to ±1.5-A load step and release, the output voltage measurement shows no difference between the dc and ac conditions.

8.2.1.3 Application Curves

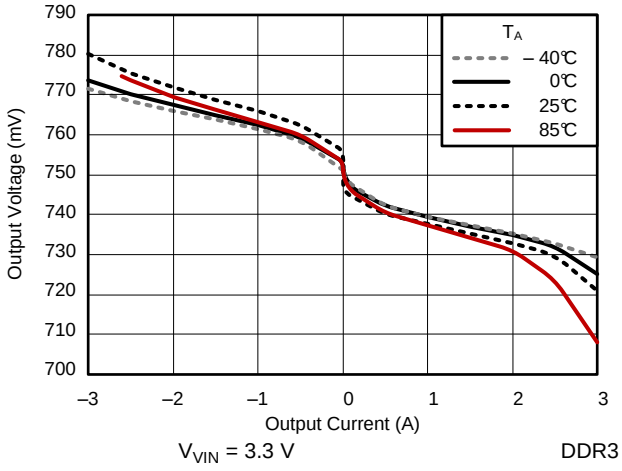


Figure 24. Output Current vs Output voltage

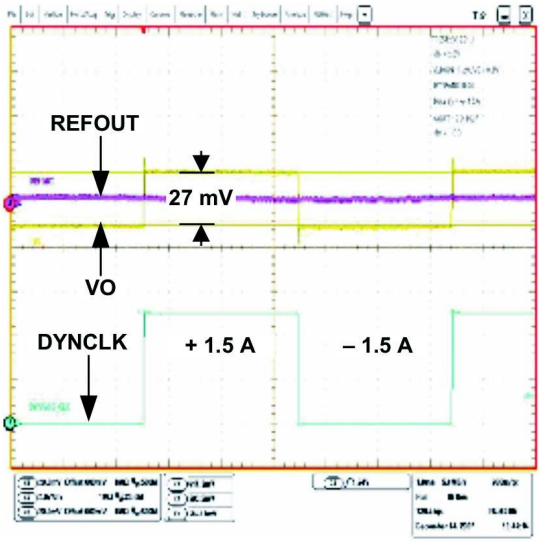


Figure 25. Transient Waveform

8.2.2 Design Example 1

This design example describes a 3.3-V_{IN}, DDR2 configuration.

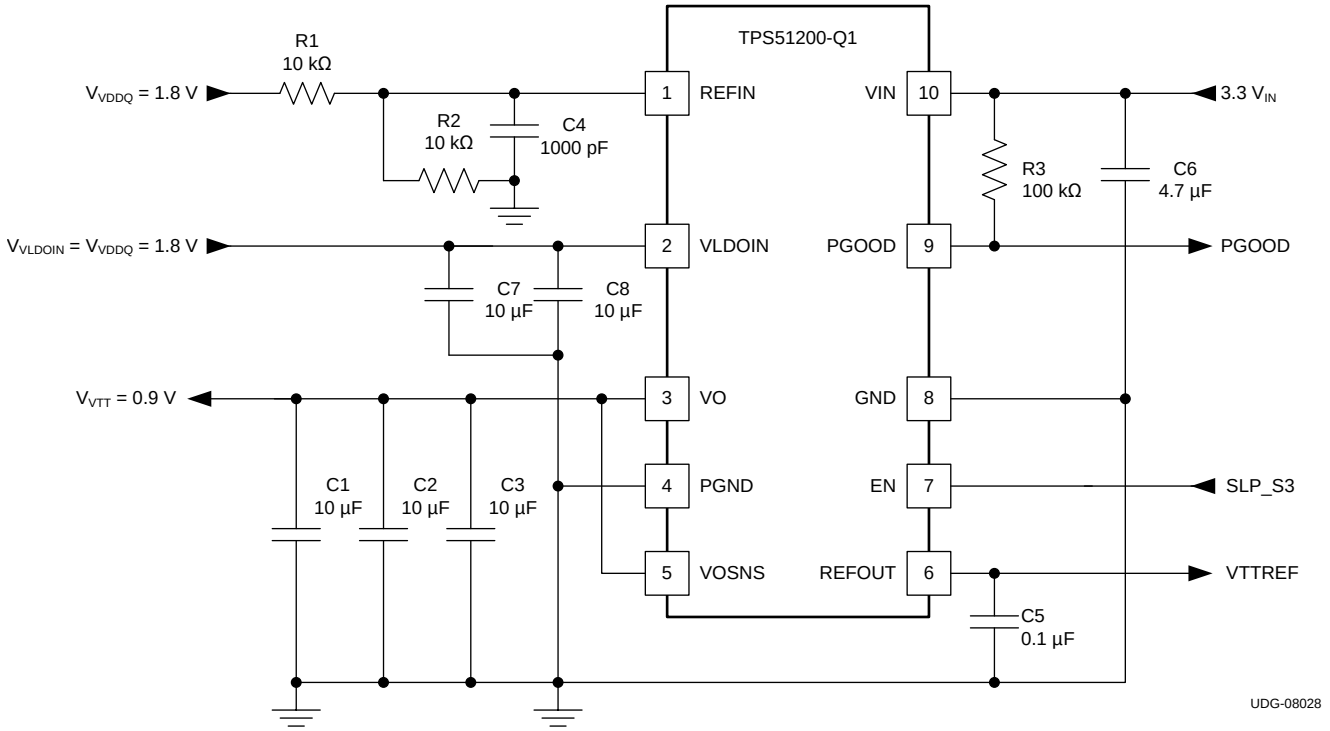


Figure 26. 3.3-V_{IN}, DDR2 Configuration

8.2.2.1 Design Parameters

For this design example, use the parameters listed in Table 2.

Table 2. Design Example 1 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.3 Design Example 2

This design example describes a 3.3-V_{IN}, DDR3 configuration.

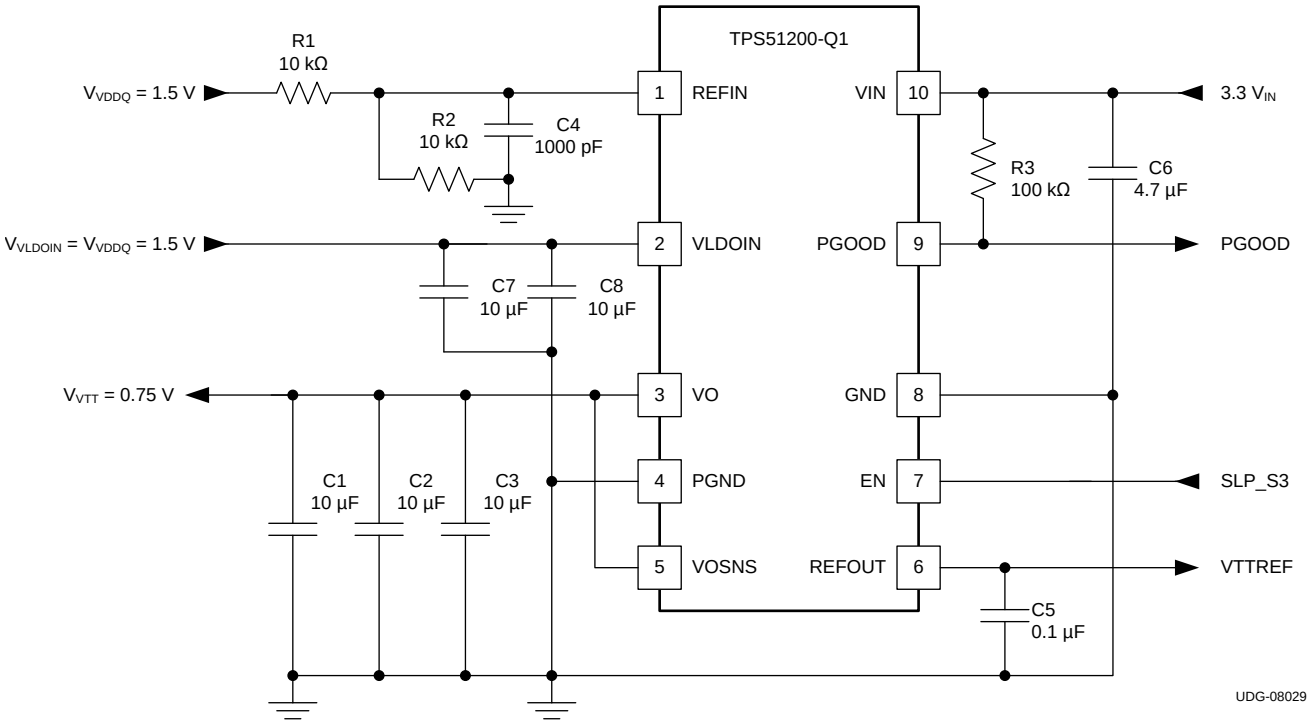


Figure 27. 3.3-V_{IN}, DDR3 Configuration

8.2.3.1 Design Parameters

For this design example, use the parameters listed in Table 3.

Table 3. Design Example 2 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.4 Design Example 3

This design example describes a 2.5-V_{IN}, DDR3 configuration.

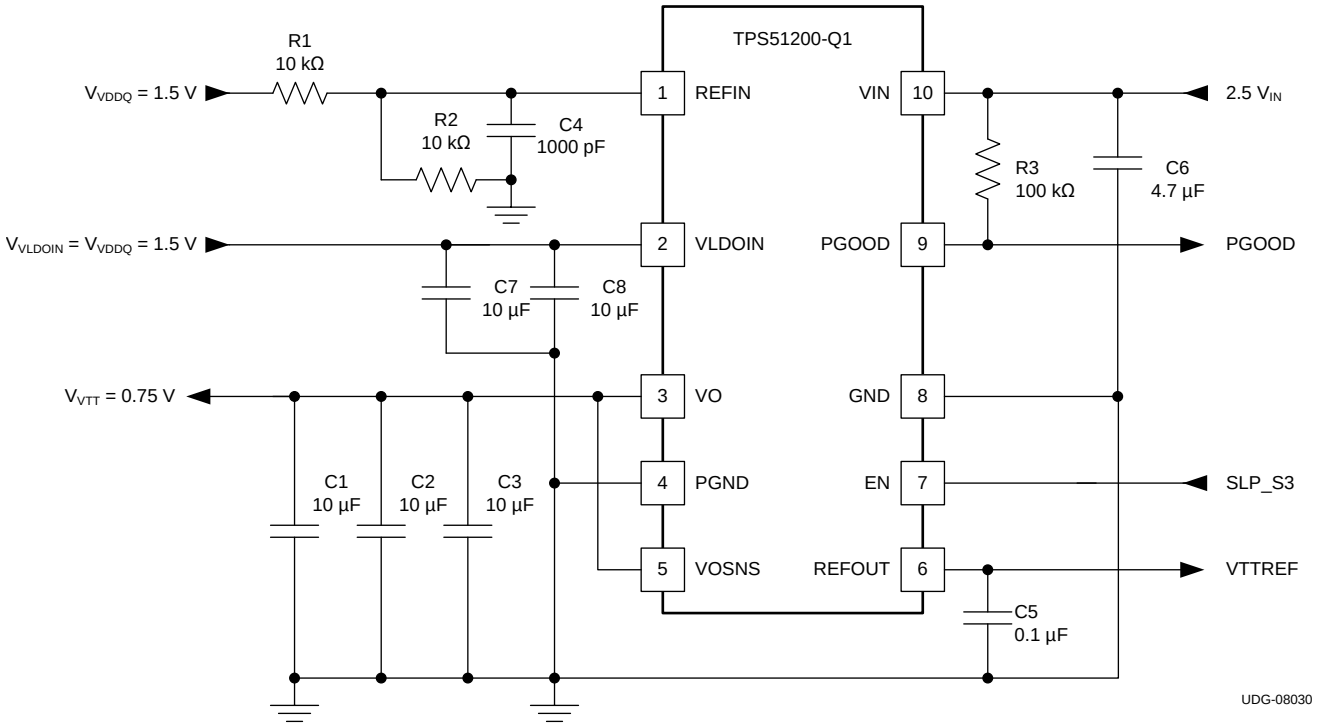


Figure 28. 2.5-V_{IN}, DDR3 Configuration

8.2.4.1 Design Parameters

For this design example, use the parameters listed in Table 4.

Table 4. Design Example 3 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.5 Design Example 4

This design example describes a 3.3-V_{IN}, LP DDR3 or DDR4 configuration.

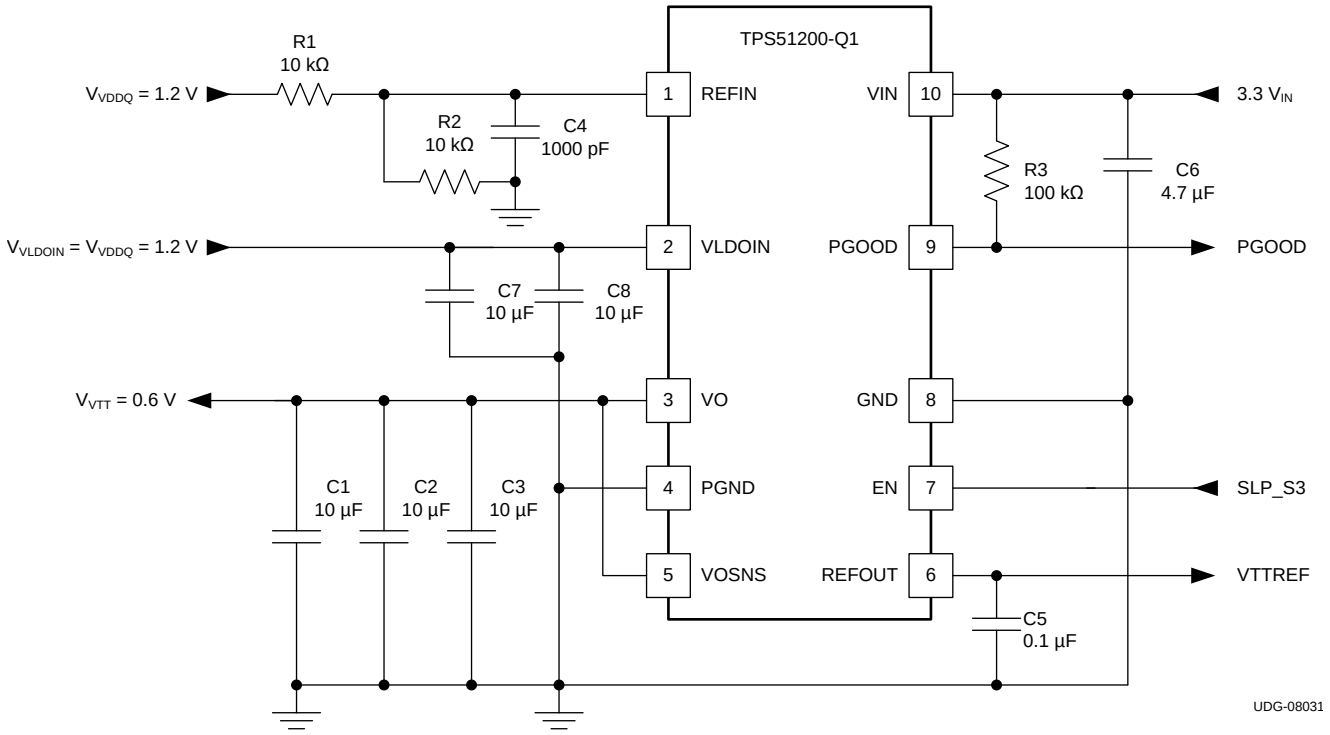


Figure 29. 3.3-V_{IN}, LP DDR3 or DDR4 Configuration

8.2.5.1 Design Parameters

For this design example, use the parameters listed in Table 5.

Table 5. Design Example 4 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.6 Design Example 5

This design example describes a 3.3-V_{IN}, DDR3 tracking configuration.

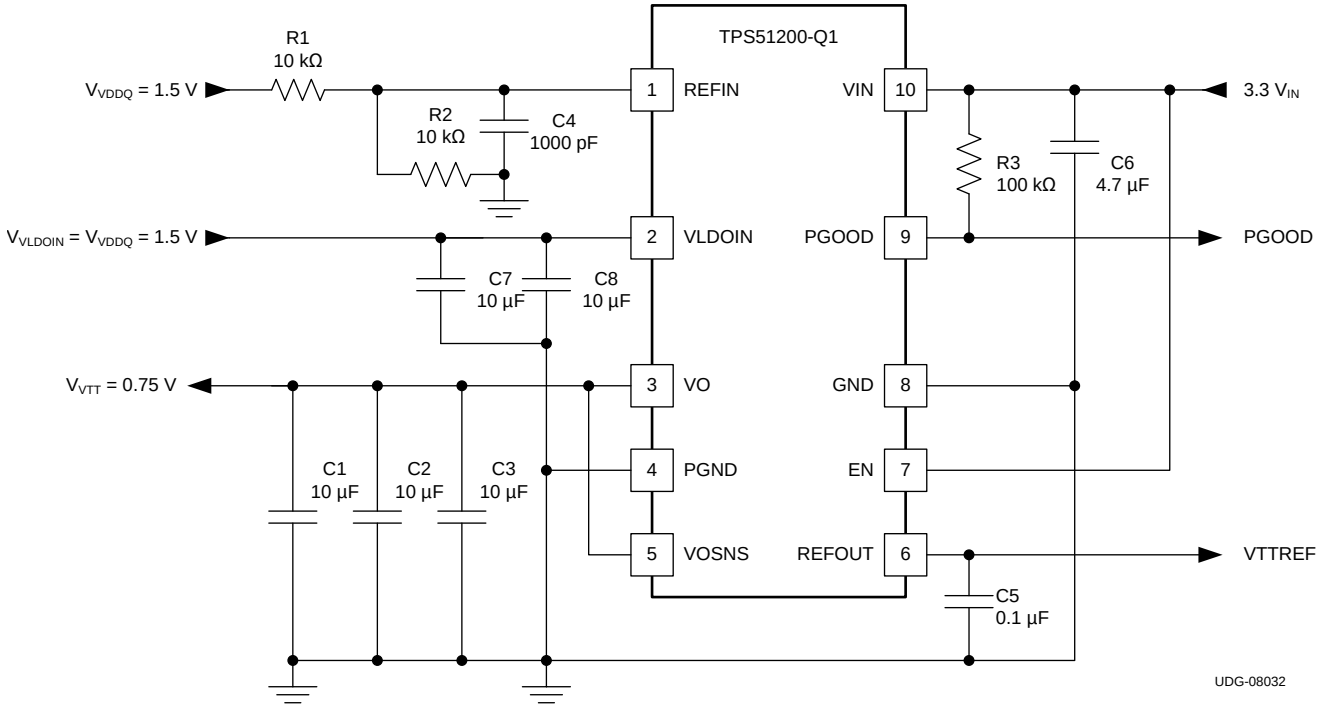


Figure 30. 3.3-V_{IN}, DDR3 Tracking Configuration

8.2.6.1 Design Parameters

For this design example, use the parameters listed in Table 6.

Table 6. Design Example 5 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.7 Design Example 6

This design example describes a 3.3-V_{IN}, LDO configuration.

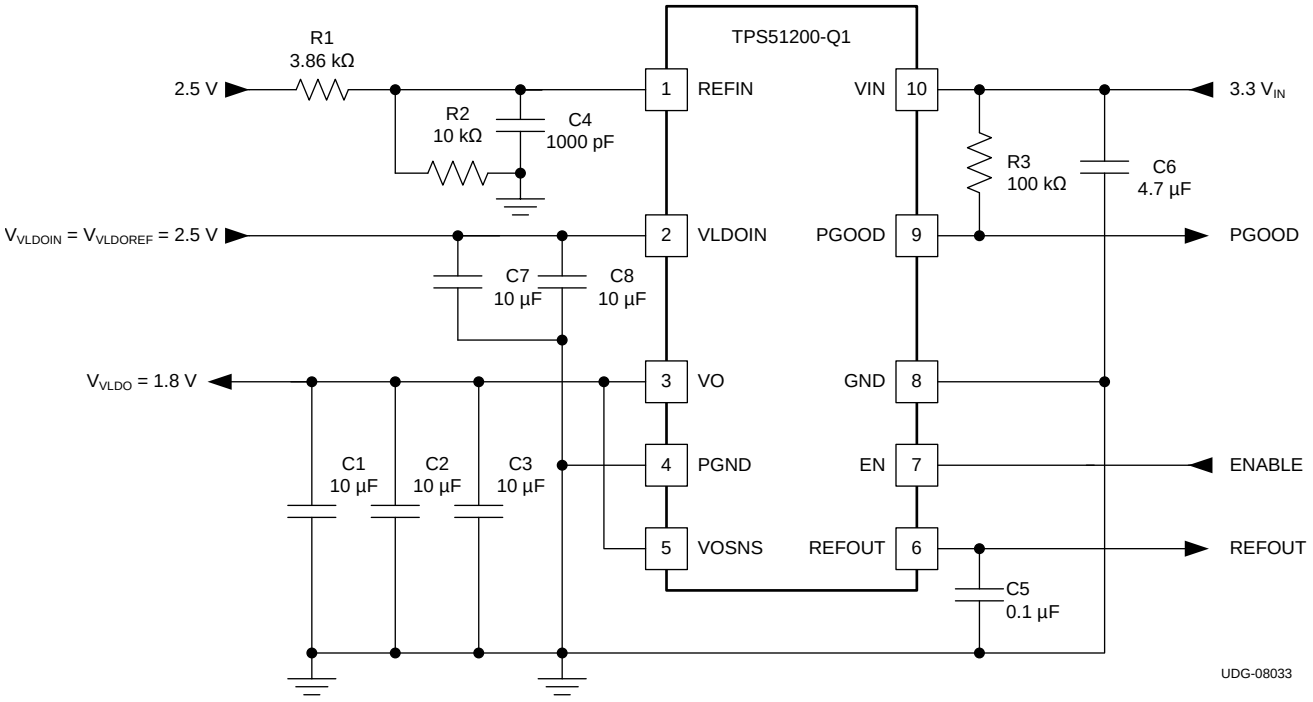


Figure 31. 3.3-V_{IN}, LDO Configuration

8.2.7.1 Design Parameters

For this design example, use the parameters listed in Table 7.

Table 7. Design Example 6 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	10 kΩ		
R2		3.86 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

8.2.8 Design Example 7

This design example describes a 3.3-V_{IN}, DDR3 configuration with LPF (low pass filter between VTT and VOSNS).

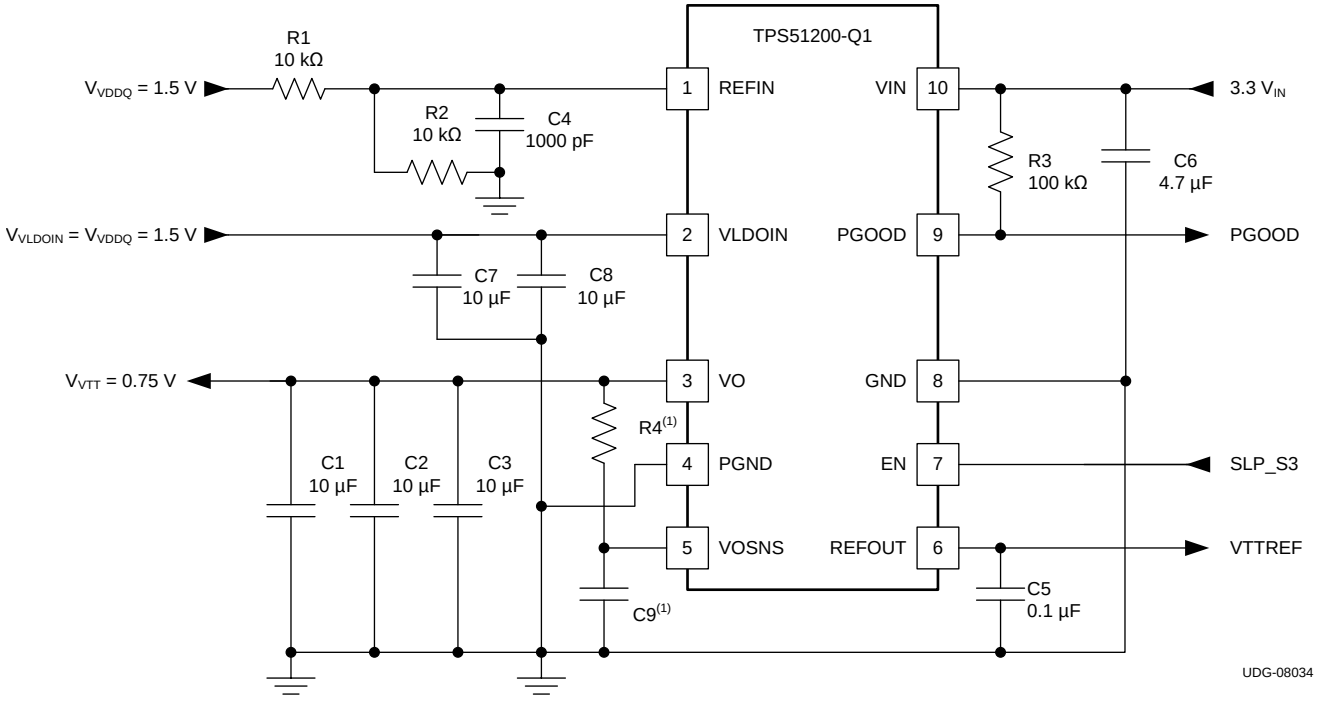


Figure 32. 3.3-V_{IN}, DDR3 Configuration with LPF

8.2.8.1 Design Parameters

For this design example, use the parameters listed in Table 8.

Table 8. Design Example 7 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
R4(1)				
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C9(1)				

(1) The values of R4 and C9 must be chosen to reduce the parasitic effect of the trace (between VO and the output MLCCs) and the output capacitors (ESR and ESL).

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range between 2.375 V and 3.5 V. This input supply must be well regulated. TI recommends adding at least one 1-µF to 4.7-µF ceramic capacitor at the VIN pin.

10 Layout

10.1 Layout Guidelines

Consider the following points before starting the TPS51200-Q1 layout design.

- Place the input capacitors as close to VDLOIN pin as possible with short and wide connection.
- Place the output capacitor as close to VO pin as possible with short and wide connection. Place a ceramic capacitor with a value of at least 10-µF as close to VO pin if the rest of output capacitors need to be placed on the load side.
- Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VO sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.
- Consider adding low-pass filter at VOSNS if the VO sense trace is very long.
- Connect the GND pin and PGND pin to the thermal pad directly.
- The device uses its thermal pad to dissipate heat. In order to effectively remove heat from device package, place numerous ground vias on the thermal pad. Use large ground copper plane, especially the copper plane on surface layer, to pour over those vias on thermal pad.
- Consult the TPS51200EVM User's Guide (SLUU323) for detailed layout recommendations.

10.2 Layout Example

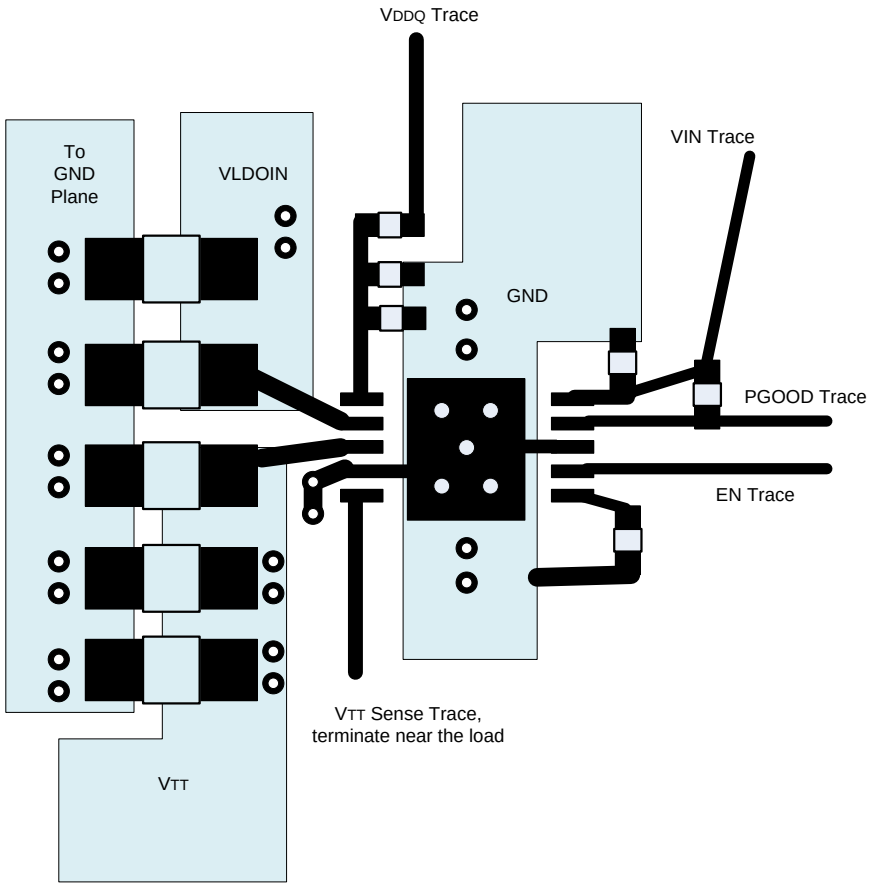


Figure 33. TPS51200-Q1 Layout Example

10.3 Thermal Considerations

Because the TPS51200-Q1 device is a linear regulator, the VO current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VLDOIN and VO times IO (I_{IO}) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O\_SRC} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VO voltage is applied across the internal LDO regulator, and the power dissipation, P_{DISS_SNK} can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \quad (3)$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation must be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the VIN supply and the VLDOIN supply. This can be estimated as 5 mW or less during normal operatiing conditions. This power must be effectively dissipated from the package.

Maximum power dissipation allowed by the package is calculated by Equation 4.

$$P_{PKG} = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA}$$

$$P_{PKG} = \frac{T_{J(max)} \times T_{A(max)}}{R_{\theta JA}} \quad (4)$$

where

- $T_{J(MAX)}$ is 125°C
- $T_{A(MAX)}$ is the maximum ambient temperature in the system
- $R_{\theta JA}$ is the thermal resistance from junction to ambient

The thermal performance of an LDO depends on the printed circuit board (PCB) layout. The TPS51200-Q1 device is housed in a thermally-enhanced package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to ground via thermal land on the PCB. This ground trace acts as a both a heatsink and heatspreader. The typical thermal resistance, $R_{\theta JA}$, 52.06°C/W, is achieved based on a land pattern of 3 mm × 1,9 mm with four vias (0,33-mm via diameter, the standard thermal via size) without air flow (see Figure 34).

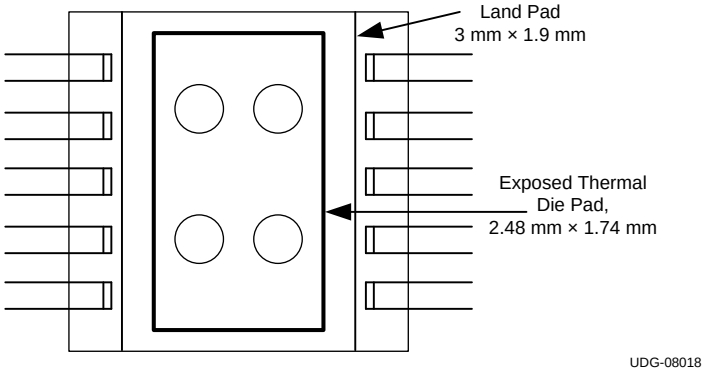


Figure 34. Recommend Land Pad Pattern for TPS51200-Q1

Thermal Considerations (continued)

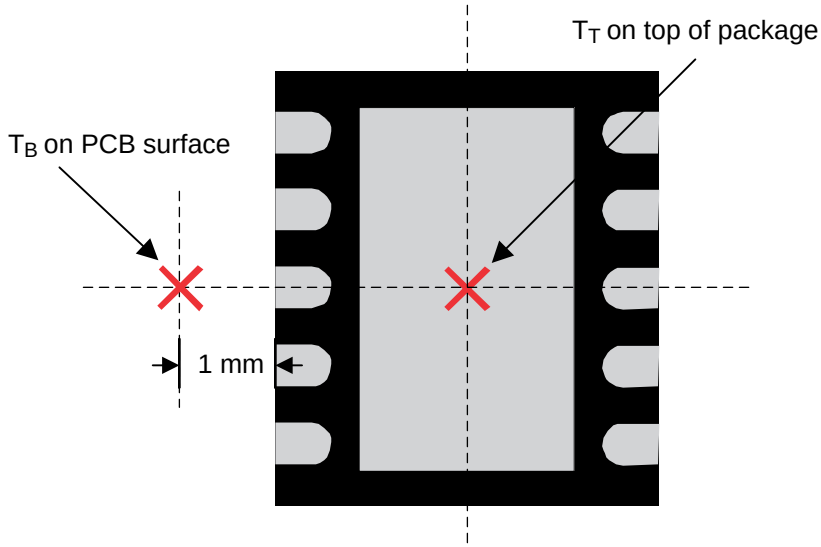


Figure 35. Package Thermal Measurement

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to thermal pad. The typical thermal resistance from junction to thermal pad, $R_{\theta JP}$, is 10.24°C/W (based on the recommend land pad and four standard thermal vias).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

TPS51200-EVM User's Guide, SLUU323

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51200QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PSNQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS51200-Q1 :

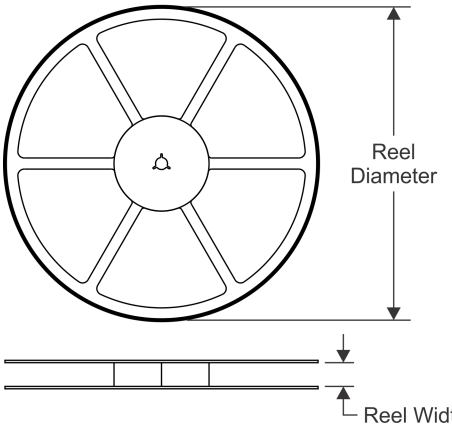
- Catalog: TPS51200
- Enhanced Product: TPS51200-EP

NOTE: Qualified Version Definitions:

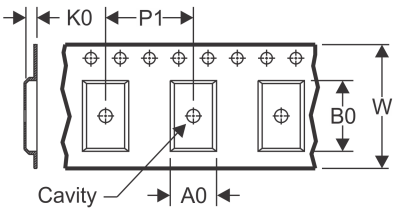
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

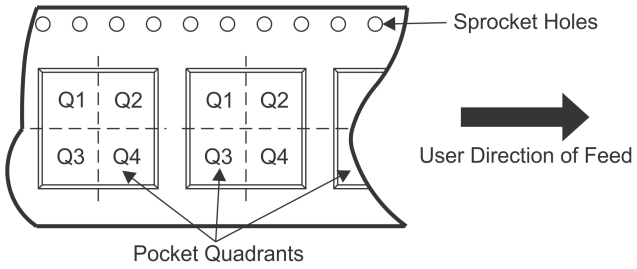


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

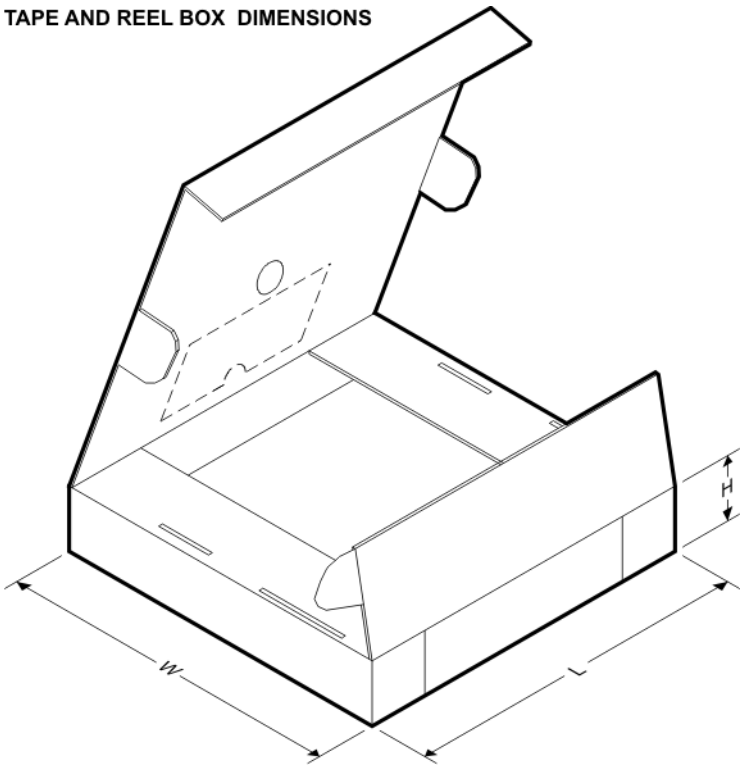
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51200QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



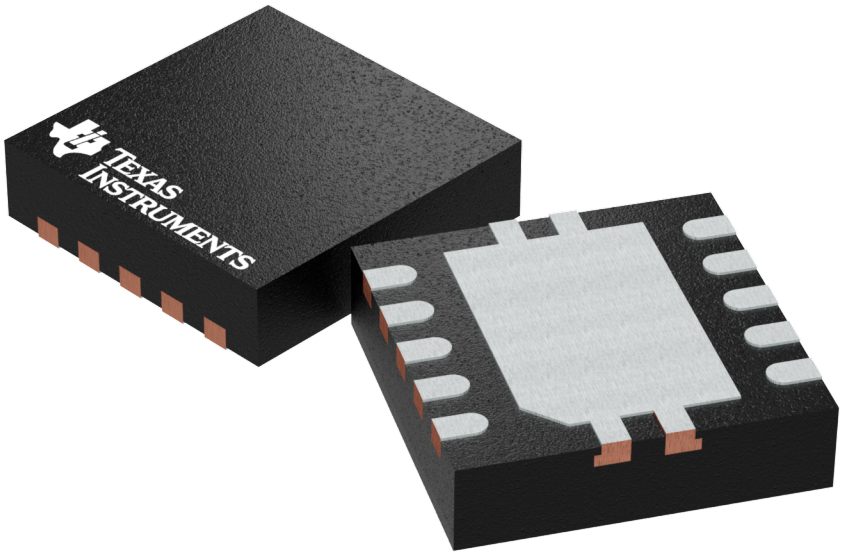
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51200QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



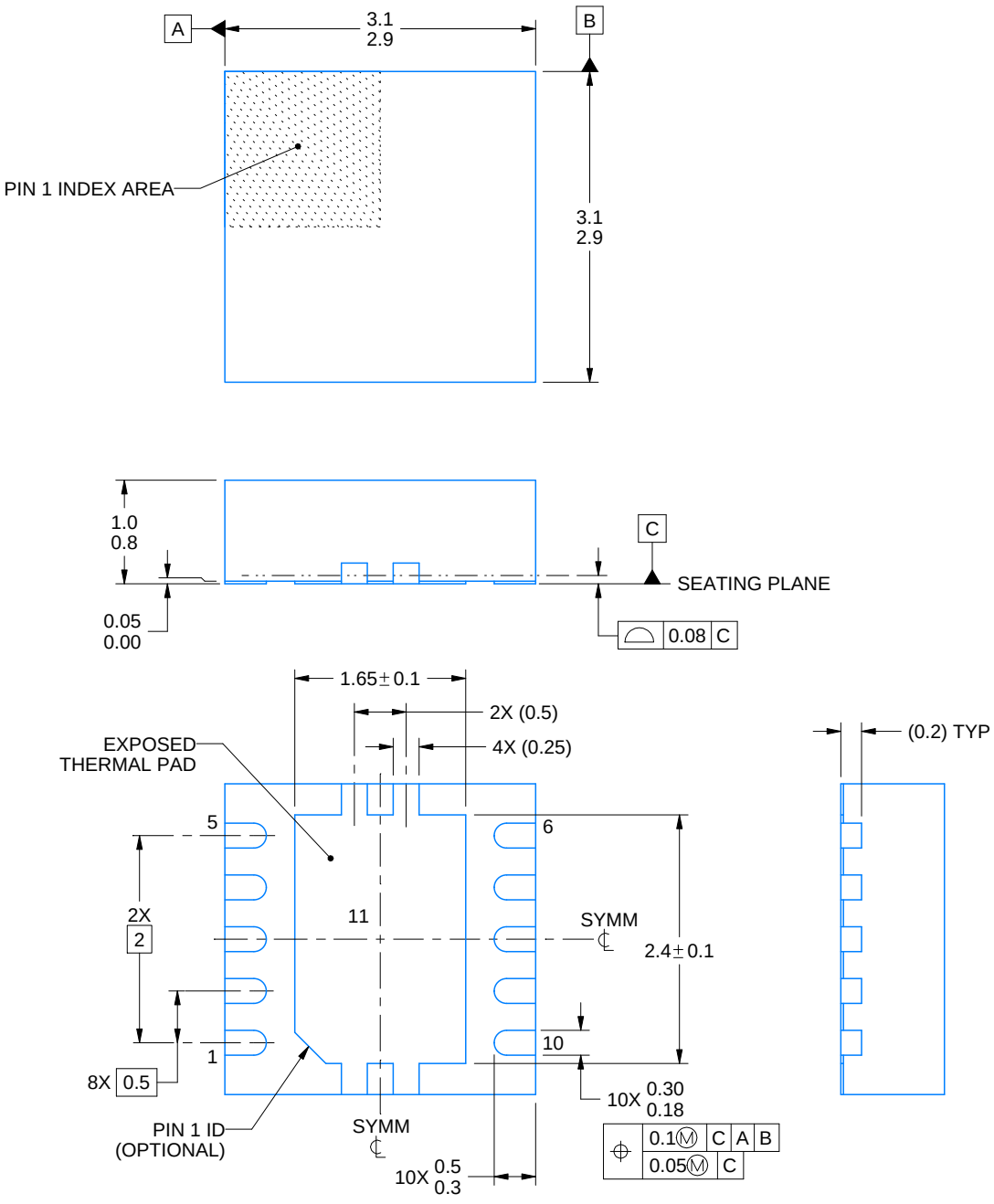
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

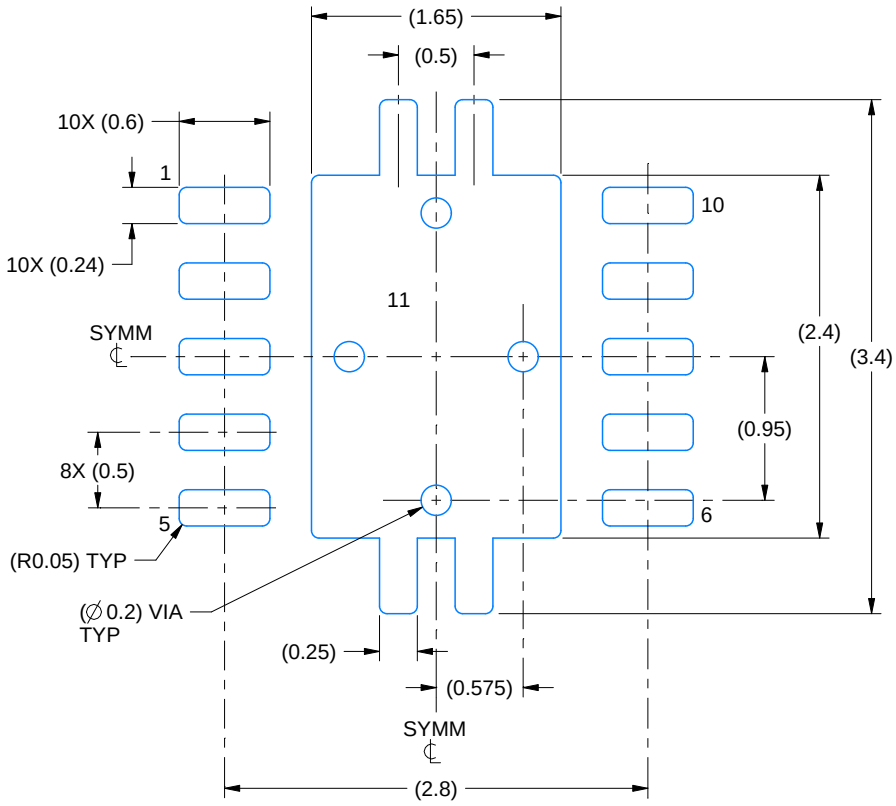
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

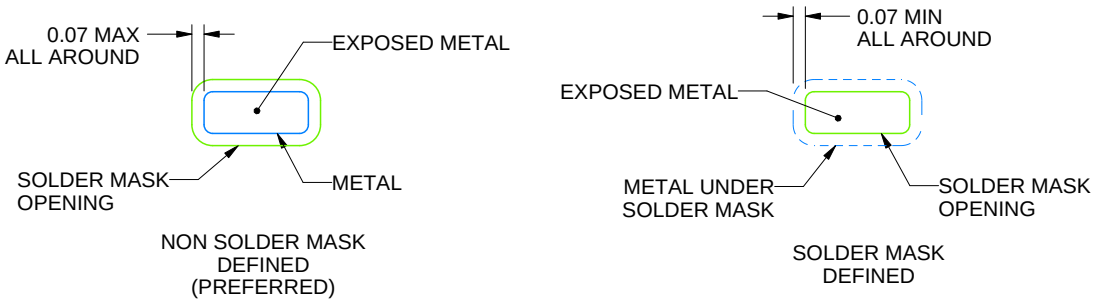


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

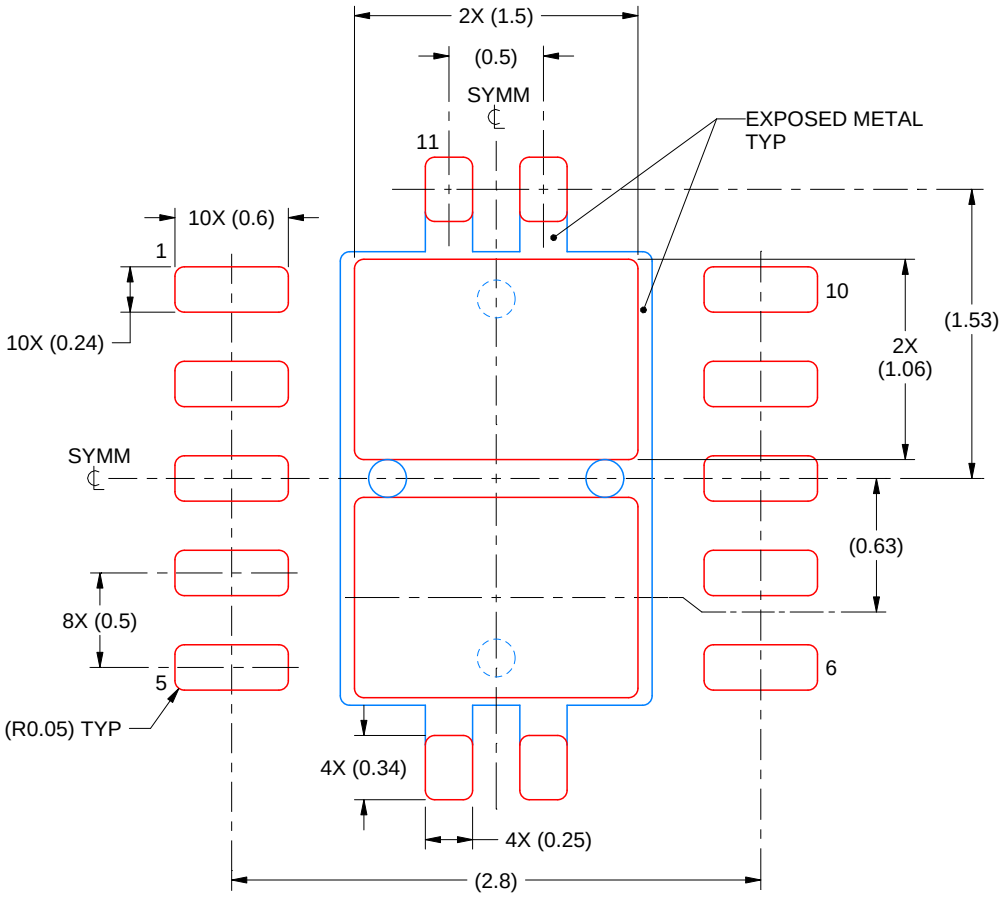
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265