TPL0202 256-Taps Dual Channel Digital Potentiometer With SPI and Non-Volatile Memory

1 Features

- Two Potentiometers With 256-Position Resolution
- Non-Volatile Memory Stores Wiper Settings
- 10-kΩ End-to-End Resistance (TPL0202-10)
- Fast Power-Up Response Time: <100 µs
- ±1 LSB INL, ±0.5 LSB DNL (Voltage-Divider Mode)
- 12 ppm/°C Ratiometric Temperature Coefficient
- SPI Serial Interface
- 2.7 to 5.5 V Single-Supply Operation
- Operating Temperature Range From –40°C to +105°C

2 Applications

- Adjustable Gain Amplifiers and Offset Trimming
- Adjustable Power Supplies
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration
- Mechanical Potentiometer Replacement

3 Description

The TPL0202 has two linear-taper digital potentiometers (DPOTs) with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0202-10 has an end-to-end resistance of 10 kΩ.

This DPOT can be used as a mechanical potentiometer replacement, allowing the user (or software) to digitally control and adjust resistance.

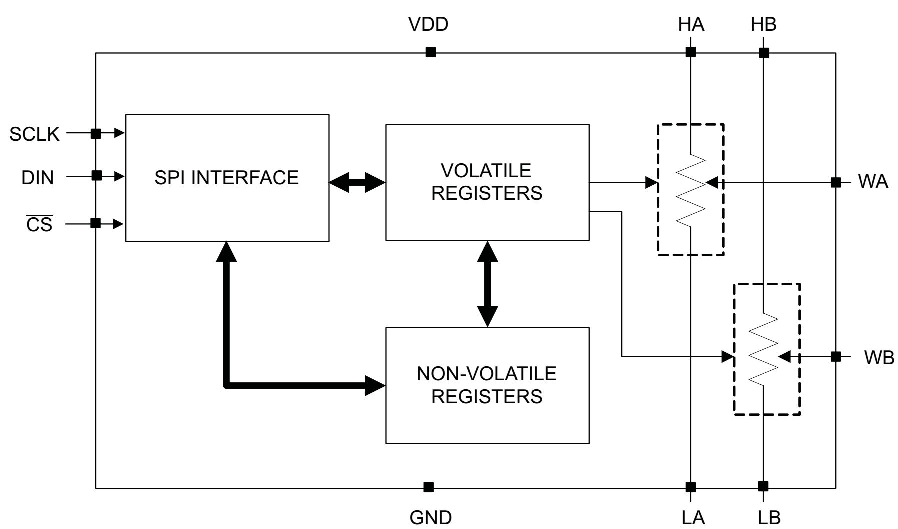
The TPL0202 has non-volatile memory (EEPROM) which can be used to store the wiper position for automatic recall upon power-up. The internal registers of the TPL0202 can be accessed using a SPI-compatible digital interface.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPL0202	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

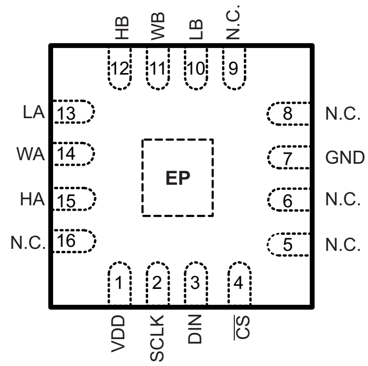
Changes from Revision D (October 2015) to Revision E	Page
• Changed "read endurance" to: "write endurance"	6
• Added *Receiving Notification of Documentation Updates* section	27

Changes from Revision C (June 2012) to Revision D	Page
• Added *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Fixed *SPI Timing Requirements* to show 5 MHz max SCLK frequency	7

Changes from Revision B (August 2011) to Revision C	Page
• Updated Pin Description Table.	3

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	Power	Supply voltage
SCLK	2	Input	SPI clock
DIN	3	Input	SPI input
$\overline{CS}$	4	Input	SPI chip select (active low)
N.C.	5, 6, 8, 9, 16	—	Not internally connected. Can be connected to GND
GND	7	—	Ground
LB	10	I/O	Low terminal of potentiometer B
WB	11	I/O	Wiper terminal of potentiometer B
HB	12	I/O	High terminal of potentiometer B
LA	13	I/O	Low terminal of potentiometer A
WA	14	I/O	Wiper terminal of potentiometer A
HA	15	I/O	High terminal of potentiometer A
EP	EP	—	Exposed thermal pad Can be connected to GND or left unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2] [3]

			MIN	MAX	UNIT
	Supply voltage	V_{DD} to GND	–0.3	7	V
		All other pins to GND	–0.3	V_{DD} + 0.3	V
I_L I_W I_H	Pulse current			±20	mA
	Continuous current	TPL0202-10		±2	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Follows the algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{DD,GND}$			2.7	5.5	V
V_H, V_L, V_W	Terminal voltage range		0	V_{DD}	V
V_{IH}	Voltage input high (SCLK, DIN, CS)	V_{DD} = 3.6 V to 5.5 V	2.4	5.5	V
		V_{DD} = 2.7 V to 3.6 V	0.7 × V_{DD}	5.5	
V_{IL}	Voltage input low (SCLK, DIN, CS)		0	0.8	V
I_W	Wiper current			±2	mA
T_A	Free-air ambient temperature		–40	105	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPL0202 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

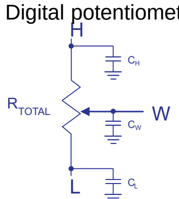
V_{DD} = 2.7 to 5.5 V, T_A= –40°C to +105°C (unless otherwise noted). Typical values are at V_{DD}= 5 V, T_A= 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TOT}	End-to-end resistance (between H and L terminals)	$V_L = V_{DD}$ / 2, I_{HL} = 100 µA, Input code = 0x80, Measure V_{HL}	8	10	12	kΩ
R_H	High terminal resistance	$V_L = V_{DD}$ / 2, I_{HL} = 100 µA, Input code = 0xFF, Measure V_{HW}		100	200	Ω
R_L	Low terminal resistance	$V_L = V_{DD}$ / 2, I_{HL} = 100 µA, Input code = 0x00, Measure V_{WL}		60	200	Ω
R_W	Wiper resistance	$V_L = V_{DD}$ / 2, I_{WL} = 100 µA, Input code = 0x00, Measure V_{HW}		25	100	Ω
C_H, C_L (1) (2)	Terminal capacitance			22		pF
C_W (1) (2)	Wiper capacitance			18		pF
I_{LKG}	Terminal leakage current	$V_H = V_{SS}$ to V_{DD}, V_L = Floating OR $V_L = V_{SS}$ to V_{DD}, V_H = Floating		0.1	1	µA
TC_R	Resistance temperature coefficient	Input code = 0x80h		132		ppm/°C
$R_{TOT,MATCH}$	Channel-to-channel resistance match			0.1%		
VOLTAGE DIVIDER MODE						
INL (3) (4)	Integral non-linearity		–1		1	LSB
DNL (3) (5)	Differential non-linearity		–0.5		0.5	LSB
ZS_{ERROR} (6) (7)	Zero-scale error		0	2	5	LSB
FS_{ERROR} (6) (8)	Full-scale error		–5	–2	0	LSB
V_{MATCH} (6) (9)	Channel-to-channel matching	Wiper at the same tap position, same voltage all H and the same voltage at all L terminals	–2		2	LSB
TC_V	Ratiometric temperature coefficient	Wiper set at midscale		12		ppm/°C
BW	Bandwidth	Wiper set at midscale C_{LOAD} = 10 pF $V_L = V_{DD}$ / 2, Signal applied to H; measurement at W		2000		kHz
t_{wo}	Register write to output time	Time from CS rising edge to 90% of expected value		2		µs
THD+N	Total harmonic distortion + noise	V_{HL} = 1 V_{RMS} at 1 kHz, $V_L = V_{DD}$ / 2, Measurement at W		0.03%		

(1) Terminal and wiper capacitance extracted from self admittance of three-port network measurement

$$Y_{ii} = \left.\frac{I_i}{V_i}\right|_{V_k = 0 \text{ for } k \neq i}$$

(2) Digital potentiometer macromodel



(3) LSB = ($V_{MEAS[code\ 255]} - V_{MEAS[code\ 0]}$) / 255
(4) INL = (($V_{MEAS[code\ x]} - V_{MEAS[code\ 0]}$) / LSB) – [code x]
(5) DNL = (($V_{MEAS[code\ x]} - V_{MEAS[code\ x-1]}$) / LSB) – 1
(6) IDEAL_LSB = ($V_H - V_L$) / 256
(7) $ZS_{ERROR} = V_{MEAS[code\ 0]}$ / IDEAL_LSB
(8) FS_{ERROR} = [($V_{MEAS[code\ 255]}$ – ($V_H - V_L$)) / IDEAL_LSB] + 1
(9) V_{MATCH} = ($V_{MEAS\_A[code\ x]} - V_{MEAS\_B[code\ x]}$) / IDEAL_LSB

Electrical Characteristics (continued)

V_{DD} = 2.7 to 5.5 V, T_A= –40°C to +105°C (unless otherwise noted). Typical values are at V_{DD}= 5 V, T_A= 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
X_{TALK}	Crosstalk	f_{H_A} = 1 kHz, V_{L_A} = V_{L_B} = V_{DD} / 2, V_{H_B} = Floating Measurement at W_A and W_B		–94		dB
RHEOSTAT MODE (Measurements between W and L with H not connected, or between W and H with L not connected)						
RINL (10) (11)	Integral non-linearity		–1.5		1.5	LSB
RDNL (10) (12)	Differential non-linearity		–0.5		0.5	LSB
R_{OFFSET} (13) (14)	Offset		0	2.5	7	LSB
R_{MATCH} (13) (15)	Channel-to-channel matching		–2		2	LSB

(10) RLSB = ($R_{MEAS[code\ 255]}$ – $R_{MEAS[code\ 0]}$) / 255
(11) RINL =(($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ 0]}$) / RLSB) - [code x]
(12) RDNL = (($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ x-1]}$) / RLSB) – 1
(13) IDEAL_RLSB = R_{TOT} / 256
(14) R_{OFFSET} = $R_{MEAS[code\ 0]}$ / IDEAL_RLSB
(15) R_{MATCH} = ($R_{MEAS\_A[code\ x]}$ – $R_{MEAS\_B[code\ x]}$) / IDEAL_RLSB

6.6 Operating Characteristics

V_{DD} = 2.7 V to 5.5 V, V_H= V_{DD}, V_L= GND, T_A= –40°C to +105°C (unless otherwise noted). Typical values are at V_{DD}= 5 V, T_A= 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(STBY)}$	V_{DD} supply current during standby	Digital inputs = V_{DD} or GND		1	5	µA
I_{DD}	V_{DD} supply current during write cycle only	Digital inputs = V_{DD} or GND			400	µA
$I_{IN\text{-}DIG}$	Digital pins leakage current (SCLK, DIN, $\overline{CS}$ inputs)		–1		1	µA
V_{POR}	Power-on recall voltage	Minimum V_{DD} at which memory recall occurs		2		V
EEPROM SPECIFICATION						
	EEPROM write endurance	T_A = 105°C		1000		cycles
		T_A = 25°C		10000		
	EEPROM retention	T_A = 105°C		20		years
		T_A = 85°C		100		
t_{BUSY}	Write NV register busy time			20		ms
t_{ACC}	Read NV register access time	Time from CS rising edge to wiper start to 10% of expected change with read NVM command		40		ns
t_D	Power-up response time (V_{DD} above V_{POR} to wiper register value recall completed)	Time from V_{POR} to wiper output settled		35	100	µs
SERIAL INTERFACE SPECIFICATIONS (SCLK, DIN, $\overline{CS}$ INPUTS)						
V_{IH}	Input high voltage	V_{DD} = 3.6 to 5.5 V	2.4		5.5	V
		V_{DD} = 2.7 to 3.6 V	0.7 × V_{DD}		5.5	
V_{IL}	Input low voltage	SCLK, DIN, $\overline{CS}$ inputs	0		0.8	V
C_{IN}	Pin capacitance	SCLK, DIN, $\overline{CS}$ inputs		7		pF

6.7 SPI Timing Requirements

V_{DD} = 2.7 V to 5.5 V, V_H= V_{DD}, V_L= GND, T_A= –40°C to +105°C (unless otherwise noted)

		MIN	MAX	UNIT
f_{SCLK}	SCLK frequency		5	MHz
t_{SCP}	SCLK period	200		ns
t_{SCH}	SCLK high time	80		ns
t_{SCL}	SCLK low time	80		ns
t_{CSS}	$\overline{CS}$ fall to SCLK rise setup time	80		ns
t_{CSH}	SCLK rise to $\overline{CS}$ hold time	0		ns
t_{DS}	DIN to SCLK setup time	50		ns
t_{DH}	DIN hold after SCLK rise to $\overline{CS}$ fall	0		ns
t_{CS0}	SCLK rise to $\overline{CS}$ fall	20		ns
t_{CS1}	$\overline{CS}$ rise to SCLK rise hold	80		ns
t_{CSW}	$\overline{CS}$ pulse width high	200		ns

6.8 Typical Characteristics

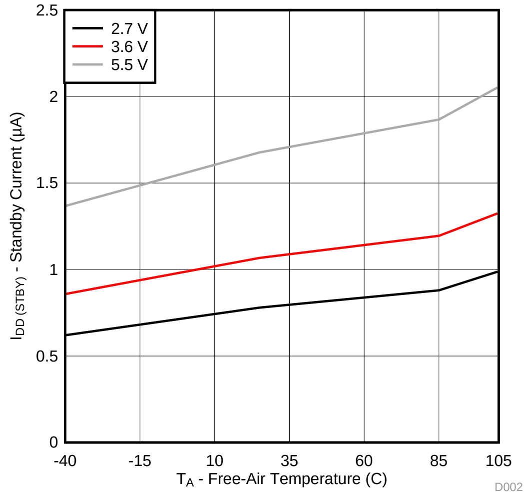


Figure 1. Standby Current vs Temperature

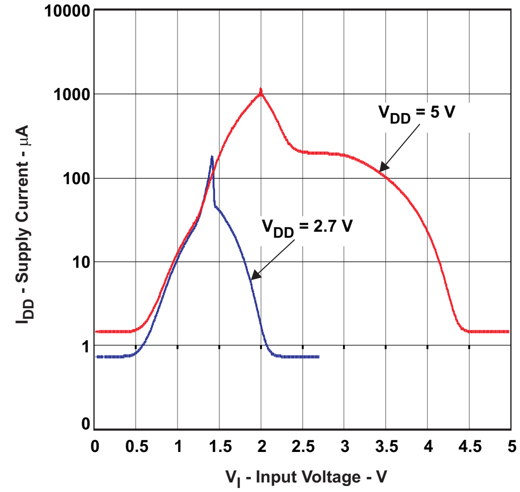


Figure 2. Supply Current vs Digital Input Voltage

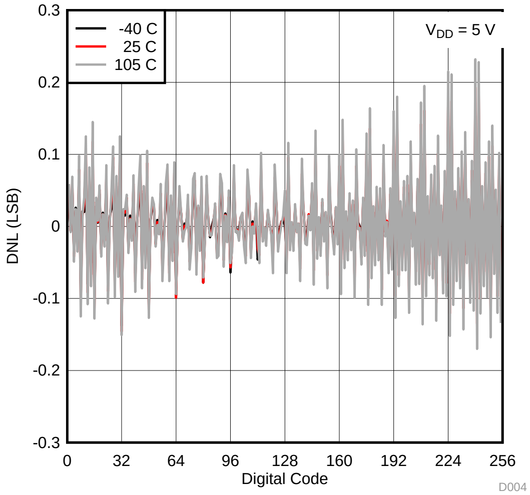


Figure 3. Voltage Divider Mode DNL vs Temperature (V_{DD} = 5 V)

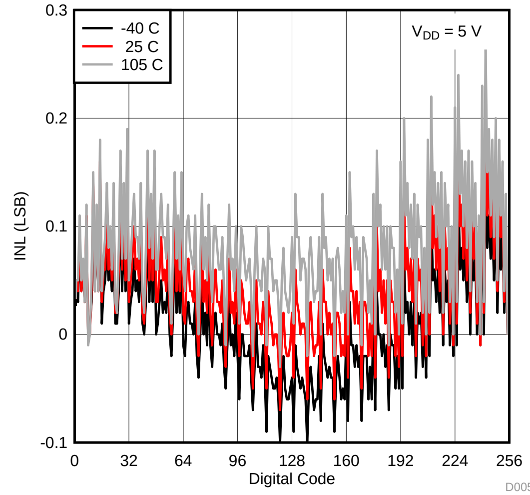


Figure 4. Voltage Divider Mode INL vs Temperature (V_{DD} = 5 V)

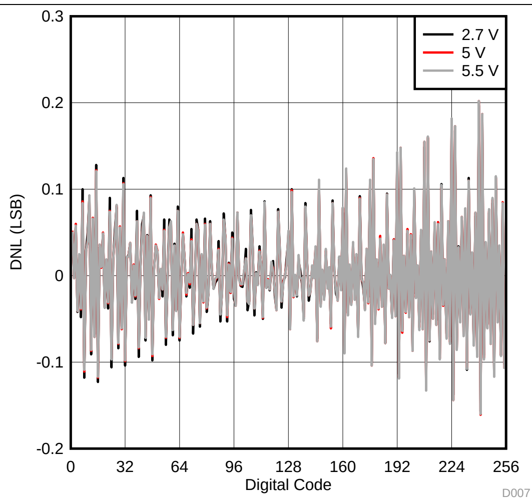


Figure 5. Voltage Divider Mode DNL vs Supply Voltage (25°C)

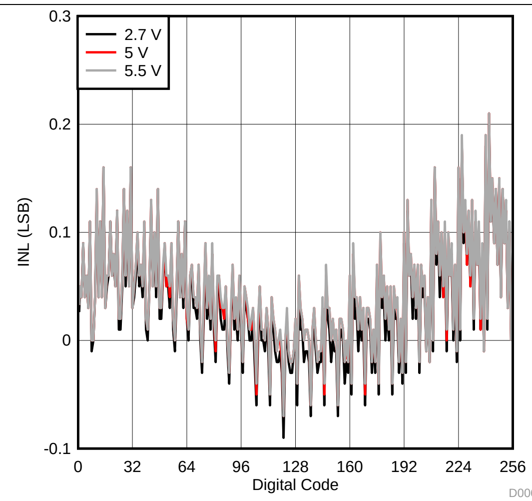


Figure 6. Voltage Divider Mode INL vs Supply Voltage (25°C)

Typical Characteristics (continued)

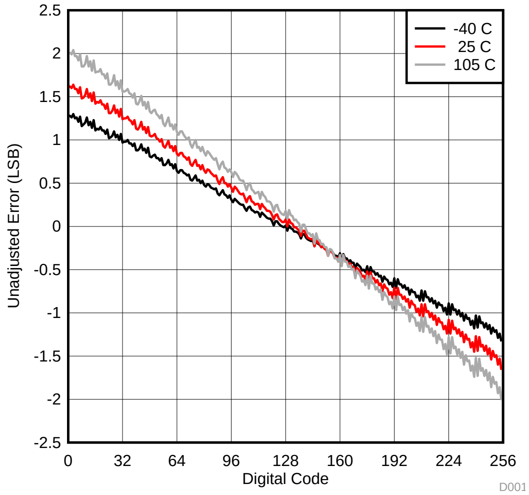


Figure 7. Voltage Divider Mode Unadjusted Error (V_{DD} = 5V)

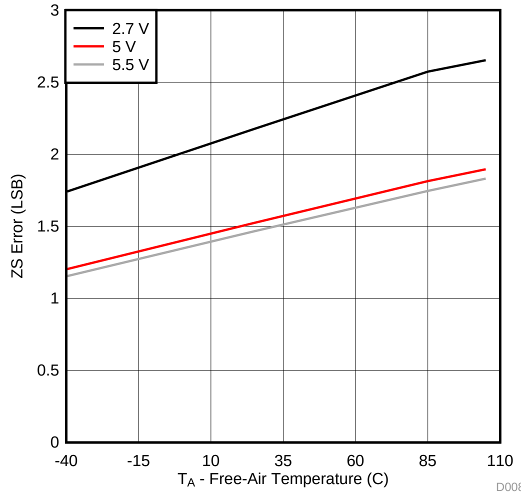


Figure 8. Voltage Divider Mode ZS Error vs Temperature

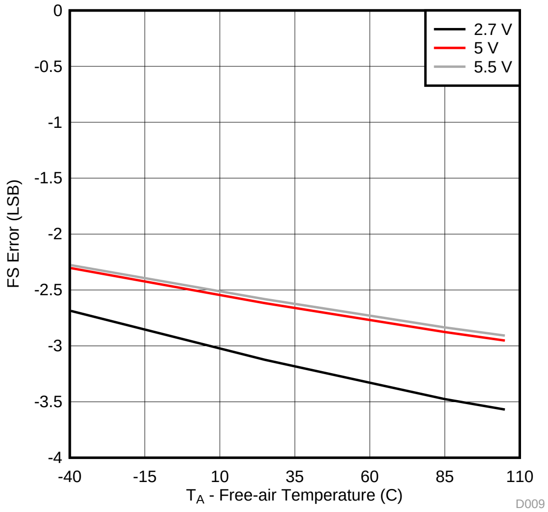


Figure 9. Voltage Divider Mode FS Error vs Temperature

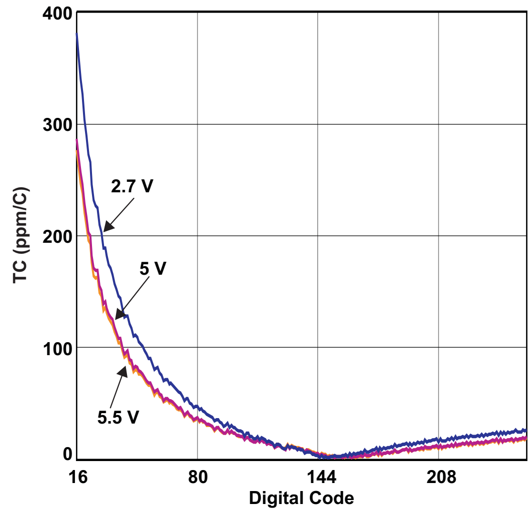


Figure 10. Voltage Divider Mode vs Digital Code

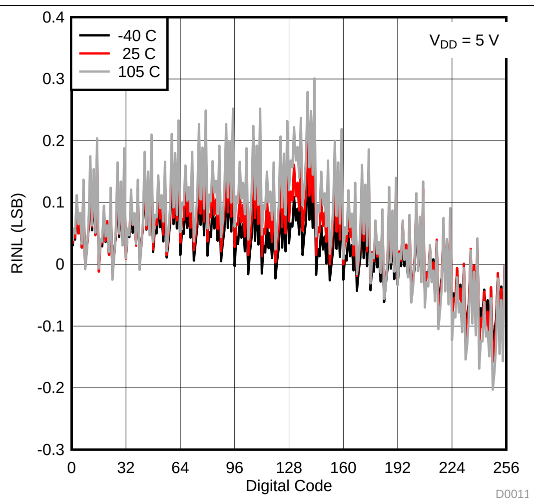


Figure 11. Rheostat Mode RINL vs Temperature (V_{DD} = 5 V)

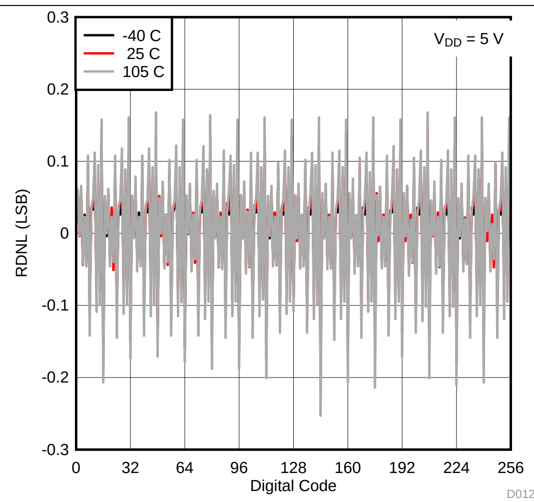


Figure 12. Rheostat Mode RDNL vs Temperature (V_{DD} = 5 V)

Typical Characteristics (continued)

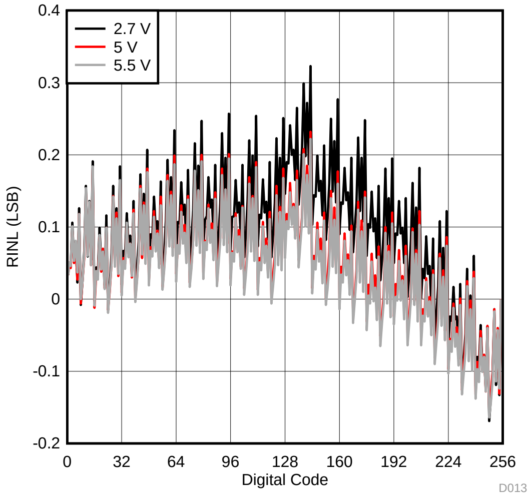


Figure 13. Rheostat Mode RINL vs Supply Voltage (25°C)

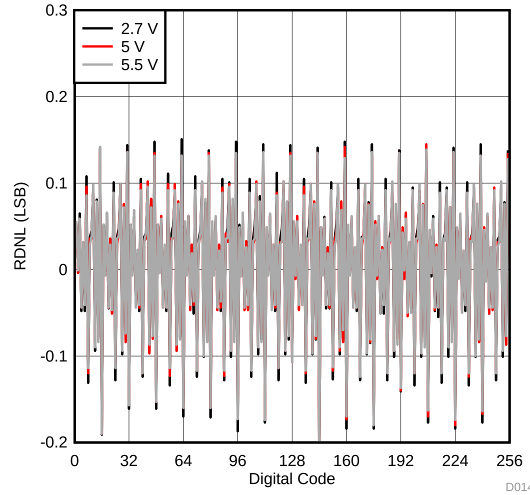


Figure 14. Rheostat Mode RDNL vs Supply Voltage (25°C)

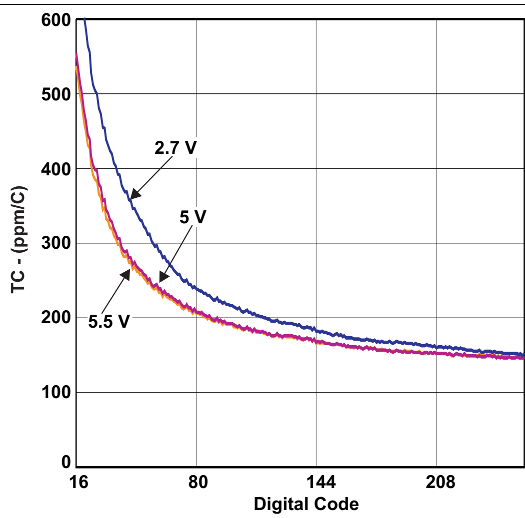


Figure 15. Rheostat Mode TC vs Digital Code

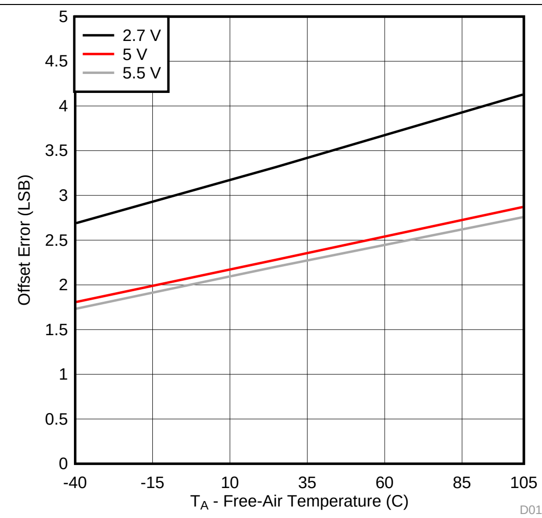


Figure 16. Rheostat Mode Offset Error vs Temperature

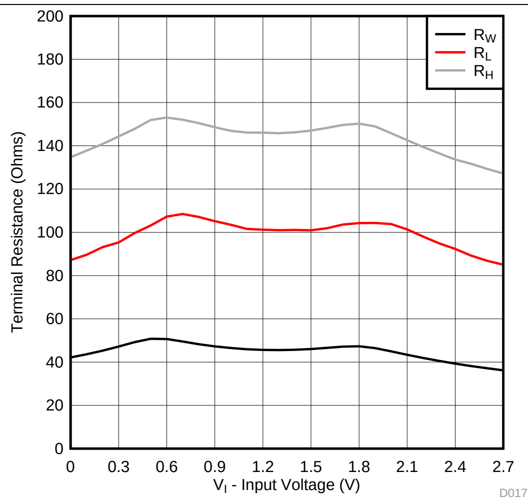


Figure 17. Wiper and Terminal Resistance (V_{DD} = 2.7 V)

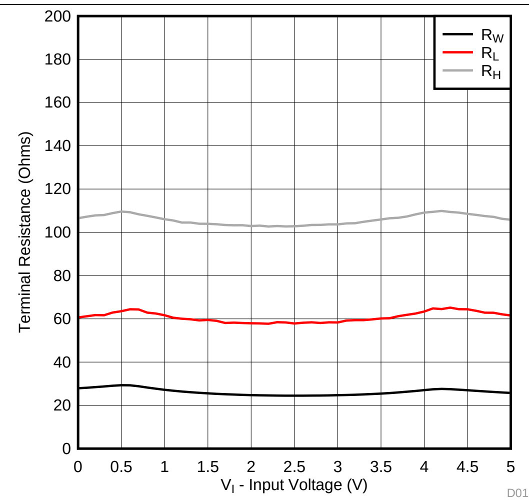


Figure 18. Wiper and Terminal Resistance (V_{DD} = 5 V)

Typical Characteristics (continued)

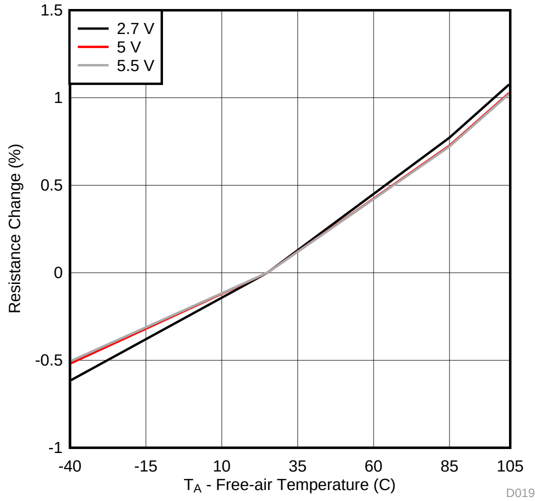


Figure 19. End-End Resistance Change vs Temperature

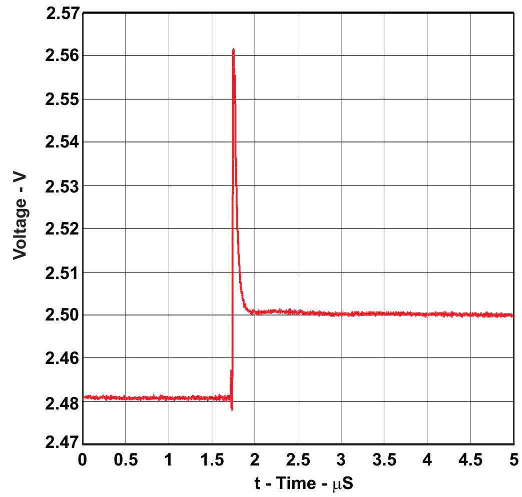


Figure 20. Midscale Wiper Glitch (Code 7fh to 80h) V_{DD} = 5 V, V_H = V_{DD}, V_L = GND, C_{load} = 10 pF

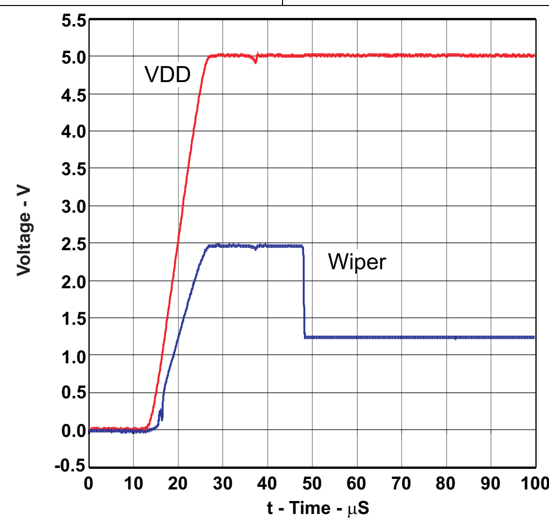


Figure 21. t_{POR} (Power-Up Response Time) Non-Volatile Memory = 40h

7 Detailed Description

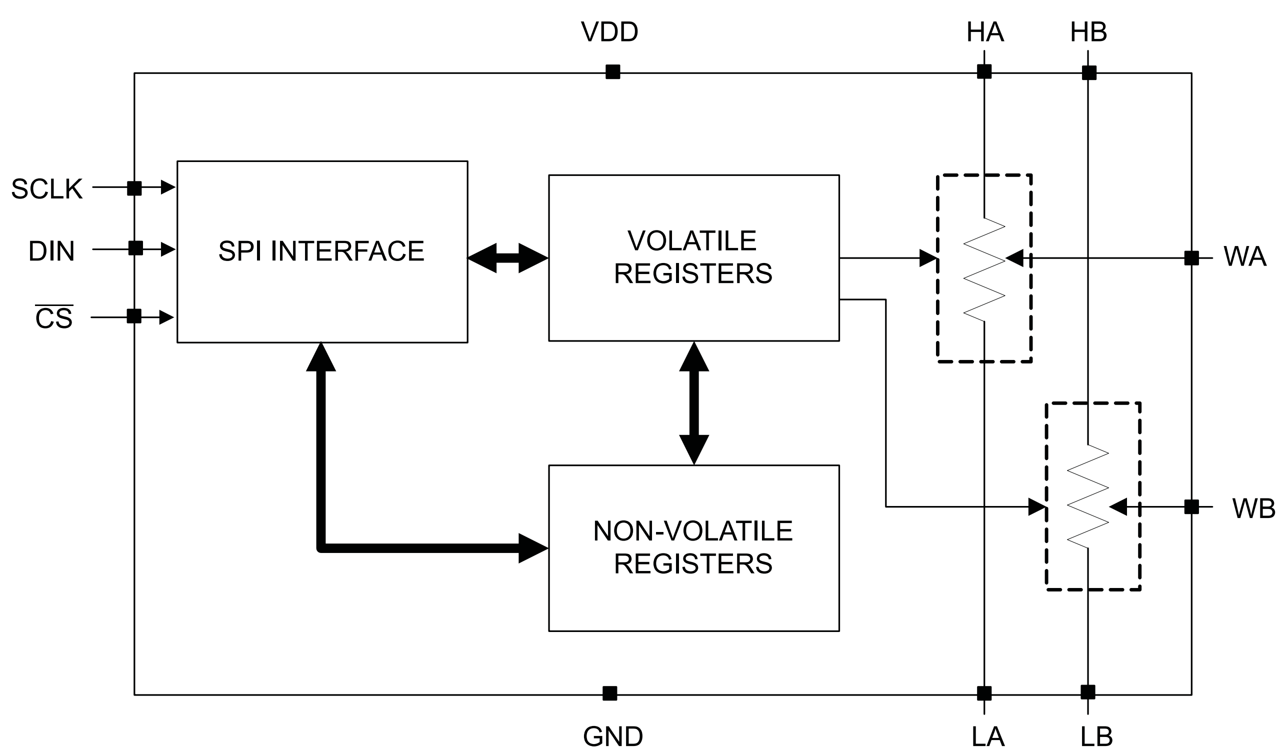
7.1 Overview

The TPL0202 has two linear-taper digital potentiometers with 256 wiper positions and an end-to-end resistance of 100 kΩ. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The two potentiometers can both be used in voltage divider mode or rheostat mode at the same time, or any combination of those modes. For example, potentiometer A can be used in voltage divider mode and potentiometer B can be used in rheostat mode. The two potentiometers are functionally independent of one another.

The high (H) and low (L) terminals of the TPL0202 are equivalent to the fixed terminals of a mechanical potentiometer. The H and L terminals do not have any polarity restrictions (H can be at a higher voltage than L, or L can be at a higher voltage than H). The position of the wiper (W) terminal is controlled by the value in the Wiper Resistance (WR) 8-bit register. When the WR register contains all zeroes (zero-scale), the wiper terminal is closest to its L terminal. As the value of the WR register increases from all zeroes to all ones (full-scale), the wiper moves from the position closest to the L terminal, to the position closest to the H terminal. At the same time, the resistance between W and L increases, whereas the resistance between W and H decreases.

The TPL0202 has non-volatile memory (EEPROM) that can be used to store the wiper position. When the device is powered down, the last value copied in the non-volatile memory (NVM) will be maintained. When power is restored, the contents of the NVM are automatically recalled and loaded into the corresponding wiper register to set the wipers. The internal registers of the TPL0202 can be written to using a SPI-compatible interface. The factory-programmed default value for the NVM is 0x80h (1000 0000). The wiper registers (volatile memory) and the NVM registers can be written to independently without having to modify the current value in another register. See the *Register Map* section for more information.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Dual Channel, 256-Position Resolution

The TPL0202 features two independent DPOTs. Each DPOT is capable of being used and controlled independently of the other one.

7.3.2 Non-Volatile Memory

The TPL0202 device features non-volatile memory which is used to store the wiper positions of both potentiometers independently. This allows the user to set the default power-up position of the wiper. By default, this is 0x80h (midscale).

7.4 Device Functional Modes

7.4.1 Voltage Divider Mode

The digital potentiometer generates a voltage divider when all three terminals are used. The voltage divider at wiper-to-H and wiper-to-L is proportional to the input voltage at H to L.

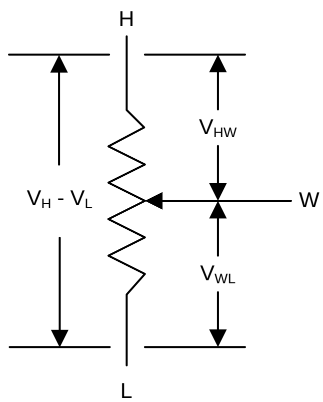


Figure 22. Equivalent Circuit for Voltage Divider Mode

For example, connecting terminal H to 5 V and terminal L to ground, the output voltage at terminal W can range from 0 V to 5 V. The general equation defining the output voltage at terminal W for any valid input voltage applied to terminal H and terminal L is:

$$V_W = V_{WL} = (V_H - V_L) \times \frac{D}{256} \quad (1)$$

The voltage difference between terminal H and terminal W can also be calculated using Equation 2.

$$V_{HW} = (V_H - V_L) \times \left(1 - \left(\frac{D}{256}\right)\right)$$

where

- D is the decimal value of the wiper code. (2)

7.4.2 Rheostat Mode

The TPL0202 operates in rheostat mode when only two terminals are used as a variable resistor. The variable resistance can either be between terminal H and terminal W or between terminal L and terminal W. The unused terminal can be left floating or it can be tied to terminal W. The nominal resistance between terminal H and terminal L is 10 kΩ and has 256 tap points accessed by the wiper terminal. The 8-bit volatile register value is used to determine one of the 256 possible wiper positions.

To set the resistance between terminal H and terminal W in rheostat mode, the potentiometer can be configured in two possible ways.

Device Functional Modes (continued)

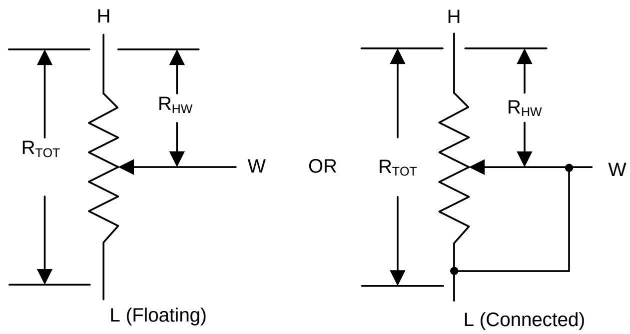


Figure 23. Equivalent Circuit for Rheostat Mode With Terminal H to Terminal W Resistance

The general equation for determining the digitally-programmed output resistance between terminal H and terminal W is:

$$R_{HW} = R_{TOT} \times \left(1 - \left(\frac{D}{256}\right)\right)$$

where
- R_{TOT} is the end-to-end resistance between terminal H and terminal L.
- D is the decimal value of the wiper code. (3)

Similarly, to set the resistance between terminal L and terminal W, the potentiometer can be configured in two possible ways.

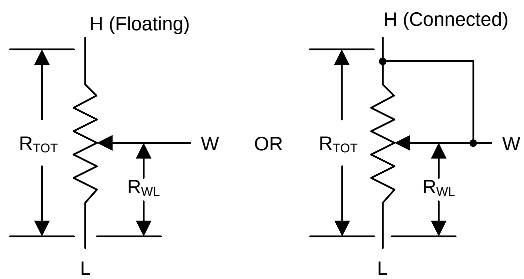


Figure 24. Equivalent Circuit for Rheostat Mode With Terminal L to Terminal W Resistance

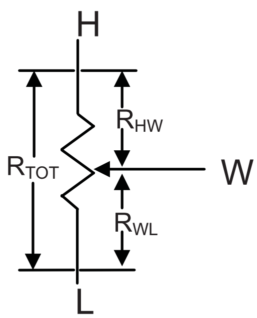
The general equation for determining the digitally-programmed output resistance between terminal L and terminal W is:

$$R_{WL} = R_{TOT} \times \frac{D}{256}$$

where
- R_{TOT} is the end-to-end resistance between terminal H and terminal L.
- D is the decimal value of the wiper code. (4)

Device Functional Modes (continued)

7.4.3 Ideal Resistance Values



$R_{WL} = R_{TOT} \times D/256$

$R_{HW} = R_{TOT} \times (1 – (D/256))$

Where D = Decimal Value of Wiper Code

Figure 25. Digital Potentiometer Measurements

Table 1 shows the ideal values for DPOT with end-to-end resistance of 10 kΩ. The absolute values of resistance can vary significantly, but the ratio (R_{WL} / R_{HW}) is extremely accurate.

Table 1. Ideal Values for DPOT

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
0	00000000	00	0.00	10.00	0.00
1	00000001	01	0.04	9.96	0.00
2	00000010	02	0.08	9.92	0.01
3	00000011	03	0.12	9.88	0.01
4	00000100	04	0.16	9.84	0.02
5	00000101	05	0.20	9.80	0.02
6	00000110	06	0.23	9.77	0.02
7	00000111	07	0.27	9.73	0.03
8	00001000	08	0.31	9.69	0.03
9	00001001	09	0.35	9.65	0.04
10	00001010	0A	0.39	9.61	0.04
11	00001011	0B	0.43	9.57	0.04
12	00001100	0C	0.47	9.53	0.05
13	00001101	0D	0.51	9.49	0.05
14	00001110	0E	0.55	9.45	0.06
15	00001111	0F	0.59	9.41	0.06
16	00010000	10	0.63	9.38	0.07
17	00010001	11	0.66	9.34	0.07
18	00010010	12	0.70	9.30	0.08
19	00010011	13	0.74	9.26	0.08
20	00010100	14	0.78	9.22	0.08
21	00010101	15	0.82	9.18	0.09
22	00010110	16	0.86	9.14	0.09
23	00010111	17	0.90	9.10	0.10
24	00011000	18	0.94	9.06	0.10
25	00011001	19	0.98	9.02	0.11
26	00011010	1A	1.02	8.98	0.11
27	00011011	1B	1.05	8.95	0.12
28	00011100	1C	1.09	8.91	0.12
29	00011101	1D	1.13	8.87	0.13

Table 1. Ideal Values for DPOT (continued)

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
30	00011110	1E	1.17	8.83	0.13
31	00011111	1F	1.21	8.79	0.14
32	00100000	20	1.25	8.75	0.14
33	00100001	21	1.29	8.71	0.15
34	00100010	22	1.33	8.67	0.15
35	00100011	23	1.37	8.63	0.16
36	00100100	24	1.41	8.59	0.16
37	00100101	25	1.45	8.55	0.17
38	00100110	26	1.48	8.52	0.17
39	00100111	27	1.52	8.48	0.18
40	00101000	28	1.56	8.44	0.19
41	00101001	29	1.60	8.40	0.19
42	00101010	2A	1.64	8.36	0.20
43	00101011	2B	1.68	8.32	0.20
44	00101100	2C	1.72	8.28	0.21
45	00101101	2D	1.76	8.24	0.21
46	00101110	2E	1.80	8.20	0.22
47	00101111	2F	1.84	8.16	0.22
48	00110000	30	1.88	8.13	0.23
49	00110001	31	1.91	8.09	0.24
50	00110010	32	1.95	8.05	0.24
51	00110011	33	1.99	8.01	0.25
52	00110100	34	2.03	7.97	0.25
53	00110101	35	2.07	7.93	0.26
54	00110110	36	2.11	7.89	0.27
55	00110111	37	2.15	7.85	0.27
56	00111000	38	2.19	7.81	0.28
57	00111001	39	2.23	7.77	0.29
58	00111010	3A	2.27	7.73	0.29
59	00111011	3B	2.30	7.70	0.30
60	00111100	3C	2.34	7.66	0.31
61	00111101	3D	2.38	7.62	0.31
62	00111110	3E	2.42	7.58	0.32
63	00111111	3F	2.46	7.54	0.33
64	01000000	40	2.50	7.50	0.33
65	01000001	41	2.54	7.46	0.34
66	01000010	42	2.58	7.42	0.35
67	01000011	43	2.62	7.38	0.35
68	01000100	44	2.66	7.34	0.36
69	01000101	45	2.70	7.30	0.37
70	01000110	46	2.73	7.27	0.38
71	01000111	47	2.77	7.23	0.38
72	01001000	48	2.81	7.19	0.39
73	01001001	49	2.85	7.15	0.40
74	01001010	4A	2.89	7.11	0.41
75	01001011	4B	2.93	7.07	0.41

Table 1. Ideal Values for DPOT (continued)

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
76	01001100	4C	2.97	7.03	0.42
77	01001101	4D	3.01	6.99	0.43
78	01001110	4E	3.05	6.95	0.44
79	01001111	4F	3.09	6.91	0.45
80	01010000	50	3.13	6.88	0.45
81	01010001	51	3.16	6.84	0.46
82	01010010	52	3.20	6.80	0.47
83	01010011	53	3.24	6.76	0.48
84	01010100	54	3.28	6.72	0.49
85	01010101	55	3.32	6.68	0.50
86	01010110	56	3.36	6.64	0.51
87	01010111	57	3.40	6.60	0.51
88	01011000	58	3.44	6.56	0.52
89	01011001	59	3.48	6.52	0.53
90	01011010	5A	3.52	6.48	0.54
91	01011011	5B	3.55	6.45	0.55
92	01011100	5C	3.59	6.41	0.56
93	01011101	5D	3.63	6.37	0.57
94	01011110	5E	3.67	6.33	0.58
95	01011111	5F	3.71	6.29	0.59
96	01100000	60	3.75	6.25	0.60
97	01100001	61	3.79	6.21	0.61
98	01100010	62	3.83	6.17	0.62
99	01100011	63	3.87	6.13	0.63
100	01100100	64	3.91	6.09	0.64
101	01100101	65	3.95	6.05	0.65
102	01100110	66	3.98	6.02	0.66
103	01100111	67	4.02	5.98	0.67
104	01101000	68	4.06	5.94	0.68
105	01101001	69	4.10	5.90	0.70
106	01101010	6A	4.14	5.86	0.71
107	01101011	6B	4.18	5.82	0.72
108	01101100	6C	4.22	5.78	0.73
109	01101101	6D	4.26	5.74	0.74
110	01101110	6E	4.30	5.70	0.75
111	01101111	6F	4.34	5.66	0.77
112	01110000	70	4.38	5.63	0.78
113	01110001	71	4.41	5.59	0.79
114	01110010	72	4.45	5.55	0.80
115	01110011	73	4.49	5.51	0.82
116	01110100	74	4.53	5.47	0.83
117	01110101	75	4.57	5.43	0.84
118	01110110	76	4.61	5.39	0.86
119	01110111	77	4.65	5.35	0.87
120	01111000	78	4.69	5.31	0.88
121	01111001	79	4.73	5.27	0.90

Table 1. Ideal Values for DPOT (continued)

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
122	01111010	7A	4.77	5.23	0.91
123	01111011	7B	4.80	5.20	0.92
124	01111100	7C	4.84	5.16	0.94
125	01111101	7D	4.88	5.12	0.95
126	01111110	7E	4.92	5.08	0.97
127	01111111	7F	4.96	5.04	0.98
128	10000000	80	5.00	5.00	1.00
129	10000001	81	5.04	4.96	1.02
130	10000010	82	5.08	4.92	1.03
131	10000011	83	5.12	4.88	1.05
132	10000100	84	5.16	4.84	1.06
133	10000101	85	5.20	4.80	1.08
134	10000110	86	5.23	4.77	1.10
135	10000111	87	5.27	4.73	1.12
136	10001000	88	5.31	4.69	1.13
137	10001001	89	5.35	4.65	1.15
138	10001010	8A	5.39	4.61	1.17
139	10001011	8B	5.43	4.57	1.19
140	10001100	8C	5.47	4.53	1.21
141	10001101	8D	5.51	4.49	1.23
142	10001110	8E	5.55	4.45	1.25
143	10001111	8F	5.59	4.41	1.27
144	10010000	90	5.63	4.38	1.29
145	10010001	91	5.66	4.34	1.31
146	10010010	92	5.70	4.30	1.33
147	10010011	93	5.74	4.26	1.35
148	10010100	94	5.78	4.22	1.37
149	10010101	95	5.82	4.18	1.39
150	10010110	96	5.86	4.14	1.42
151	10010111	97	5.90	4.10	1.44
152	10011000	98	5.94	4.06	1.46
153	10011001	99	5.98	4.02	1.49
154	10011010	9A	6.02	3.98	1.51
155	10011011	9B	6.05	3.95	1.53
156	10011100	9C	6.09	3.91	1.56
157	10011101	9D	6.13	3.87	1.59
158	10011110	9E	6.17	3.83	1.61
159	10011111	9F	6.21	3.79	1.64
160	10100000	A0	6.25	3.75	1.67
161	10100001	A1	6.29	3.71	1.69
162	10100010	A2	6.33	3.67	1.72
163	10100011	A3	6.37	3.63	1.75
164	10100100	A4	6.41	3.59	1.78
165	10100101	A5	6.45	3.55	1.81
166	10100110	A6	6.48	3.52	1.84
167	10100111	A7	6.52	3.48	1.88

Table 1. Ideal Values for DPOT (continued)

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
168	10101000	A8	6.56	3.44	1.91
169	10101001	A9	6.60	3.40	1.94
170	10101010	AA	6.64	3.36	1.98
171	10101011	AB	6.68	3.32	2.01
172	10101100	AC	6.72	3.28	2.05
173	10101101	AD	6.76	3.24	2.08
174	10101110	AE	6.80	3.20	2.12
175	10101111	AF	6.84	3.16	2.16
176	10110000	B0	6.88	3.13	2.20
177	10110001	B1	6.91	3.09	2.24
178	10110010	B2	6.95	3.05	2.28
179	10110011	B3	6.99	3.01	2.32
180	10110100	B4	7.03	2.97	2.37
181	10110101	B5	7.07	2.93	2.41
182	10110110	B6	7.11	2.89	2.46
183	10110111	B7	7.15	2.85	2.51
184	10111000	B8	7.19	2.81	2.56
185	10111001	B9	7.23	2.77	2.61
186	10111010	BA	7.27	2.73	2.66
187	10111011	BB	7.30	2.70	2.71
188	10111100	BC	7.34	2.66	2.76
189	10111101	BD	7.38	2.62	2.82
190	10111110	BE	7.42	2.58	2.88
191	10111111	BF	7.46	2.54	2.94
192	11000000	C0	7.50	2.50	3.00
193	11000001	C1	7.54	2.46	3.06
194	11000010	C2	7.58	2.42	3.13
195	11000011	C3	7.62	2.38	3.20
196	11000100	C4	7.66	2.34	3.27
197	11000101	C5	7.70	2.30	3.34
198	11000110	C6	7.73	2.27	3.41
199	11000111	C7	7.77	2.23	3.49
200	11001000	C8	7.81	2.19	3.57
201	11001001	C9	7.85	2.15	3.65
202	11001010	CA	7.89	2.11	3.74
203	11001011	CB	7.93	2.07	3.83
204	11001100	CC	7.97	2.03	3.92
205	11001101	CD	8.01	1.99	4.02
206	11001110	CE	8.05	1.95	4.12
207	11001111	CF	8.09	1.91	4.22
208	11010000	D0	8.13	1.88	4.33
209	11010001	D1	8.16	1.84	4.45
210	11010010	D2	8.20	1.80	4.57
211	11010011	D3	8.24	1.76	4.69
212	11010100	D4	8.28	1.72	4.82
213	11010101	D5	8.32	1.68	4.95

Table 1. Ideal Values for DPOT (continued)

STEP	BINARY	HEX	10 kΩ		R_{WL} / R_{HW}
			R_{WL}	R_{HW}	
214	11010110	D6	8.36	1.64	5.10
215	11010111	D7	8.40	1.60	5.24
216	11011000	D8	8.44	1.56	5.40
217	11011001	D9	8.48	1.52	5.56
218	11011010	DA	8.52	1.48	5.74
219	11011011	DB	8.55	1.45	5.92
220	11011100	DC	8.59	1.41	6.11
221	11011101	DD	8.63	1.37	6.31
222	11011110	DE	8.67	1.33	6.53
223	11011111	DF	8.71	1.29	6.76
224	11100000	E0	8.75	1.25	7.00
225	11100001	E1	8.79	1.21	7.26
226	11100010	E2	8.83	1.17	7.53
227	11100011	E3	8.87	1.13	7.83
228	11100100	E4	8.91	1.09	8.14
229	11100101	E5	8.95	1.05	8.48
230	11100110	E6	8.98	1.02	8.85
231	11100111	E7	9.02	0.98	9.24
232	11101000	E8	9.06	0.94	9.67
233	11101001	E9	9.10	0.90	10.13
234	11101010	EA	9.14	0.86	10.64
235	11101011	EB	9.18	0.82	11.19
236	11101100	EC	9.22	0.78	11.80
237	11101101	ED	9.26	0.74	12.47
238	11101110	EE	9.30	0.70	13.22
239	11101111	EF	9.34	0.66	14.06
240	11110000	F0	9.38	0.63	15.00
241	11110001	F1	9.41	0.59	16.07
242	11110010	F2	9.45	0.55	17.29
243	11110011	F3	9.49	0.51	18.69
244	11110100	F4	9.53	0.47	20.33
245	11110101	F5	9.57	0.43	22.27
246	11110110	F6	9.61	0.39	24.60
247	11110111	F7	9.65	0.35	27.44
248	11111000	F8	9.69	0.31	31.00
249	11111001	F9	9.73	0.27	35.57
250	11111010	FA	9.77	0.23	41.67
251	11111011	FB	9.80	0.20	50.20
252	11111100	FC	9.84	0.16	63.00
253	11111101	FD	9.88	0.12	84.33
254	11111110	FE	9.92	0.08	127.00
255	11111111	FF	9.96	0.04	255.00

7.5 Programming

7.5.1 SPI Digital Interface

The TPL0202 uses a 3-wire SPI-compatible serial data interface. This write-only interface has three inputs: chip-select ($\overline{CS}$), data clock (SCLK), and data input (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge. The WRITE commands (C1, C0 = 00 or 01) require 16 clock cycles to clock in the command, address, and data. The COPY commands (C1, C0 = 10 or 11) can use either eight clock cycles to transfer only command and address bits or 16 clock cycles, with the device disregarding 8 data bits. After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial data stream to avoid corruption of the data.

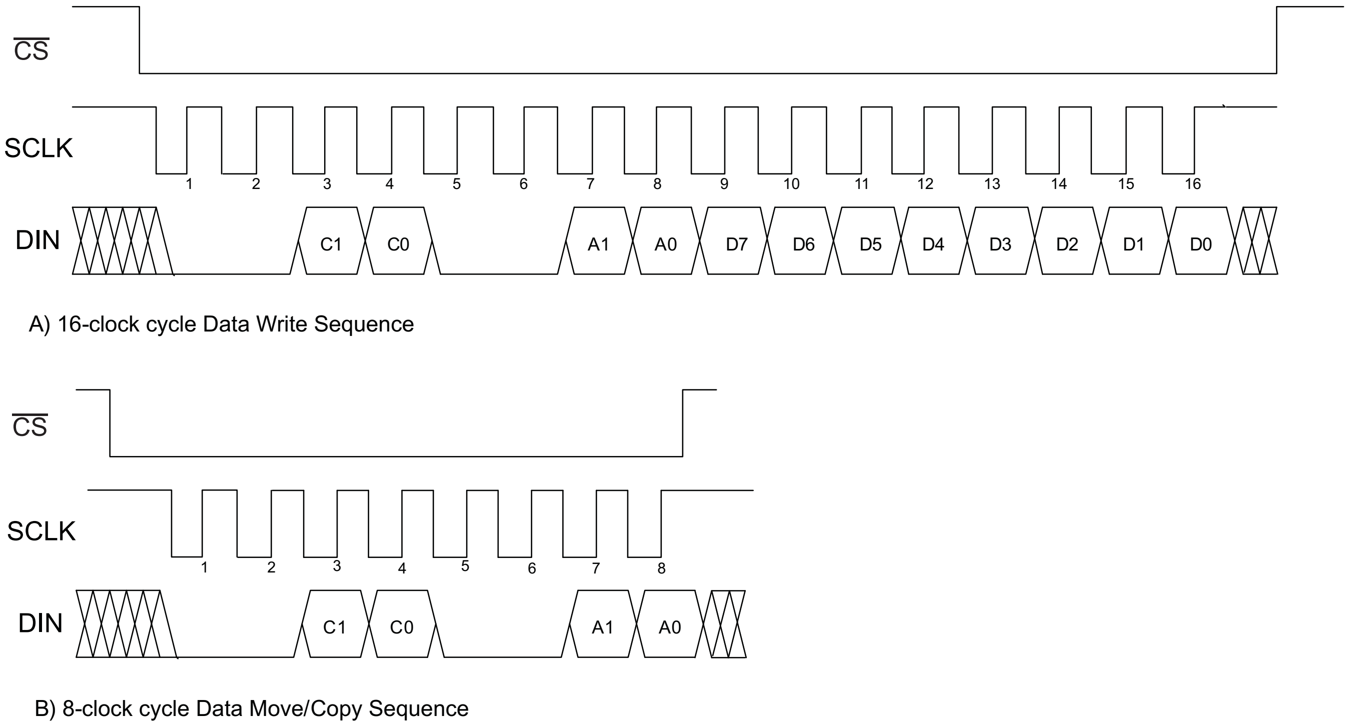


Figure 26. Digital Interface Write Sequence

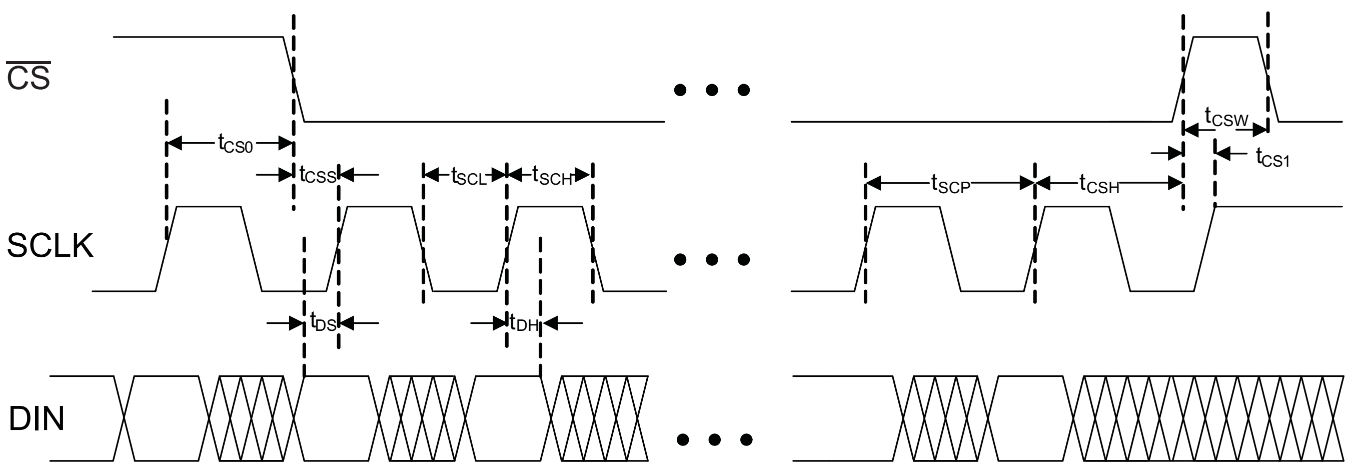


Figure 27. Digital Interface Timing Diagram

7.6 Register Map

Table 2. Register Map

CLOCK EDGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	–	–	C1	C0	–	–	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A	0	0	0	0	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register B	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Wiper Register A and B	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register A	0	0	0	1	0	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register B	0	0	0	1	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write NV Register A and B	0	0	0	1	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Copy Wiper Register A to NV Register A	0	0	1	0	0	0	0	1	–	–	–	–	–	–	–	–
Copy Wiper Register B to NV Register B	0	0	1	0	0	0	1	0	–	–	–	–	–	–	–	–
Copy Both Wiper Registers to NV Registers	0	0	1	0	0	0	1	1	–	–	–	–	–	–	–	–
Copy NV Register A to Wiper Register A	0	0	1	1	0	0	0	1	–	–	–	–	–	–	–	–
Copy NV Register B to Wiper Register A	0	0	1	1	0	0	1	0	–	–	–	–	–	–	–	–
Copy Both NV Registers to Wiper Registers	0	0	1	1	0	0	1	1	–	–	–	–	–	–	–	–

7.6.1 Digital Interface Format

The data format consists of three elements: command bits, address bits, and data bits. The command bits (C1 and C0) indicate the action to be taken such as changing or storing the wiper position. The address bits (A1 and A0) specify which potentiometer the command affects and the 8 data bits (D7 to D0) specify the wiper position.

7.6.2 Write-Wiper Register (Command 00)

Data written to the write-wiper registers (C1, C0 = 00) controls the wiper positions. The 8 data bits (D7 to D0) indicate the position of the wiper. If DIN = 0x00h, the wiper moves to the position closest to the L terminal. If DIN = 0xFFh, the wiper moves to the position closest to the H terminal. This command writes data to the volatile RAM, leaving the NV registers unchanged. When the device powers up, the data stored in the NV registers transfers to the volatile wiper register, moving the wiper to the stored position

7.6.3 Write-NV Register (Command 01)

This command (C1, C0 = 01) stores the position of the wipers to the NV registers for use at power-up. Alternatively, the *copy wiper register to NV register* command can be used to store the position of the wipers to the NV registers. Writing to the NV registers does not affect the position of the wipers.

7.6.4 Copy Wiper Register to NV Register (Command 10)

This command (C1, C0 = 10) stores the current position of the wiper to the NV register, for use at power-up. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0. Alternatively, the *write NV register* command can be used to store the current position of the wiper to the NV register.

7.6.5 Copy NV Register to Wiper Register (Command 11)

This command (C1, C0 = 11) restores the wiper position to the previously stored position in the NV register. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Many applications require using a digital potentiometer such as the TPL0202 for variable resistance or voltage division; the following application shows a few examples. In conjunction with various amplifiers, the TPL0202 can effectively be used in rheostat mode to modify the gain of an amplifier, in voltage divider mode to create a digital-to-analog converter (DAC), or one of the potentiometers can be used in voltage divider mode while the other is in rheostat mode to create a variable current sink.

Digital potentiometers have additional use cases. See the *Related Documentation* section for additional resources that have application examples including adjustable current source and gain adjustment.

8.2 Typical Application

The following typical application shows a DAC.

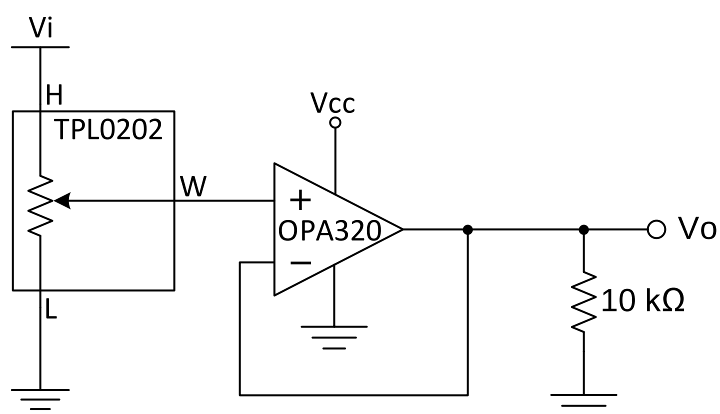


Figure 28. DAC Schematic

8.2.1 Design Requirements

Table 3 shows the design parameters for this application.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0 to 5 V
Output voltage range	0 to 5 V

8.2.2 Detailed Design Procedure

The TPL0202 can be used in voltage divider mode with a unity-gain operational amplifier buffer to create an 8-bit DAC. The analog output voltage of the circuit is determined by the wiper setting programmed through the I^2C bus.

The operational amplifier is required to buffer the high-impedance output of the TPL0202 or else loading placed on the output of the voltage divider will affect the output voltage.

8.2.3 Application Curve

The voltage at terminal H determines the maximum analog voltage at the output. As the TPL0202 moves from zero-scale to full-scale, the voltage divider adjusts with relation to the voltage divider formula (Equation 1), resulting in the desired voltage at terminal W. The voltage at terminal W will range linearly from 0 V to the terminal H voltage. In this example, Vin at terminal H is 5 V and 2.7 V.

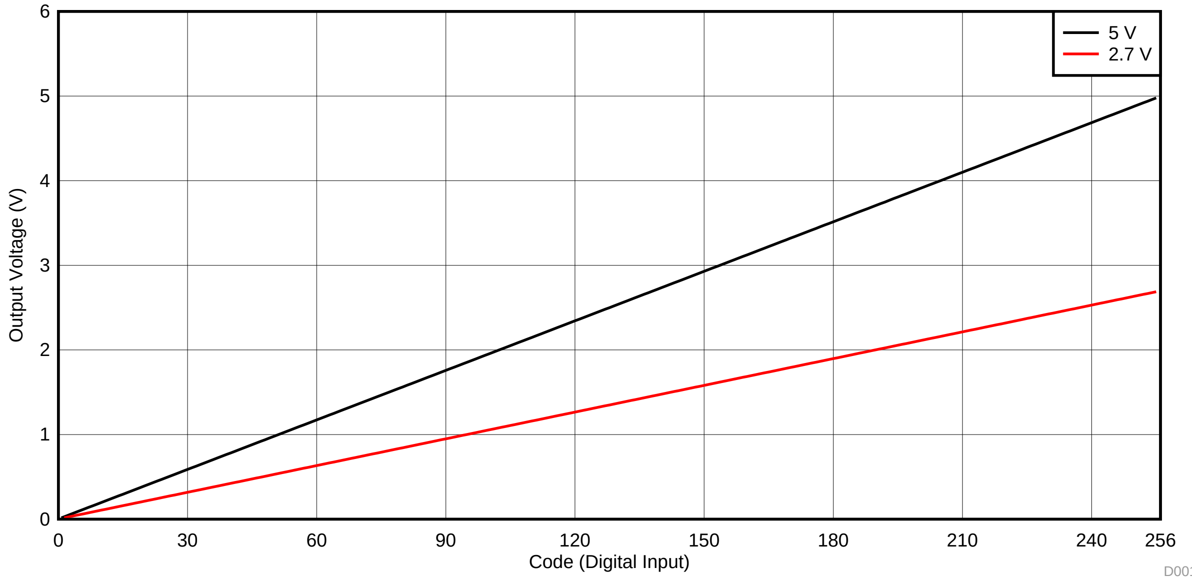


Figure 29. TPL0202 Digital Input vs OPA320 Analog Output (DAC)

9 Power Supply Recommendations

9.1 Power Sequence

Protection diodes limit the voltage compliance at terminal H, terminal L, and terminal W, making it important to power up V_{DD} first before applying any voltage to terminal H, terminal L, and terminal W. The diodes are forward-biasing, meaning V_{DD} can be powered unintentionally if V_{DD} is not powered first. The ideal power-up sequence is V_{DD}, digital inputs, and V_H, V_L, and V_W. The order of powering digital inputs, V_H, V_L, and V_W does not matter as long as they are powered after V_{DD}.

9.2 Wiper Position Upon Power Up

It is prudent to know that when the DPOT is powered off, the impedance of the device is not known. Upon power-up, the device will go to 0x80h code for a brief period of time while it loads the stored wiper position from the EEPROM, then goes to the stored position. This process happens in less than 100 µs.

10 Layout

10.1 Layout Guidelines

To ensure reliability of the device, follow common printed-circuit board (PCB) layout guidelines.

- Leads to the input should be as direct as possible with a minimum conductor length.
- The ground path should have low resistance and low inductance.
- Use short trace-lengths to avoid excessive loading.
- It is common to have a dedicated ground plane on an inner layer of the board.
- Terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias.
- Use bypass capacitors on power supplies and placed them as close as possible to the VDD pin.
- Apply low equivalent series resistance (0.1 µF to 10 µF tantalum or electrolytic capacitors) at the supplies to minimize transient disturbances and to filter low frequency ripple.
- To reduce the total I^{2}C bus capacitance added by PCB parasitics, data lines (SCL and SDA) should be as short as possible and the widths of the traces should also be minimized (for example, 5 to 10 mils depending on copper weight).

10.2 Layout Example

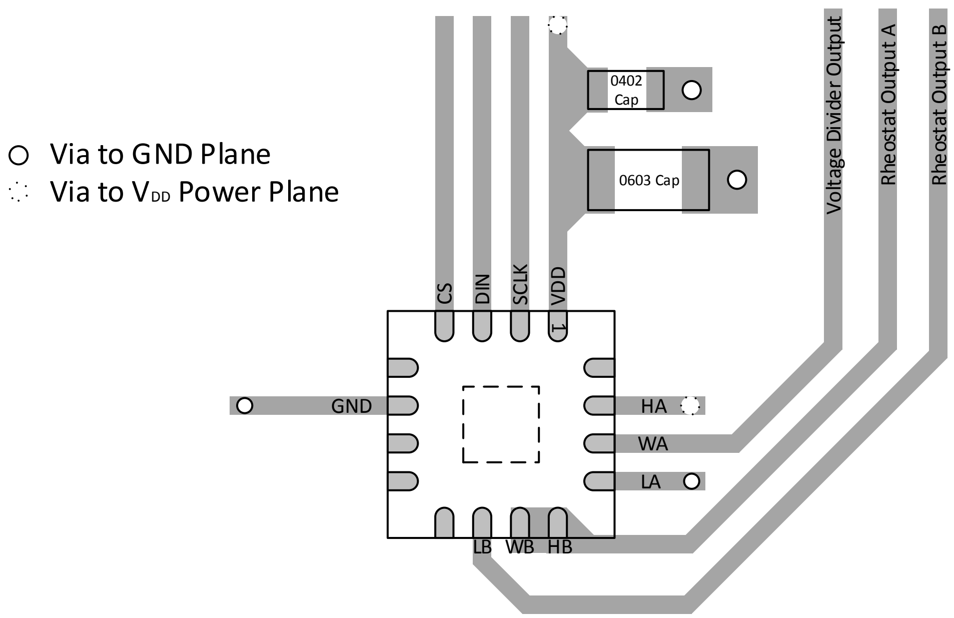


Figure 30. Example Layout for RTE Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TPL0102 Two 256-Taps Digital Potentiometers With Non-Volatile Memory (SLIS134)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL0202-10MRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZUR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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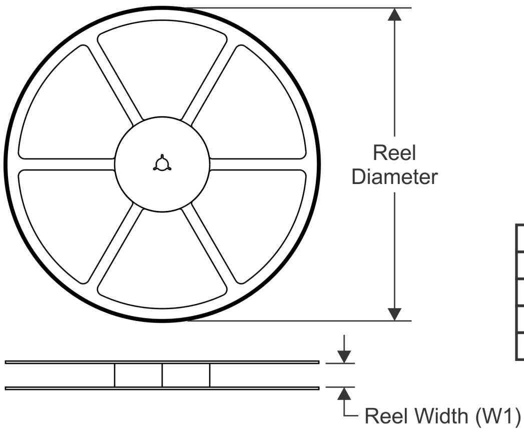
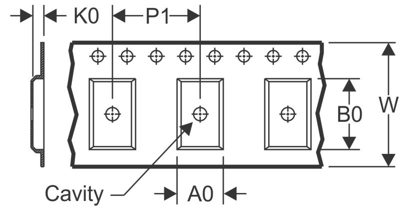
TAPE AND REEL INFORMATION

REEL DIMENSIONS

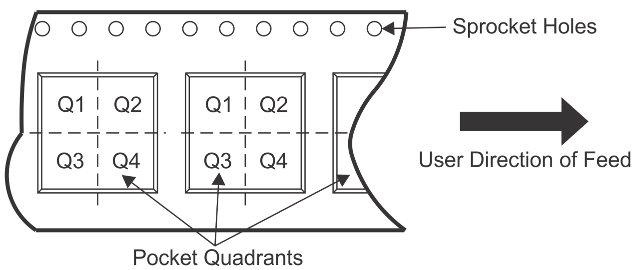


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

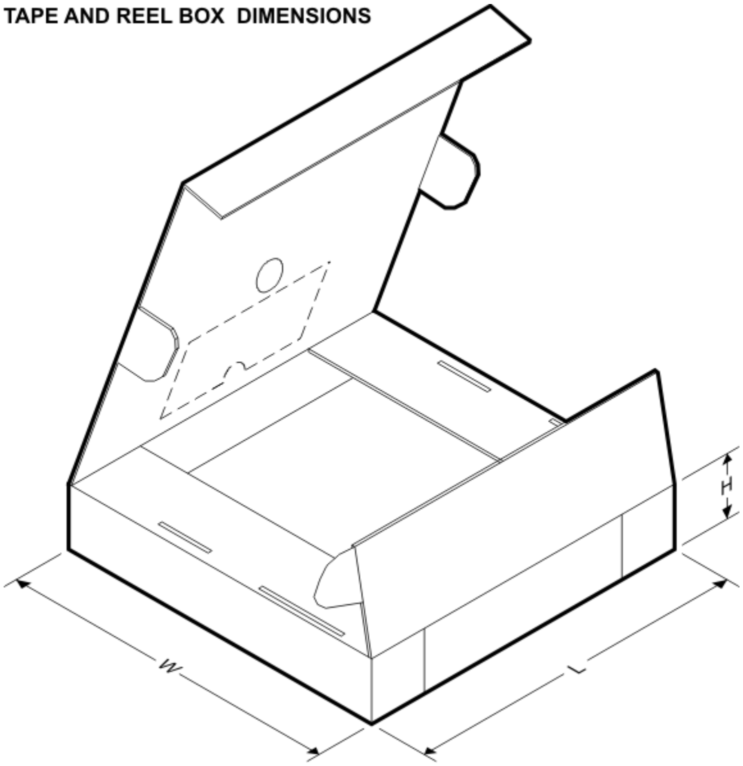
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0202-10MRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

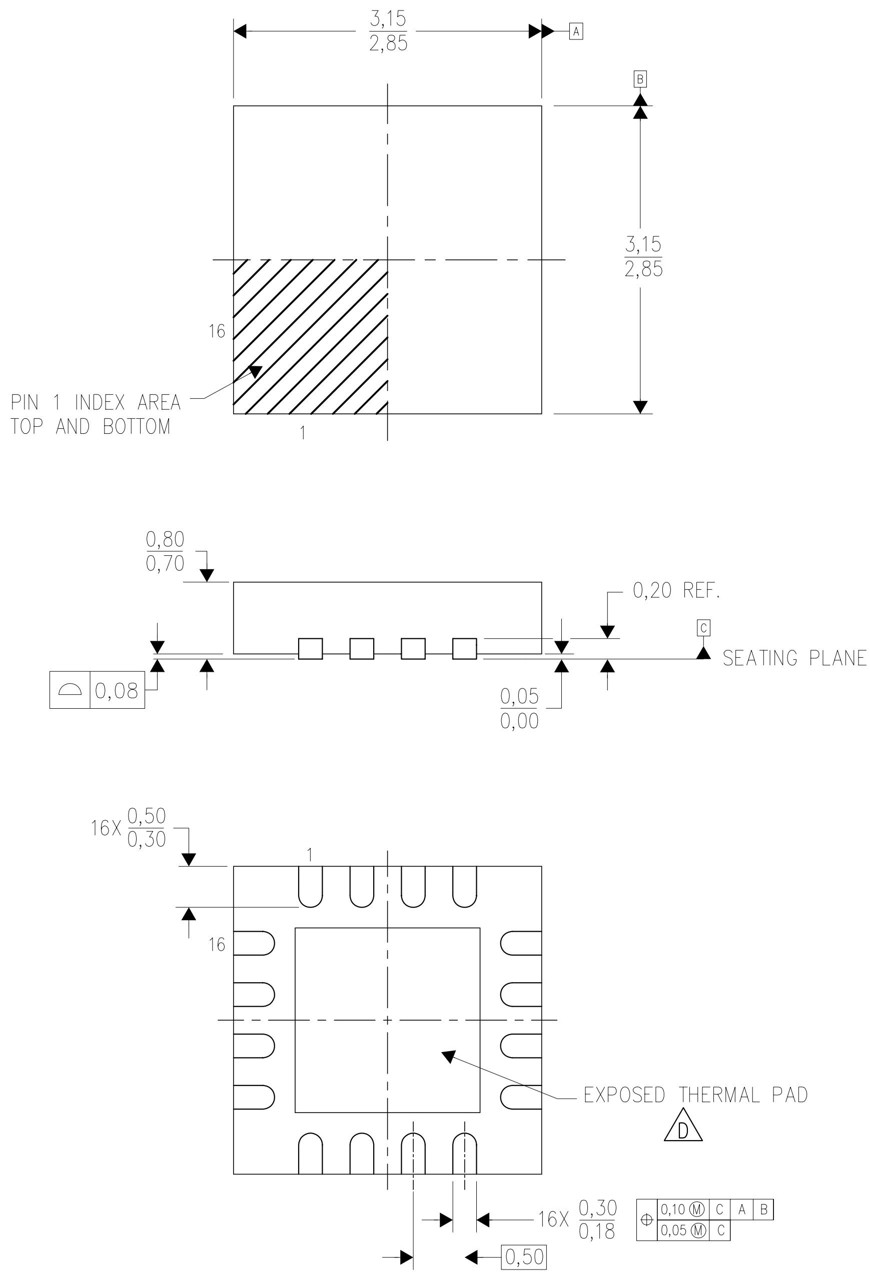
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0202-10MRTER	WQFN	RTE	16	3000	370.0	355.0	55.0

RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

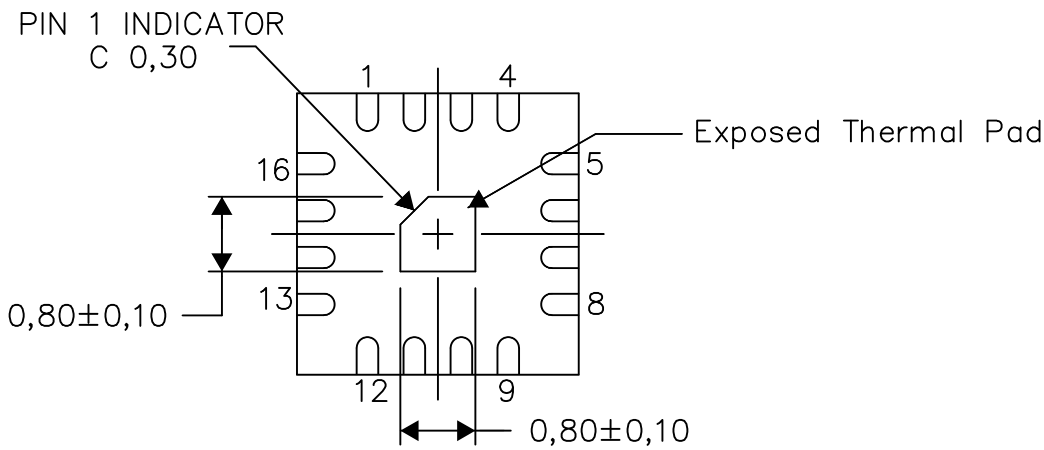
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



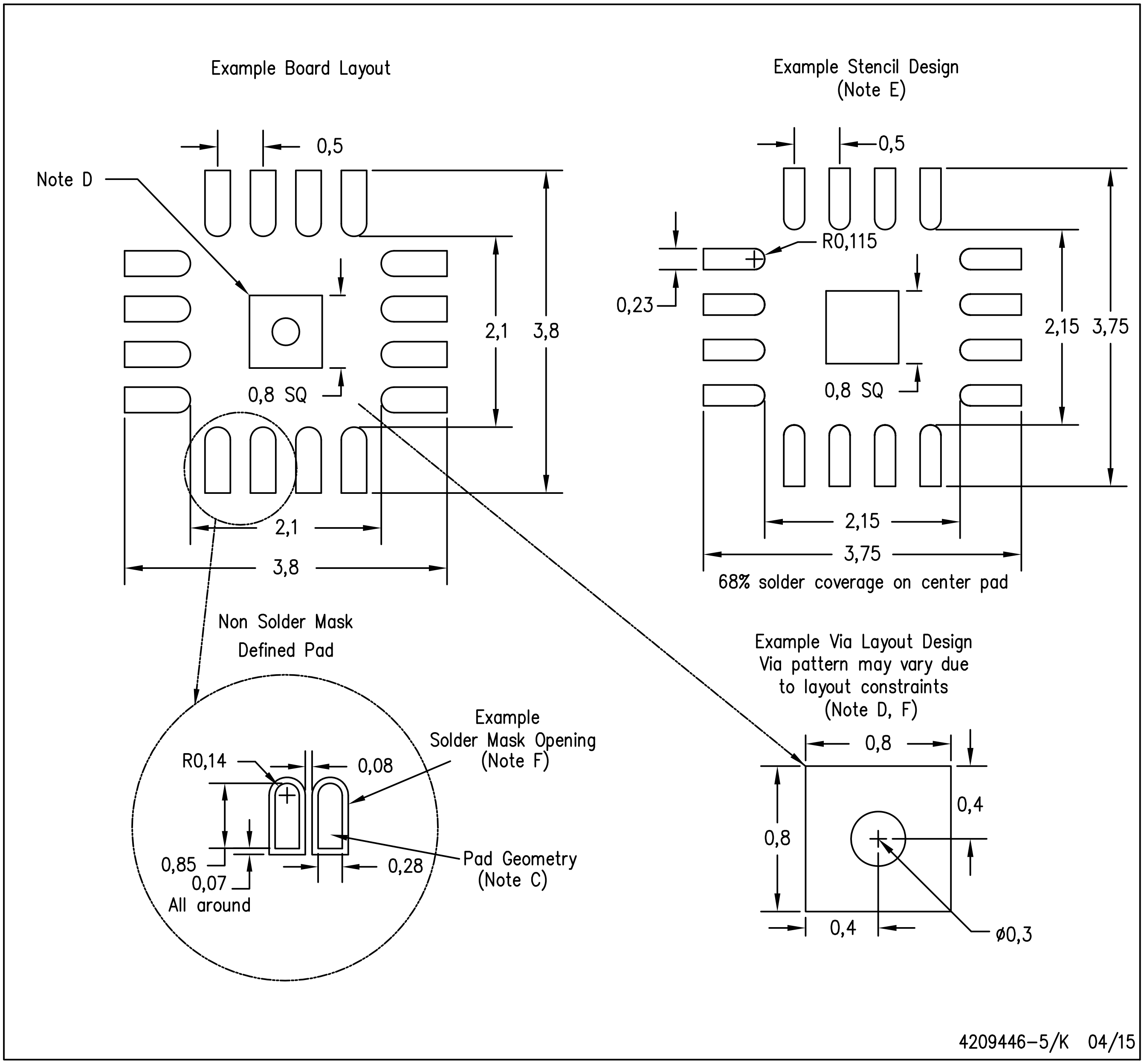
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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