# SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR
WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

Check for Samples: SN74AUP1T57

FEATURES

- **Available in the Texas Instruments NanoStar™ Packages**
- **Single-Supply Voltage Translator**
- **1.8 V to 3.3 V (at V_{CC} = 3.3 V)**
- **2.5 V to 3.3 V (at V_{CC} = 3.3 V)**
- **1.8 V to 2.5 V (at V_{CC} = 2.5 V)**
- **3.3 V to 2.5 V (at V_{CC} = 2.5 V)**
- **Nine Configurable Gate Logic Functions**
- **Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity**
- **I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μA)**
- **Very Low Static and Dynamic Power Consumption**
- **Pb-Free Packages Available: SON (DRY or DSF), SOT-23 (DBV), SC-70 (DCK), and NanoStar WCSP**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Related Devices: SN74AUP1T58, SN74AUP1T97, and SN74AUP1T98**

DBV OR DCK PACKAGE
(TOP VIEW)
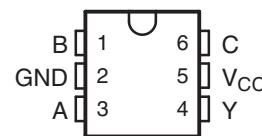
DRY OR DSF PACKAGE
(TOP VIEW)
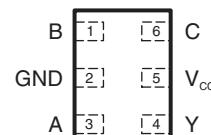
YFP OR YZP PACKAGE
(TOP VIEW)
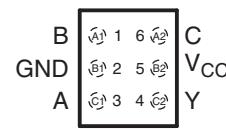
DESCRIPTION/ORDERING INFORMATION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T57 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVCMOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs (ΔV_T = 210 mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T57 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

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NanoStar is a trademark of Texas Instruments.

I_{off} is a feature that allows for powered-down conditions (V_{CC} = 0 V) and is important in portable and mobile applications. When V_{CC} = 0 V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.

The SN74AUP1T57 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1T57YZPR	_ _ _TG_
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP	Reel of 3000	SN74AUP1T57YFPR	_ _ _TG_
	QFN – DRY	Reel of 5000	SN74AUP1T57DRYR	TG
	uQFN – DSF	Reel of 5000	SN74AUP1T57DSFR	TG
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1T57DBVR	HT3_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1T57DCKR	TG_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-input AND gate	5
2-input NOR gate with both inputs inverted	5
2-input NAND gate with inverted input	6, 7
2-input OR gate with inverted input	6, 7
2-input AND gate with both inputs inverted	8
2-input NOR gate	8
2-input XNOR gate	9
Inverter	10
Noninverted buffer	11
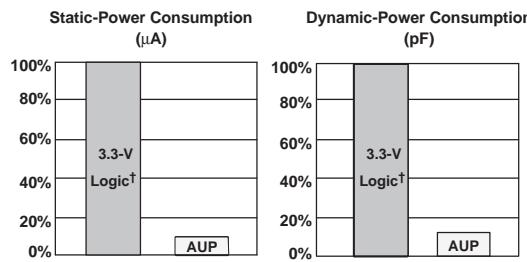
† Single, dual, and triple gates

Figure 1. AUP – The Lowest-Power Family
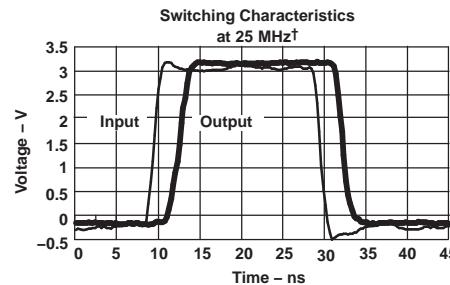
† AUP1G08 data at C_L = 15 pF

Figure 2. Excellent Signal Integrity

Product Folder Link(s): *SN74AUP1T57*
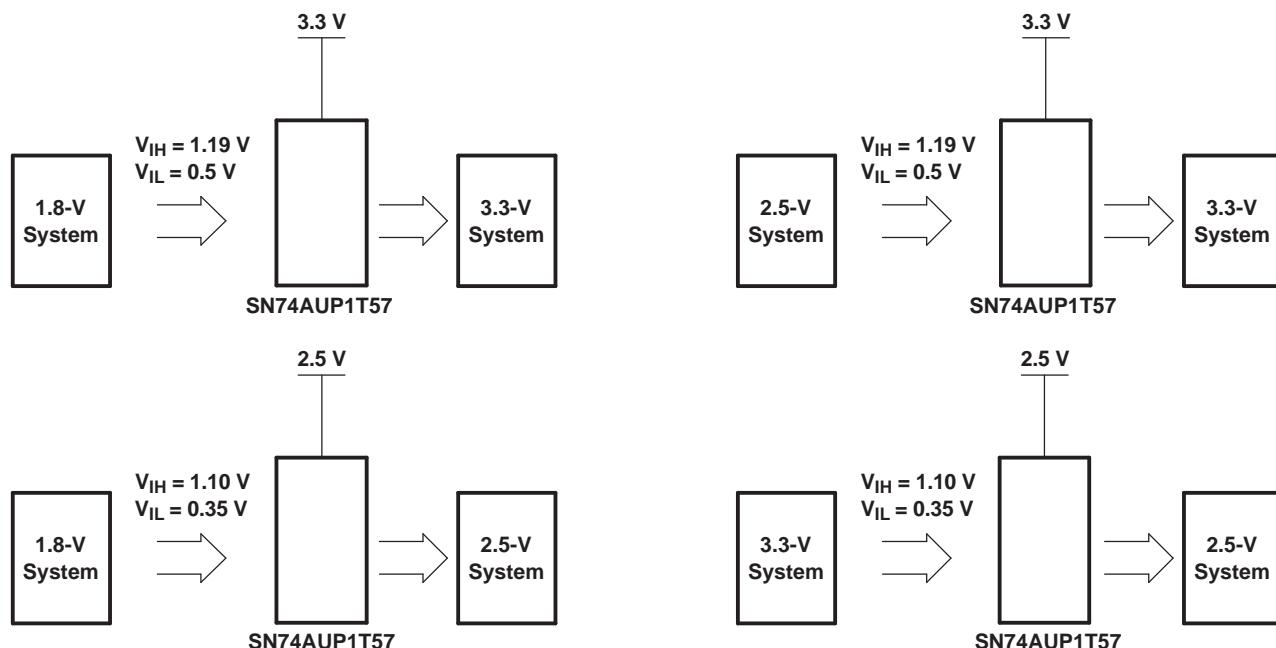
Figure 3. Possible Voltage-Translation Combinations
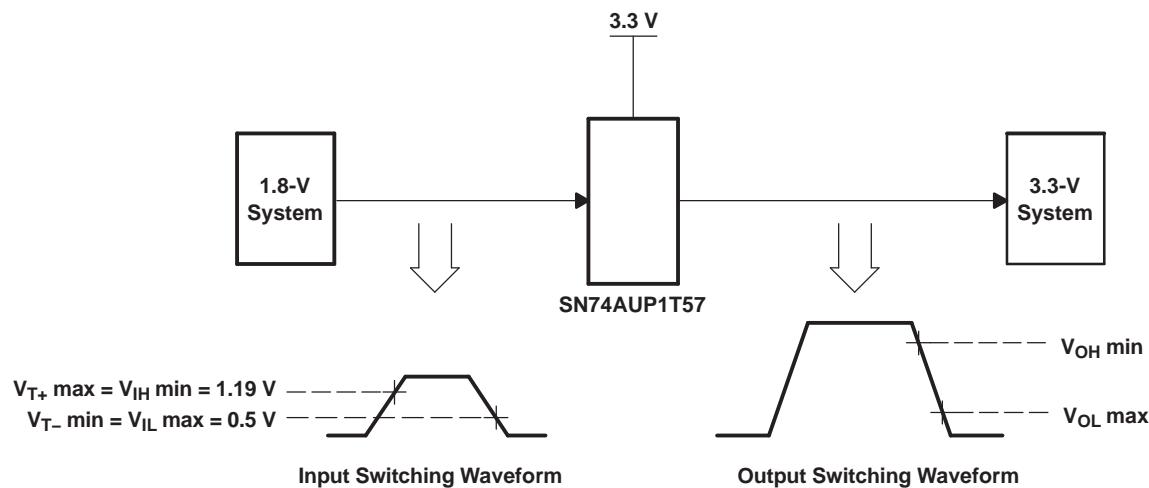
Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

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FUNCTION TABLE

INPUTS			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)
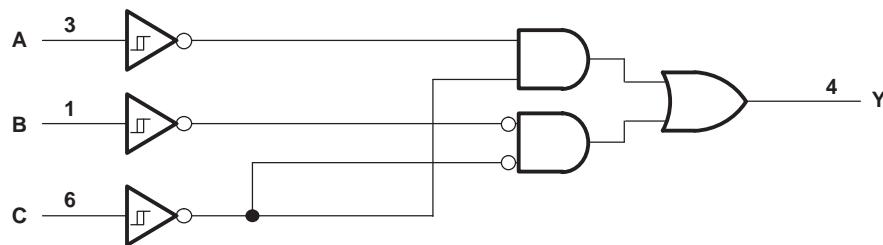
LOGIC CONFIGURATIONS
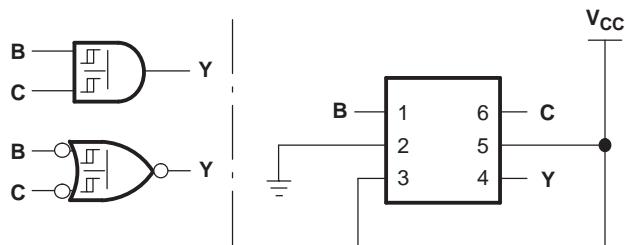
**Figure 5. 08/14+2: 2-Input AND Gate
2-Input NOR Gate With Both Inputs Inverted**
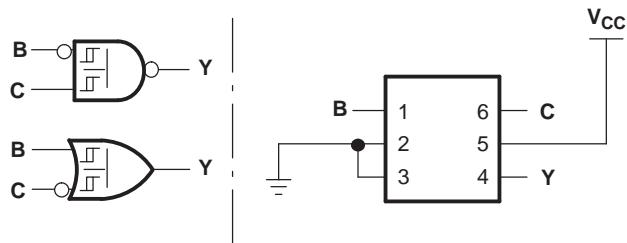
**Figure 6. 14+00/14+32: 2-Input NAND Gate With Inverted B Input
2-Input OR Gate With Inverted Input**

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Product Folder Link(s): *SN74AUP1T57*
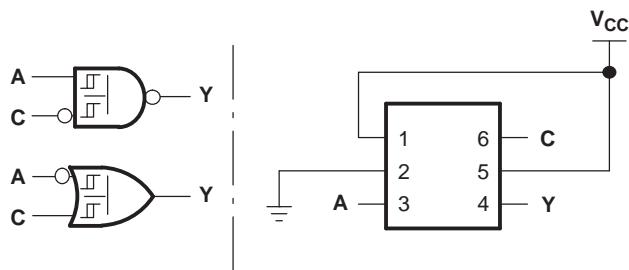
Figure 7. 14+00/14+32: 2-Input NAND Gate With Inverted C Input
2-Input OR Gate With Inverted Input
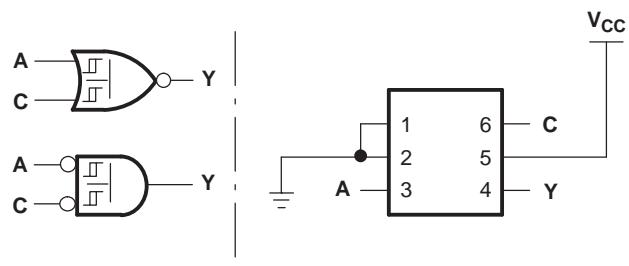
Figure 8. 02/14+08: 2-Input OR Gate
2-Input AND Gate With Both Inputs Inverted
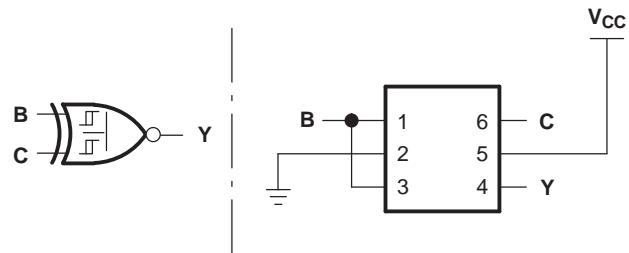
Figure 9. 86+04: 2-Input XNOR Gate

Figure 10. 04/14: Inverter

Product Folder Link(s): *SN74AUP1T57*
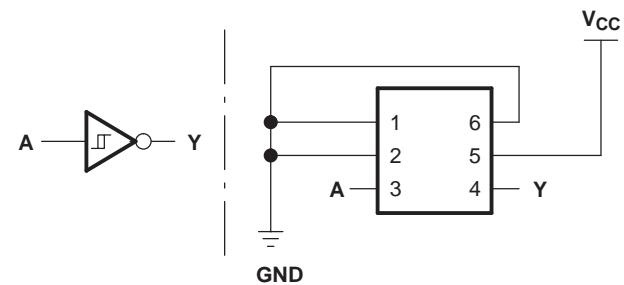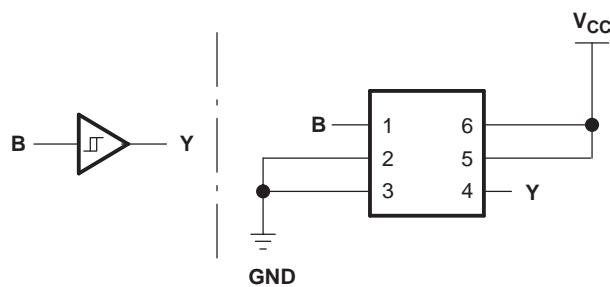
Figure 11. 17/34: Noninverted Buffer

Product Folder Link(s): *SN74AUP1T57*

ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

|			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[(2)]		−0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[(2)]		−0.5	4.6	V
V_O	Output voltage range in the high or low state[(2)]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[(3)]	DBV package		165	°C/W
		DCK package		259	
		DRY package		340	
		DSF package		300	
		YFP package		123	
		YZP package		123	
T_{stg}	Storage temperature range		−65	150	°C

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3)   The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		−3.1	mA
		V_{CC} = 3 V		−4	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		3.1	mA
		V_{CC} = 3 V		4	
T_A	Operating free-air temperature		−40	85	°C

(1)   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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TEXAS INSTRUMENTS

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{T+} Positive-going input threshold voltage			2.3 V to 2.7 V	0.6		1.1	0.6	1.1	V
			3 V to 3.6 V	0.75		1.16	0.75	1.19	
V_{T-} Negative-going input threshold voltage			2.3 V to 2.7 V	0.35		0.6	0.35	0.6	V
			3 V to 3.6 V	0.5		0.85	0.5	0.85	
ΔV_T Hysteresis (V_{T+} − V_{T-})			2.3 V to 2.7 V	0.23		0.6	0.1	0.6	V
			3 V to 3.6 V	0.25		0.56	0.15	0.56	
V_{OH}		I_{OH} = −20 μA	2.3 V to 3.6 V	V_{CC} − 0.1			V_{CC} − 0.1		V
		I_{OH} = −2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = −3.1 mA		1.9			1.85		
		I_{OH} = −2.7 mA	3 V	2.72			2.67		
		I_{OH} = −4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	2.3 V to 3.6 V			0.1		0.1	V
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	All inputs	V_I = 3.6 V or GND	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.1		0.5	μA
ΔI_{off}		V_I or V_O = 3.6 V	0 V to 0.2 V			0.2		0.5	μA
I_{CC}		V_I = 3.6 V or GND, I_O = 0	2.3 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		One input at 0.3 V or 1.1 V, Other inputs at 0 or V_{CC}, I_O = 0	2.3 V to 2.7 V					4	μA
		One input at 0.45 V or 1.2 V, Other inputs at 0 or V_{CC}, I_O = 0	3 V to 3.6 V					12	
C_i		V_I = V_{CC} or GND	3.3 V		1.5				pF
C_o		V_O = V_{CC} or GND	3.3 V		3				pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, V_I = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd} Power dissipation capacitance	f = 10 MHz	4	5	pF

Product Folder Link(s): *SN74AUP1T57*

PARAMETER MEASUREMENT INFORMATION
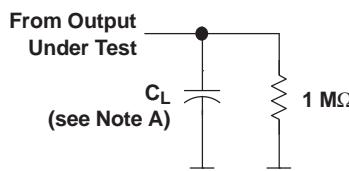
LOAD CIRCUIT

	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$
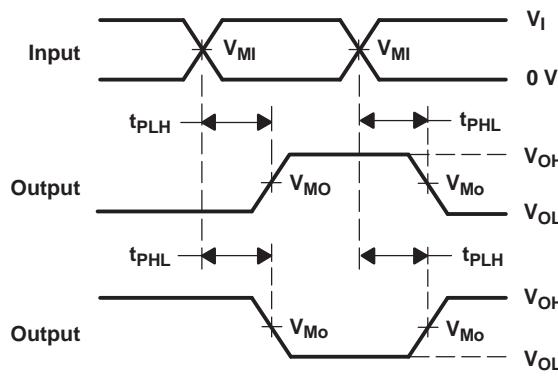
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 12. Load Circuit and Voltage Waveforms

![Texas Instruments Logo]

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T57DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HT3F ~ HT3R)	Samples
SN74AUP1T57DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HT3F ~ HT3R)	Samples
SN74AUP1T57DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TGF ~ TGR)	Samples
SN74AUP1T57DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TGF ~ TGR)	Samples
SN74AUP1T57DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(TGF ~ TGR)	Samples
SN74AUP1T57DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TG	Samples
SN74AUP1T57DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TG	Samples
SN74AUP1T57YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TG2 ~ TGN)	Samples
SN74AUP1T57YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TG7 ~ TGN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
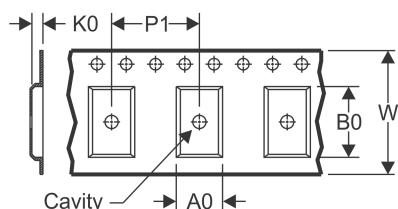
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
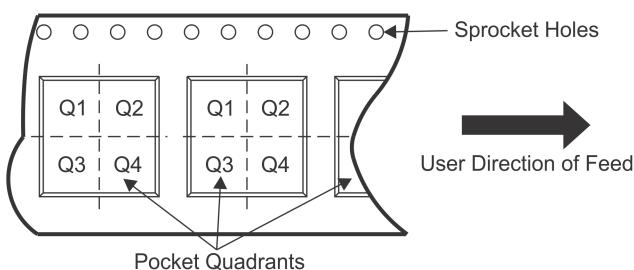
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T57DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T57DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T57DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T57DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T57DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1T57YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1T57YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T57DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T57DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T57DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T57DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T57DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1T57YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1T57YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PIN 1 INDEX AREA

1.05
0.95

1.05
0.95

A

B

0.4 MAX

C

SEATING PLANE

⌓ | 0.05Ⓜ | C

(0.11) TYP

0.05
0.00

SYMM
℄

SYMM
℄

3

4

2X
0.7

4X
0.35

1

6

(0.1)
PIN 1 ID

6X 0.45
   0.35

6X 0.22
   0.12

⊕ | 0.07Ⓜ | C | AⓈ | BⓈ
  | 0.05Ⓜ | C

4208186/F   10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern   Stencil Pattern

0.20   0.165

0.35   0.35

0.53   0.53

0.15 1.20   0.15 1.20

0.70   0.70
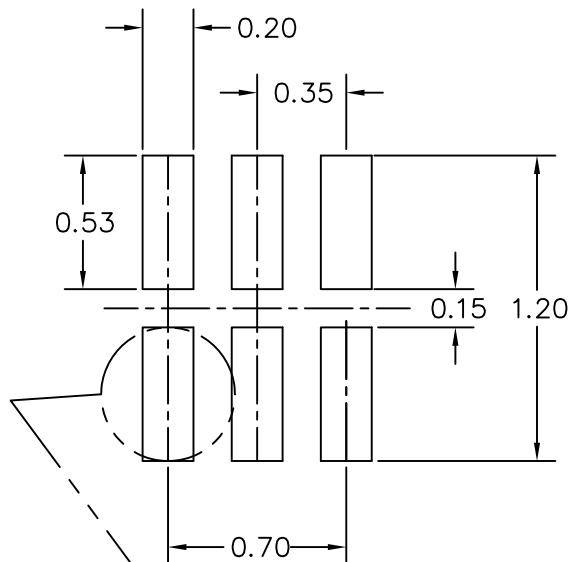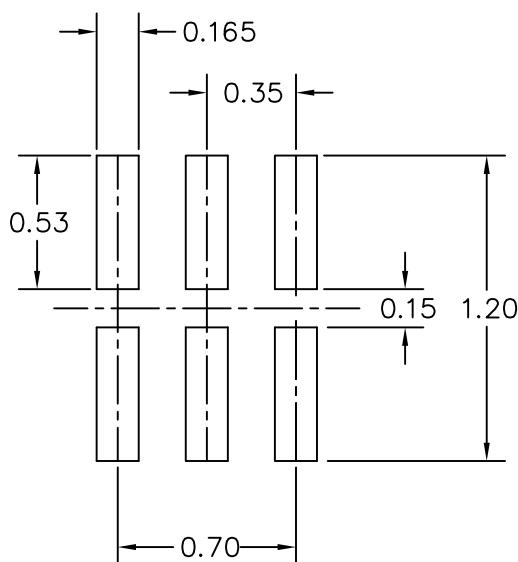
Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.53

0.20

4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
            If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
        E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
        H. Component placement force should be minimized to prevent excessive paste block deformation.

B ◄—— E ——► A

BALL A1
CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.15

BALL TYP

⌒ | 0.05 | C

0.5 TYP

C

SYMM
₵

B

1
TYP

0.5
TYP

A

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

1   2

6X ∅ 0.25
0.21

SYMM
₵

⊕ | 0.015Ⓢ | C | AⓈ | BⓈ

4219524/A   06/2014

NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

6X ($\emptyset$ 0.225)

(0.5) TYP

1
2

A

(0.5) TYP

B
SYMM
℄

C
SYMM
℄

LAND PATTERN EXAMPLE
SCALE:40X

($\emptyset$ 0.225)
METAL

0.05 MAX

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL
UNDER
MASK

($\emptyset$ 0.225)
SOLDER MASK
OPENING
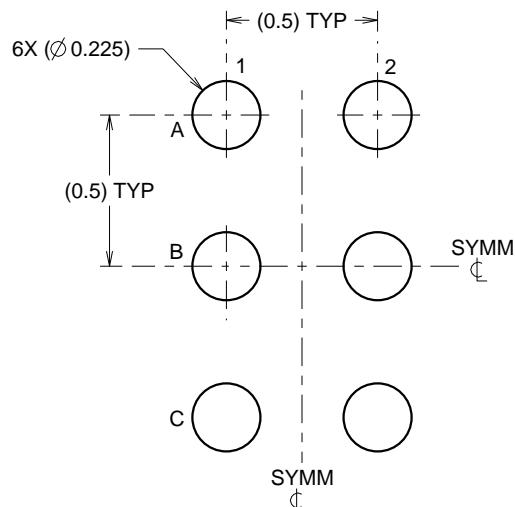
SOLDER MASK
DEFINED
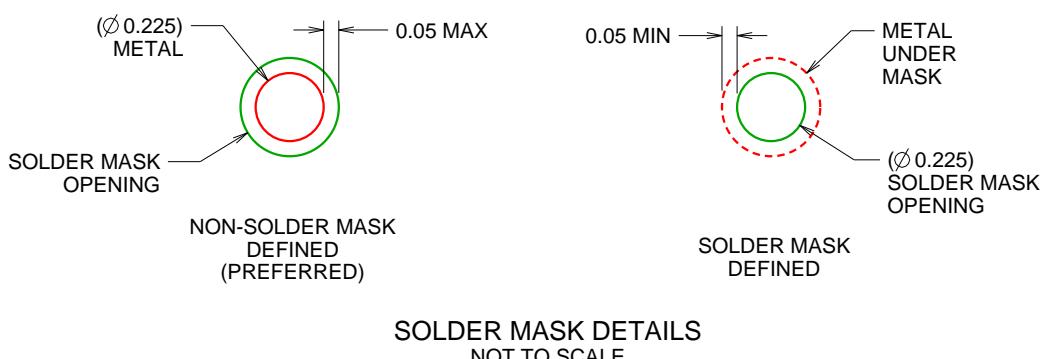
SOLDER MASK DETAILS
NOT TO SCALE

4219524/A   06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

(0.5) TYP

6X ($\square$0.25)

(R0.05) TYP

1

2

A

(0.5)
TYP

B

SYMM
$\mathbb{C}$

METAL
TYP

C

SYMM
$\mathbb{C}$
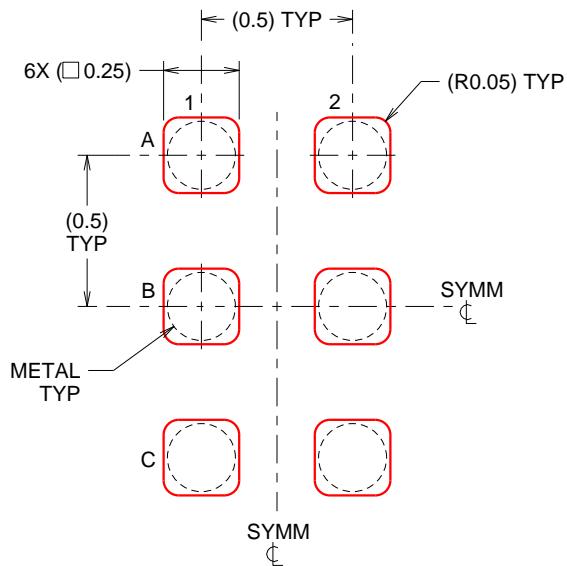
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A   06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

0.05 / 0.00

SEATING PLANE

⌒ 0.08 C

3X 0.6

SYMM ₵

(0.05) TYP

3

4

4X 0.5

SYMM ₵

2X 1

1

6

0.4 / 0.3

6X 0.25 / 0.15

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ C

PIN 1 ID (OPTIONAL)

5X 0.35 / 0.25

(0.127) TYP

4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
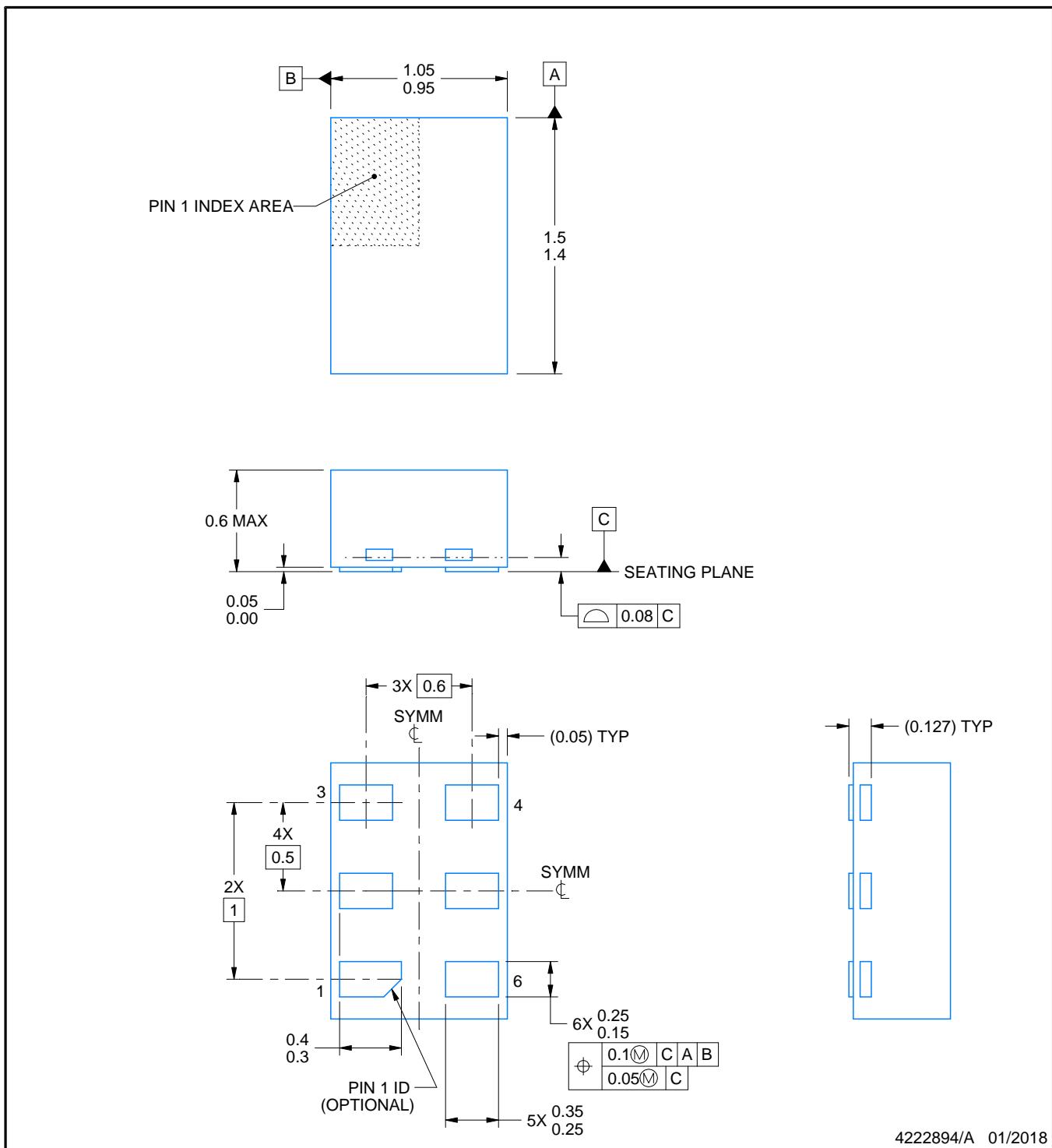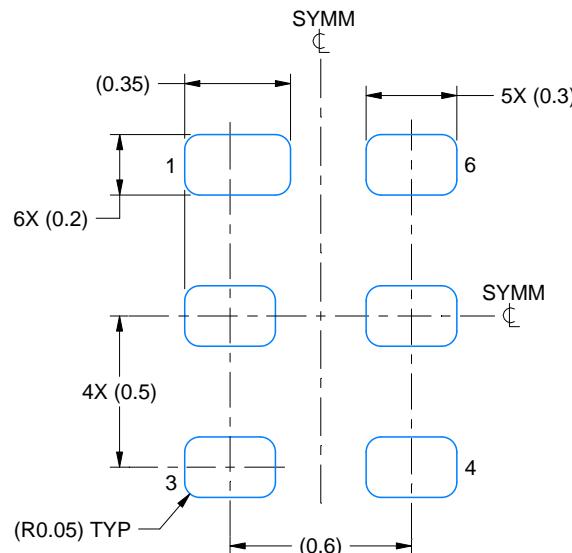
LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
(PREFERRED)
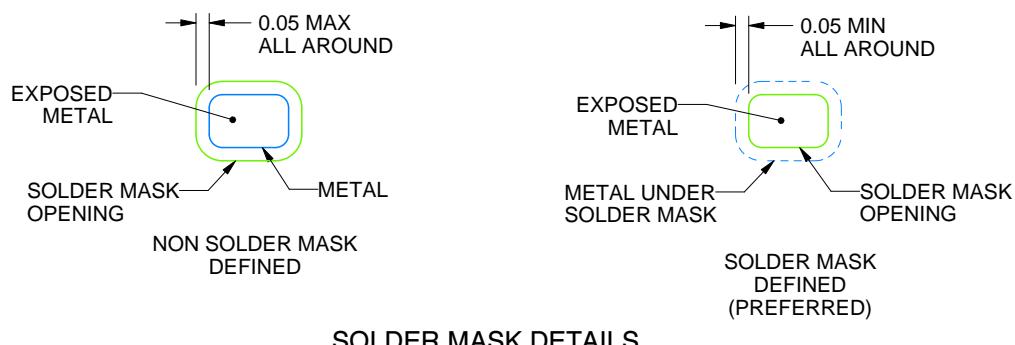
SOLDER MASK DETAILS

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.35)

5X (0.3)

6X (0.2)

SYMM

4X (0.5)

(R0.05) TYP

(0.6)
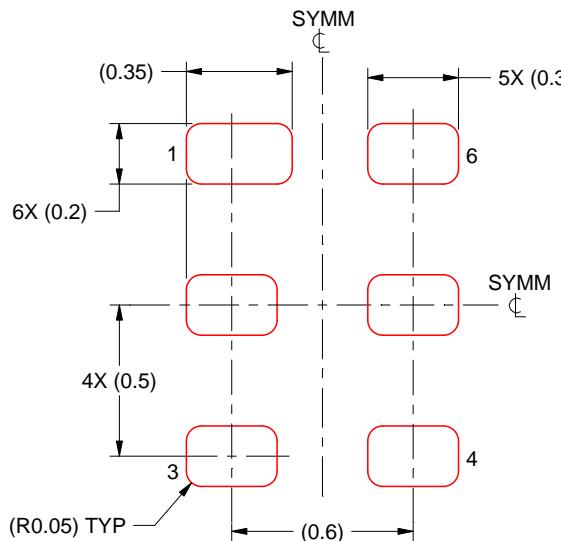
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBV (R−PDSO−G6)　　　　　　PLASTIC SMALL−OUTLINE PACKAGE

6　　　　　4

Pin 1
Index Area

DETAIL:
OPTIONAL ORIENTATION
MARKING

1　　　3

0,95

6X 0,50 / 0,25

⊕ 0,20 Ⓜ

6　　　4

1,75 / 1,45

3,00 / 2,60

Pin 1
Index Area
(See Detail)

1　　　3

3,05 / 2,75

0,22 / 0,08

Gage Plane

0°−8°

0,25

0,60 / 0,30

1,45 MAX

0,15 / 0,00

Seating Plane

⬠ 0,10
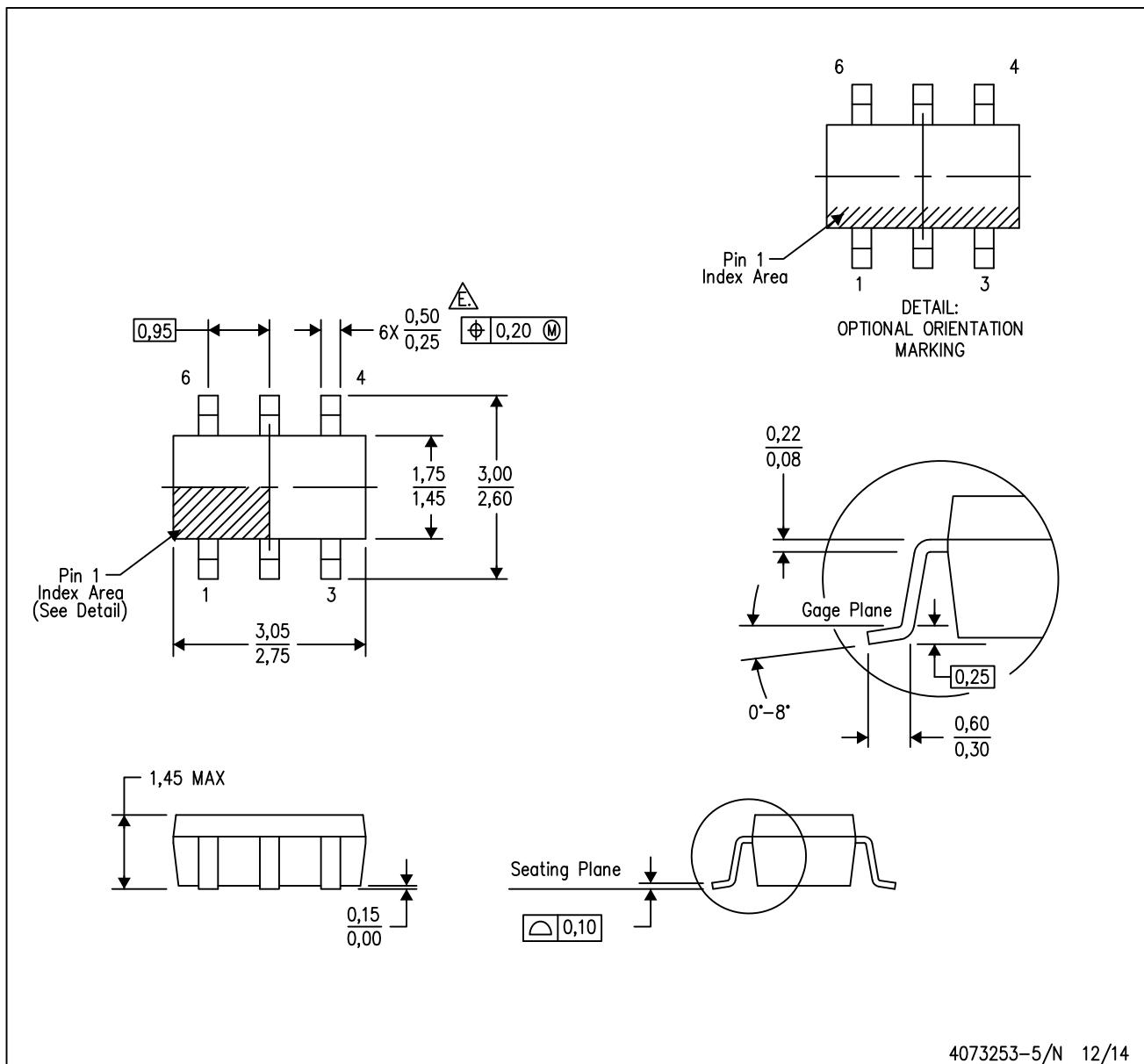
4073253−5/N   12/14

NOTES:　A. All linear dimensions are in millimeters.
　　　　　B. This drawing is subject to change without notice.
　　　　　C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
　　　　　D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
　　　　　E. Falls within JEDEC MO−178 Variation AB, except minimum lead width.
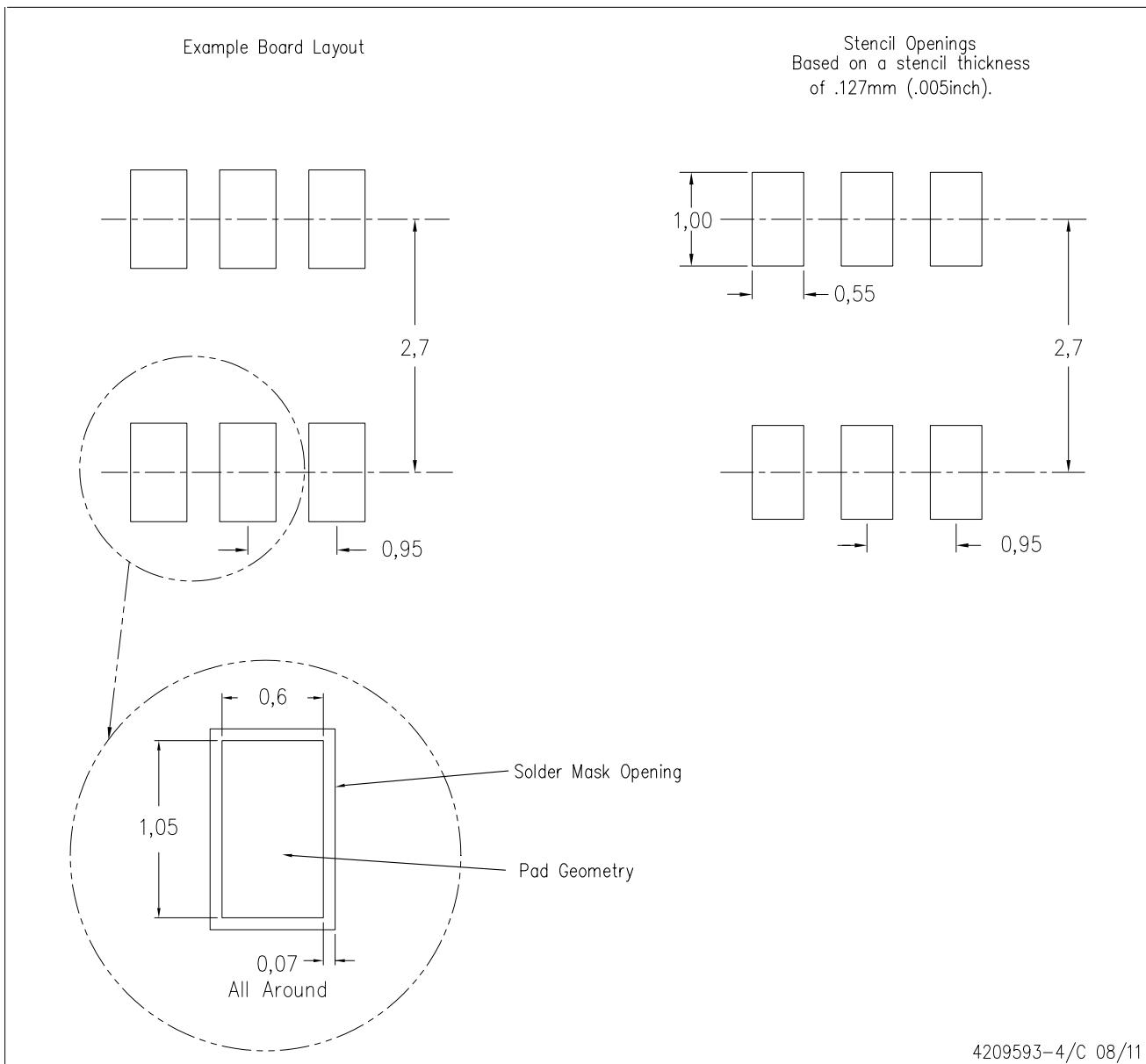
DBV (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−4/C 08/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DCK (R–PDSO–G6)   PLASTIC SMALL–OUTLINE PACKAGE

2,15
1,85

6   4

1,40
1,10

2,40
1,80

Pin 1
Index Area

1   3

0,65

6X 0,30
0,15

1,30

⊕ | 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°–8°

0,46
0,26

1,10
0,80

△ | 0,10

Seating Plane

0,10
0,00
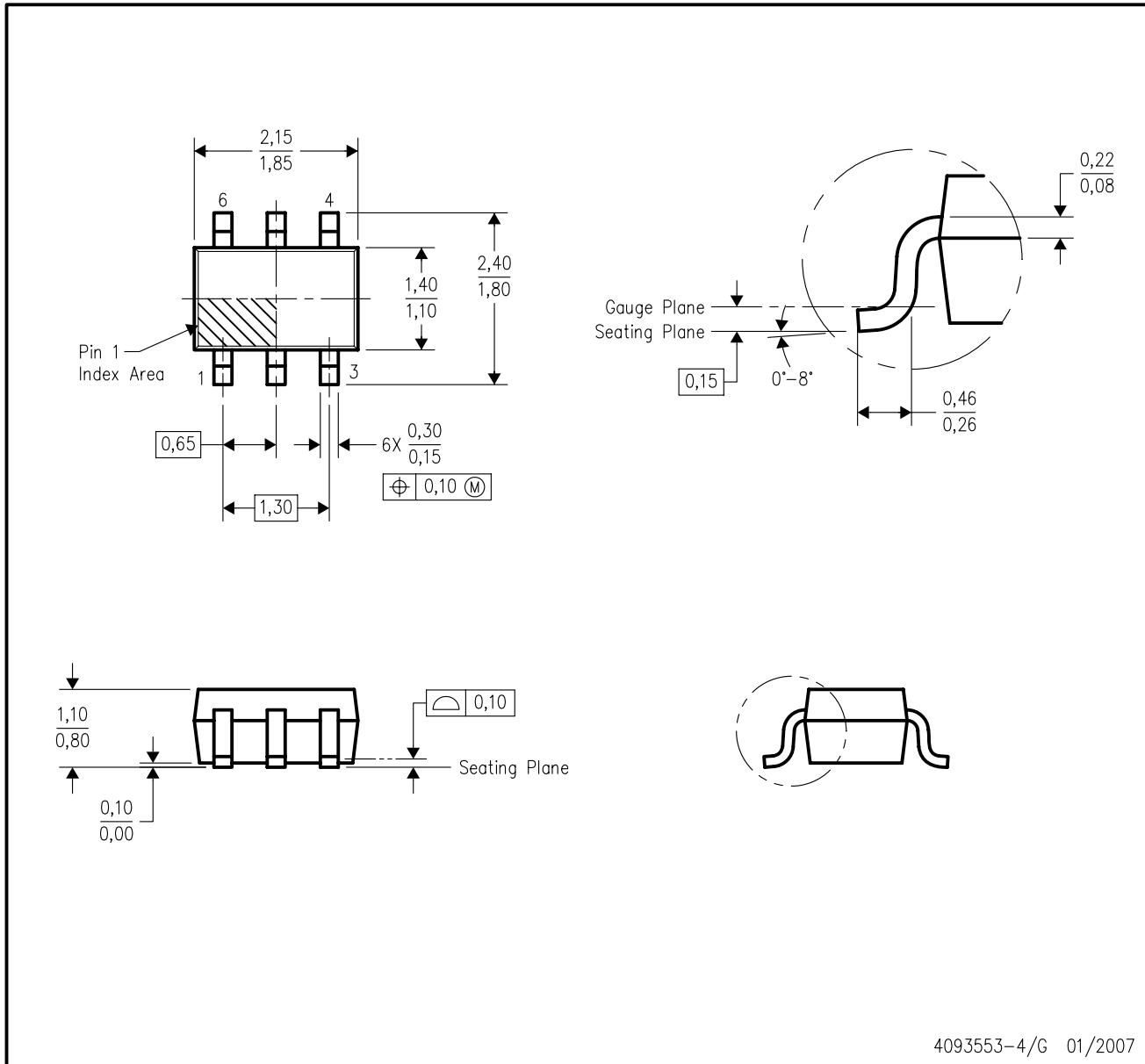
4093553–4/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO–203 variation AB.

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x1,30

4x0,65

2x1,30

4x0,65

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
        D. Publication IPC−7351 is recommended for alternate designs.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

B ◄——— E ———► A

BALL A1
CORNER

D

0.5 MAX

C

0.19
0.13

SEATING PLANE

BALL TYP

| ⌒ | 0.05 | C |

0.4
TYP

SYMM
₵

C

0.8
TYP

B

SYMM
₵

0.4 TYP

A

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

6X ⌀ 0.25
0.21

1   2

| ⌖ | 0.015 Ⓜ | C | A | B |

4223410/A   11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YFP0006
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY
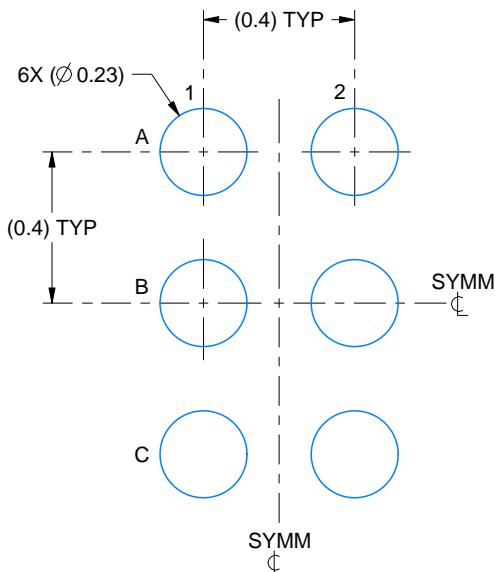
LAND PATTERN EXAMPLE
SCALE:50X
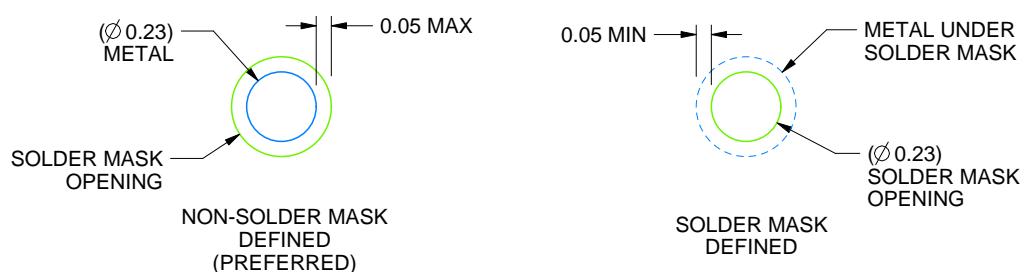
SOLDER MASK DETAILS
NOT TO SCALE

4223410/A   11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

TEXAS INSTRUMENTS
www.ti.com

6X (□0.25)

(0.4) TYP

(R0.05) TYP

1

2

A

(0.4) TYP

B

SYMM
℄

METAL
TYP

C

SYMM
℄
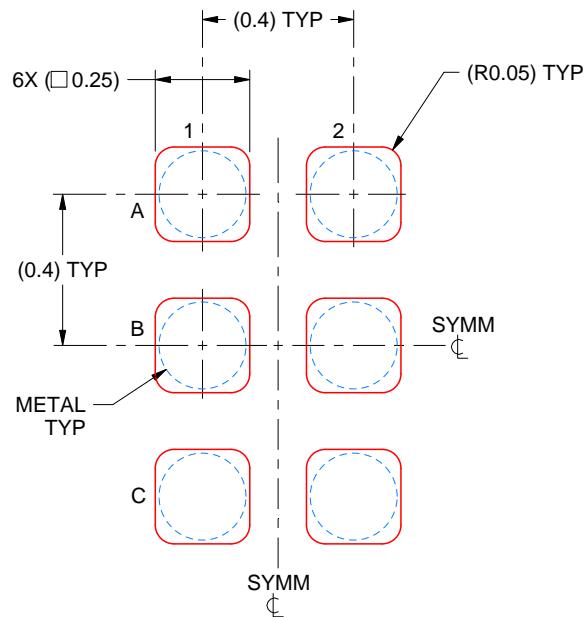
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A   11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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