

SM72445 Programmable Maximum Power Point Tracking Controller With Adjustable PWM Frequency

Check for Samples: [SM72445](#)

FEATURES

- Renewable Energy Grade
- 110kHz, 135kHz or 215kHz PWM Operating Frequency
- Panel Mode Pin for Optional Bypass Switch Control
- Programmable Maximum Power Point Tracking
- Photovoltaic Solar Panel Voltage and Current Diagnostic
- Single Inductor Four Switch Buck-Boost Converter Control
- I2C Interface for Communication
- Output Overvoltage Protection
- Over-Current Protection

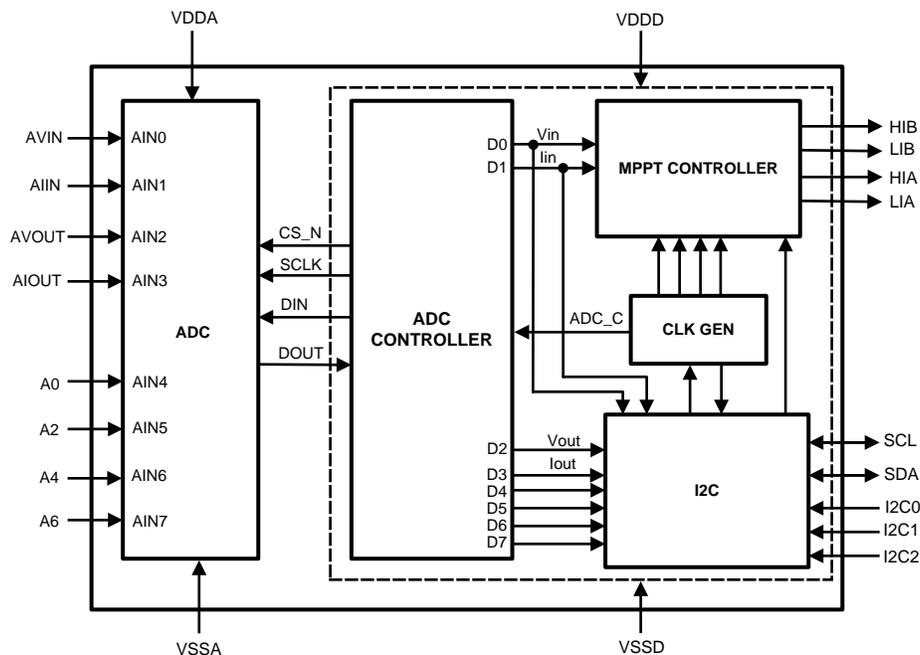
PACKAGE

- TSSOP-28

DESCRIPTION

The SM72445 is a programmable MPPT controller capable of controlling four PWM gate drive signals for a 4-switch buck-boost converter. The SM72445 also features a proprietary algorithm called Panel Mode (PM) which allows for the panel to be connected directly to the output of the power optimizer circuit when the input to output voltage ratio is close to 1. This provides an opportunity to optimize the efficiency of the power optimizer when the load is naturally matching the maximum power point of the panel. Along with the SM72295 (Photovoltaic Full Bridge Driver), it creates a solution for an MPPT configured DC-DC converter with efficiencies up to 99.5% (when operating with dedicated PM switches). Integrated into the chip is an 8-channel, 10 bit A/D converter used to sense input and output voltages and currents, as well as IC configuration. Externally programmable values include maximum output voltage and current as well as different settings for slew rate, soft-start and Panel Mode.

BLOCK DIAGRAM


Figure 1. Block Diagram


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

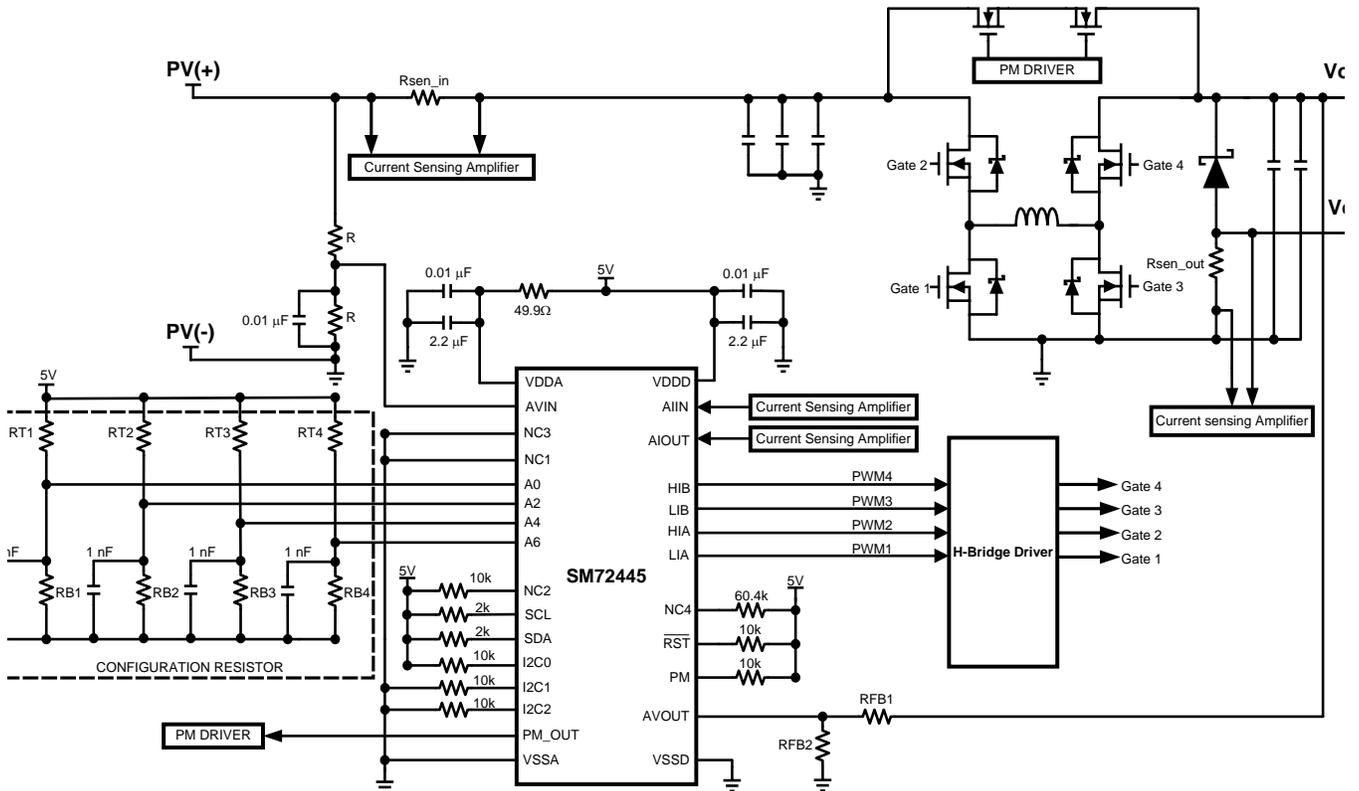


Figure 2. Typical Application Circuit

CONNECTION DIAGRAM

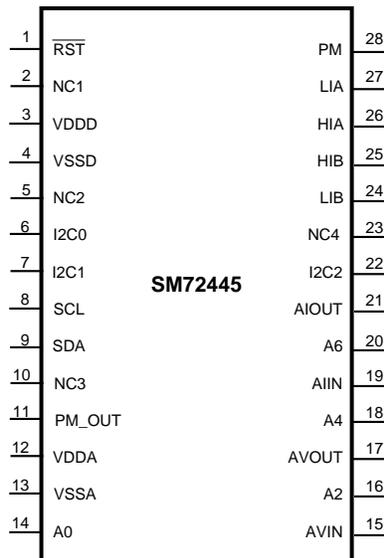


Figure 3. Top View - TSSOP-28

PIN DESCRIPTIONS

| Pin | Name | Description |
|-----|-------------------------|---|
| 1 | $\overline{\text{RST}}$ | Active low signal. External reset input signal to the digital circuit. |
| 2 | NC1 | Reserved for test only. This pin should be grounded. |
| 3 | VDDD | Digital supply voltage. This pin should be connected to a 5V supply, and bypassed to VSSD with a 0.1 μF monolithic ceramic capacitor. |
| 4 | VSSD | Digital ground. The ground return for the digital supply and signals. |
| 5 | NC2 | This pin should be pulled up to the 5V supply using a 10k resistor. |
| 6 | I2C0 | Addressing for I2C communication. |
| 7 | I2C1 | Addressing for I2C communication. |
| 8 | SCL | I2C clock. |
| 9 | SDA | I2C data. |
| 10 | NC3 | Reserved for test only. This pin should be grounded. |
| 11 | PM_OUT | When Panel Mode is active, this pin will output a 440 kHz square wave signal with amplitude of 5V. Otherwise, it stays low. |
| 12 | VDDA | Analog supply voltage. This voltage is also used as the reference voltage. This pin should be connected to a 5V supply, and bypassed to VSSA with a 1 μF and 0.1 μF monolithic ceramic capacitor. |
| 13 | VSSA | Analog ground. The ground return for the analog supply and signals. |
| 14 | A0 | A/D Input Channel 0. Connect a resistor divider to 5V supply to set the maximum output voltage. Please refer to the application section for more information on setting the resistor value. |
| 15 | AVIN | Input voltage sensing pin. |
| 16 | A2 | A/D Input Channel 2. Connect a resistor divider to a 5V supply to set the condition to enter and exit Panel Mode (PM). Refer to the Configurable Settings section. |
| 17 | AVOUT | Output voltage sensing pin. |
| 18 | A4 | A/D Input Channel 4. Connect a resistor divider to a 5V supply to set the maximum output current. Please refer to the application section for more information on setting the resistor value. |
| 19 | AIIN | Input current sensing pin. |
| 20 | A6 | A/D Input Channel 6. Connect a resistor divider to a 5V supply to set the output voltage slew rate and various PM configurations. Refer to the Configurable Settings section. |
| 21 | AIOUT | Output current sensing pin. |
| 22 | I2C2 | Addressing for I2C communication. |
| 23 | NC4 | This pin should be connected with a 60.4k pull-up resistor to 5V. |
| 24 | LIB | Low side boost PWM output. |
| 25 | HIB | High side boost PWM output. |
| 26 | HIA | High side buck PWM output. |
| 27 | LIA | Low side buck PWM output. |
| 28 | PM | Panel Mode Pin. Active low. Pulling this pin low will force the chip into Panel Mode. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

| | |
|--|----------------------------------|
| Analog Supply Voltage V_A (VDDA - VSSA) | -0.3 to 6.0V |
| Digital Supply Voltage V_D (VDDD - VSSD) | -0.3 to $V_A + 0.3V$ max 6.0V |
| Voltage on Any Pin to GND | -0.3 to $V_A + 0.3V$ |
| Input Current at Any Pin ⁽³⁾ | ± 10 mA |
| Package Input Current ⁽³⁾ | ± 20 mA |
| Storage Temperature Range | -65°C to +150°C |
| ESD Rating | See ⁽⁴⁾ |
| Human Body Model | 2 kV |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Min and Max limits are production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (4) The human body model is a 100 pF capacitor discharged through a 1.5 k Ω resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

| | |
|-----------------------|------------------|
| Operating Temperature | -40°C to 105°C |
| V_A Supply Voltage | +4.75V to +5.25V |
| V_D Supply Voltage | +4.75V to V_A |
| Digital Input Voltage | 0 to V_A |
| Analog Input Voltage | 0 to V_A |
| Junction Temperature | -40°C to 125°C |

ELECTRICAL CHARACTERISTICS

Specifications in standard typeface are for $T_J = 25^\circ\text{C}$, and those in boldface type apply over the full operating junction temperature range. ⁽¹⁾ Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_D = V_A = 5V$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|--|--|-------------------------------|------------|---------------------------|---------------|
| ANALOG INPUT CHARACTERISTICS | | | | | | |
| AV_{in} , Al_{in} AV_{out} , Al_{out} | Input Range | | - | 0 to V_A | - | V |
| I_{DCL} | DC Leakage Current | | - | - | ± 1 | μA |
| C_{INA} | Input Capacitance ⁽²⁾ | Track Mode | - | 33 | - | pF |
| | | Hold Mode | - | 3 | - | pF |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| V_{IL} | Input Low Voltage | | - | - | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.8 | - | - | V |
| C_{IND} | Digital Input Capacitance ⁽²⁾ | | - | 2 | - | pF |
| I_{IN} | Input Current | | - | ± 0.01 | ± 1 | μA |
| DIGITAL OUTPUT CHARACTERISTICS | | | | | | |
| V_{OH} | Output High Voltage | $I_{SOURCE} = 200 \mu\text{A}$ | $V_D - 0.5$ | - | - | V |
| V_{OL} | Output Low Voltage | $I_{SINK} = 200 \mu\text{A}$ to 1.0 mA | - | - | 0.4 | V |
| I_{OZH} , I_{OZL} | Hi-Impedance Output Leakage Current | | | | ± 1 | μA |
| C_{OUT} | Hi-Impedance Output Capacitance ⁽²⁾ | | | 2 | | pF |

- (1) Min and Max limits are production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (2) Not tested. Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard typeface are for $T_J = 25^\circ\text{C}$, and those in boldface type apply over the full operating junction temperature range.⁽¹⁾ Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_D=V_A=5\text{V}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|----------------|-------------|------|-------------|-------|
| POWER SUPPLY CHARACTERISTICS ($C_L = 10\text{ pF}$) | | | | | | |
| V_A, V_D | Analog and Digital Supply Voltages | $V_A \geq V_D$ | 4.75 | 5 | 5.25 | V |
| $I_A + I_D$ | Total Supply Current | | - | 11.5 | 16.5 | mA |
| PWM OUTPUT CHARACTERISTICS | | | | | | |
| A2 High Frequency Setting: | | | | | | |
| f_{PWM} | PWM switching frequency | | 170 | 215 | 250 | kHz |
| t_{DEAD} | Dead time (for Buck switch node and for Boost switch node) | | | 54 | | ns |
| A2 Medium Frequency Setting: | | | | | | |
| f_{PWM} | PWM switching frequency | | 105 | 135 | 155 | kHz |
| t_{DEAD} | Dead time | | | 87 | | ns |
| A2 Low Frequency Setting: | | | | | | |
| f_{PWM} | PWM switching frequency | | 85 | 110 | 125 | kHz |
| t_{DEAD} | Dead time | | | 106 | | ns |

TYPICAL PERFORMANCE CHARACTERISTICS

Typical performance curves reflect the performance of the SM72445 as designed into the SM3320–1A1 reference design, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $T_J = 25^\circ\text{C}$.

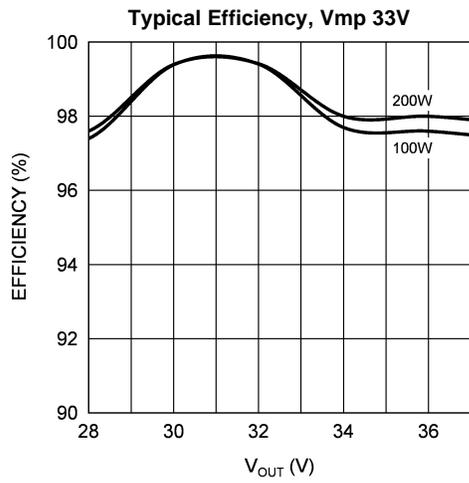


Figure 4.

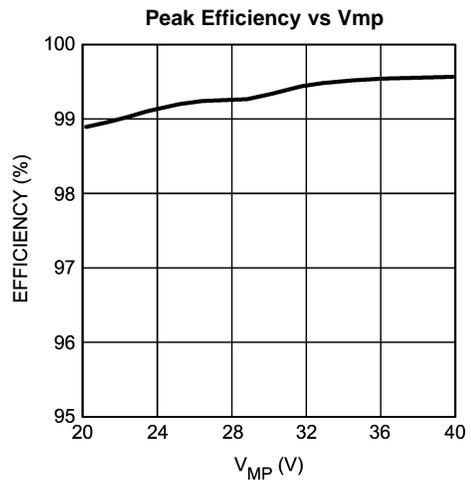


Figure 5.

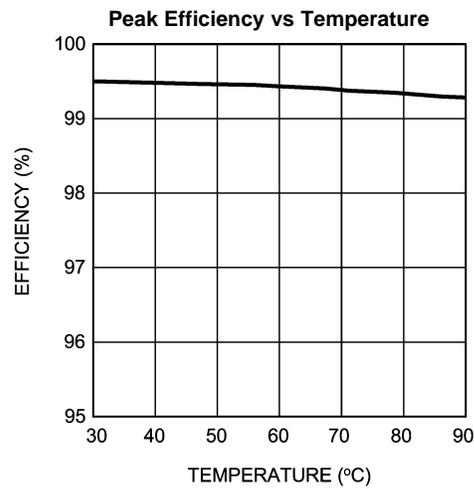


Figure 6.

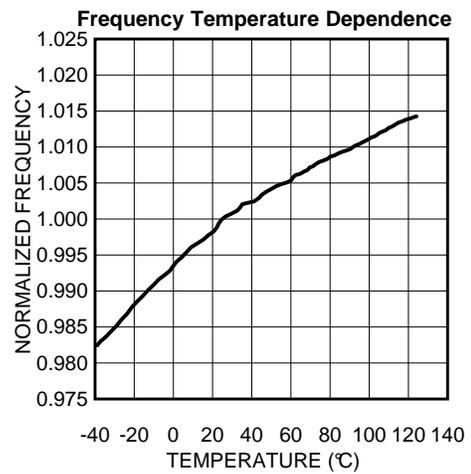


Figure 7.

OPERATION DESCRIPTION

OVERVIEW

The SM72445 is a programmable MPPT controller capable of outputting four PWM gate drive signals for a 4 switch buck-boost converter with an independent Panel Mode. The typical application circuit is shown in [Figure 2](#). The SM72445 does not require a dedicated switch to implement Panel Mode. The four buck-boost switches can be controlled to implement PM. A dedicated switch may be used for higher efficiency. Setting the voltage on pin A2 selects between the options.

The SM72445 uses an advanced digital controller to generate its PWM signals. A maximum power point tracking (MPPT) algorithm monitors the input current and voltage and controls the PWM duty cycle to maximize energy harvested from the photovoltaic module. MPPT performance is very fast. Convergence to the maximum power point of the module typically occurs within 0.01s. This enables the controller to maintain optimum performance under fast-changing irradiance conditions.

Transitions between buck, boost, and Panel Mode are smoothed. Output voltage and current limiting functionality are integrated into the digital control logic. The controller is capable of handling both shorted and no-load conditions and will recover smoothly from both conditions.

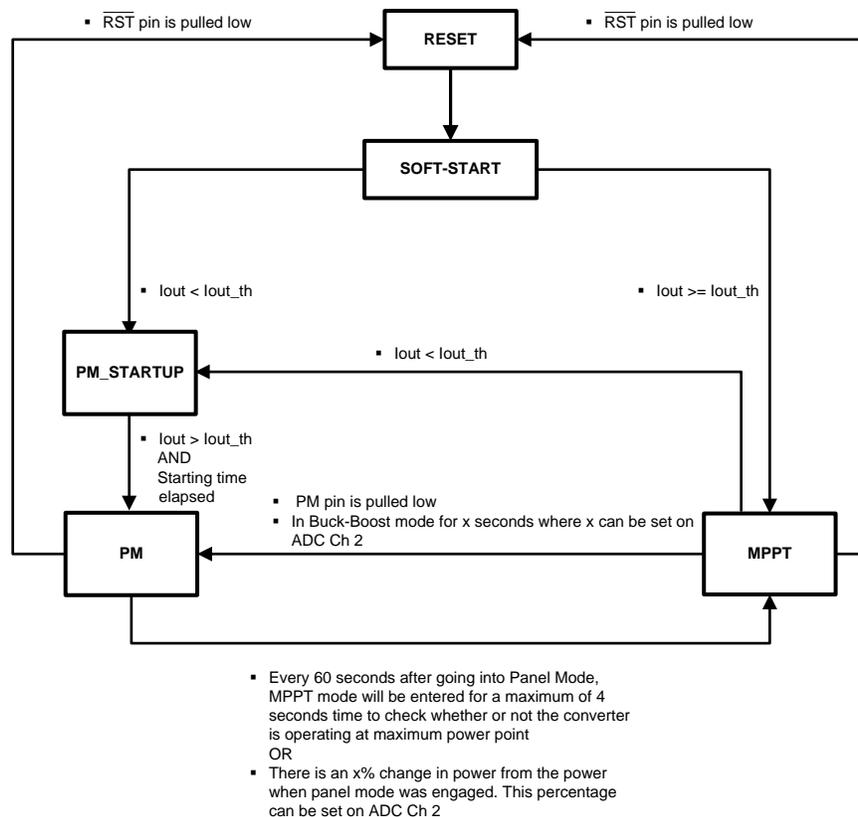


Figure 8. High Level State Diagram for Startup

STARTUP

SM72445 has a soft start feature that will ramp its output voltage for a time of 250ms if the bridge is configured to run at 215kHz and up to 500ms if the bridge is configured for 110kHz.

If no output current is detected during soft-start time, the device will then enter Panel Mode for 60 seconds. A counter will start once the minimum output current threshold is met (set by ADC input channel 4, pin A4). During these 60 seconds, any variation on the output power will not cause the chip to enter MPPT mode. Once 60 seconds have elapsed, the unit will enter operational PM mode and the pre-determined power level variation at the output will engage the chip in MPPT mode.

If the output current is greater than the current threshold set at A/D Channel 6 (A6) during soft-start, the chip will then engage in MPPT mode and will not be subject to the start-up delay.

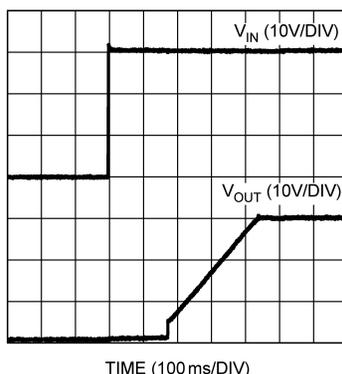


Figure 9. Startup Sequence

MAXIMUM OUTPUT VOLTAGE

The maximum output voltage on the SM72445 is set by the resistor divider ratio on pin A0. (Please refer to [Figure 2](#) Typical Application Circuit).

The value of the voltage on pin A0 is sampled and stored by the ADC of the SM72445 at start-up and after reset events. While voltage on pin AVOUT is above the voltage set at pin A0, the duty cycle of the converter will be reduced every MPPT cycle (1ms-2ms depending on the set switching frequency). This is true when the converter is running in MPPT state or during Soft-Start. When the unit is in Panel Mode (PM) or in Startup Panel Mode (PM_Startup) there is no control on the output voltage and the device will not react to the presence of a voltage on AVOUT higher than the A0 setpoint. See [Figure 8](#) for more details on the different states of operation.

This means that the voltage limit setting cannot be used to ensure overall maximum output voltage for the system: there will be times during Panel Mode operation and Stand-by mode operation when the output will increase above the programmed output voltage if the input (solar panel) gets over that voltage limit. Therefore, the maximum output voltage threshold set by programming A0 is only valid if its value is higher than the maximum input voltage (solar panel in open circuit at coldest operating point). If over-voltage protection needs to be implemented, it must be done using external components. For example, a voltage comparator with its output connected to the reset pin of the SM72445 is one possible implementation.

The maximum output voltage is always enforced during MPPT operation of the IC.

The following equation sets the maximum output voltage:

$$V_{OUT_MAX} = 5 \times \frac{RB1}{RT1 + RB1} \times \frac{(RFB1 + RFB2)}{RFB2}$$

Where RT1 and RB1 are the resistor divider on the ADC pin A0 and RFB1 and RFB2 are the output voltage sense resistors. A typical value for RFB2 is about 2 kΩ

CURRENT LIMIT SETTING

Maximum output current can be set by changing the resistor divider on A4 (pin 18). Refer to [Figure 2](#). Overcurrent at the output is detected when the voltage on AIOU (pin 21) equals the voltage on A4 (pin 18). The voltage on A4 can be set by a resistor divider connected to 5V whereas the voltage on AIOU can be set by a current sense amplifier.

AVIN PIN

AVIN is an A/D input to sense the input voltage of the SM72445. A resistor divider can be used to scale max voltage to about 4V, which is 80% of the full scale of the A/D input.

CONFIGURABLE SETTINGS

A/D pins A0, A2, A4, and A6 are used to configure the behavior of the SM72445 by adjusting the voltage applied to them through resistor dividers as shown in [Figure 2](#), where RT1 to RT4 should be in the range of 20 kΩ.

The voltages of the configuration pins are read and the operating mode is then set at start-up and after each reset of the device.

Three different frequencies for the PWM operation of the H-bridge as well as two different implementations of the Panel Mode switch can be set on the ADC input channel 2 (pin A2). The table below lists the different conditions that a user can select on pin A2. Each frequency has a different associated dead time for the operation of the synchronous switches. When dedicated PM switch modes are used, the unit will stop switching the converter upon entering PM mode and the PM_OUT pin will switch at a high frequency to provide activation of a dedicated Panel Mode switch. When the H-bridge modes are used, the unit will keep the H-bridge switching at half the operating frequency (to reduce switching losses) and with a total input to output ratio of 1. The dead times are unchanged during this phase.

Table 1. Programmable Settings on Pin A2

| A2 | PWM Frequency setting | Panel Mode Operation |
|--------|-----------------------|--------------------------------|
| 4.69 V | HIGH | Uses dedicated PM switch |
| 4.06 V | HIGH | Uses dedicated PM switch |
| 3.44 V | LOW | Uses H-bridge for PM operation |
| 2.81 V | MED. | Uses H-bridge for PM operation |
| 2.19 V | HIGH | Uses H-bridge for PM operation |
| 1.56 V | LOW | Uses dedicated PM switch |
| 0.94 V | MED. | Uses dedicated PM switch |
| 0.31 V | HIGH | Uses dedicated PM switch |

The user can also select the output voltage slew rate, minimum current threshold and duration of Panel Mode after the soft-start period has finished, by changing the voltage level on pin A6 which is the input of ADC channel 6. The slew rate limiter takes control of the duty cycle if the output voltage rises faster than the programmed limit while the unit is running in Boost mode (output voltage higher than input voltage). The device will control the duty cycle so that the output voltage stays within the allowed slew rate. The slew rate is never limited in Buck mode (output voltage lower than input voltage).

Table 2. Programmable Settings on Pin A6

| A6 | Output Voltage Slew Rate Limit | Starting Panel Mode Time | MPPT Exit Threshold (on AIOU or AIIN) | MPPT Start Threshold (on AIOU) | Starting boost ratio |
|--------|--------------------------------|--------------------------|---------------------------------------|--------------------------------|----------------------|
| 4.69 V | 10V/1.2s | Not applicable | 0 V | 0 V | N/A |
| 4.06 V | 10V/1.2s | 60s | 0.006xVDDA | 0.010xVDDA | 1:1 |
| 3.44 V | 10V/1.2s | 0s | 0.023xVDDA | 0.039xVDDA | 1:1 |
| 2.81 V | 10V/1.2s | 120s | 0.023xVDDA | 0.039xVDDA | 1:1 |
| 2.19 V | 10V/1.2s | Not applicable | 0.006xVDDA | 0.010xVDDA | 1:1.2 |
| 1.56 V | 10V/1.2s | 60s | 0.023xVDDA | 0.039xVDDA | 1:1 |
| 0.94 V | 10V/0.6s | 60s | 0.023xVDDA | 0.039xVDDA | 1:1 |
| 0.31 V | No slew rate limit | 60s | 0.023xVDDA | 0.039xVDDA | 1:1 |

PARAMETER DEFINITIONS

Output Voltage Slew Rate Limit Settling Time: Time constant of the internal filter used to limit output voltage change. At the fast slew rate, the output voltage will be held for 60 ms for every 1V increase, whereas in the slow slew rate, the output voltage will be held for 120ms for every 1V increase. (See [Figure 10](#)).

Starting PM Time: After initial power-up or reset, the output soft-starts and then enters Panel Mode for this amount of time.

MPPT Exit Threshold and MPPT Start Threshold: These are the hysteretic thresholds for `lout_th` read on pin A1OUT. The values are expressed as a fraction of the voltage at pin VDDA. A1OUT is the output current sensing pin and should be connected to the output of a current sense amplifier. For example, with a current sense amplification of 0.5V/A provided by an external current sense resistor and amplifier and assuming VDDA=5V and A6=0.94V, the output current threshold to bring the device out of stand-by mode will be 0.39A.

Starting Boost Ratio: This is the end-point of the soft-start voltage ramp expressed as a ratio of VOUT/VIN. 1:1 ratio means it stops when $V_{out} = V_{in}$, whereas a 1:1.2 ratio means it stops when $V_{out} = 1.2 \times V_{in}$.

DEAD-TIME

The dead time of the switches to avoid cross conduction of the buck FETs and boost FETs depends on the switching frequency set: it is equal to $(3/256) \times 1/f_{SWITCH}$. When the IC is programmed for 215 kHz operation, the dead time between H1A and LOA and between H1B and LOB will be 55ns.

PANEL MODE PIN (PM)

The SM72445 can be forced into Panel Mode by pulling the PM pin low. One sample application is to connect this pin to the output of an external temperature sensor; therefore whenever an over-temperature condition is detected the chip will enter Panel Mode.

Once Panel Mode is enabled, either when the unit is running in MPPT mode with a 1:1 conversion ratio or when PM is pulled low, the PM_OUT pin will output a 440 kHz square wave signal. Using a gate driver and transformer, this square wave signal can then be used to drive a Panel Mode FET as shown in Figure 11.

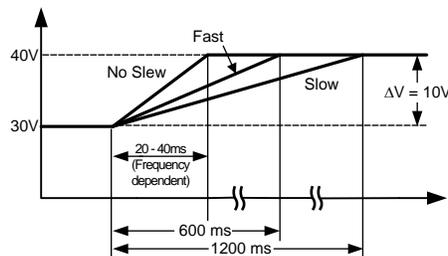


Figure 10. Slew Rate Limitation Circuit

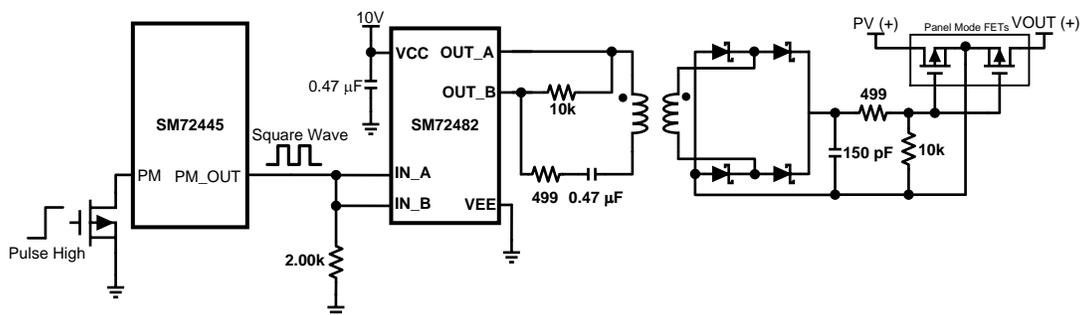


Figure 11. Sample Application for Panel Mode Operation

RESET PIN

When the reset pin is pulled low, the chip will cease its normal operation and turn-off all of its PWM outputs including the output of PM_OUT pin. Below is an oscilloscope capture of a forced reset condition.

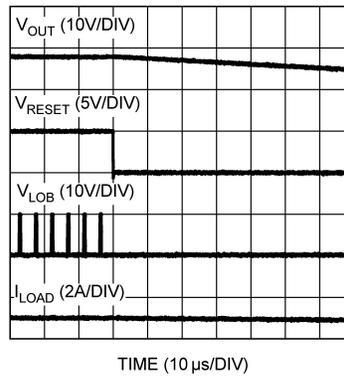


Figure 12. Forced Reset Condition

As seen in Figure 12, the initial value for output voltage and load current are 28V and 1A respectively. After the reset pin is grounded both the output voltage and load current decreases immediately. MOSFET switching on the buck-boost converter also stops immediately. VLOB indicates the low side boost output from the SM72295.

ANALOG INPUT

An equivalent circuit for one of the ADC input channels is shown in Figure 13. Diode D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0V to V_A . Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 13 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch; it is typically 500Ω. Capacitor C2 is the ADC sampling capacitor; it is typically 30 pF. The ADC will deliver best performance when driven by a low-impedance source (less than 100Ω). This is especially important when sampling dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonic and noise in the input. These filters are often referred to as anti-aliasing filters.

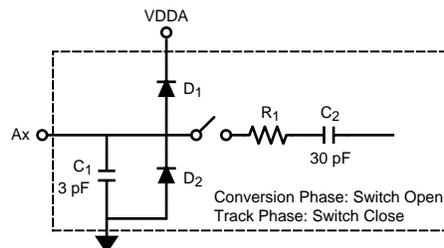


Figure 13. Equivalent Input Circuit

DIGITAL INPUTS and OUTPUTS

The digital input signals have an operating range of 0V to V_A , where $V_A = V_{DDA} - V_{SSA}$. They are not prone to latch-up and may be asserted before the digital supply V_D , where $V_D = V_{DDD} - V_{SSD}$, without any risk. The digital output signals operating range is controlled by V_D . The output high voltage is $V_D - 0.5V$ (min) while the output low voltage is 0.4V (max).

SCL and SDA

SCL is an input, and SDA is bidirectional with an open-drain output. SCL and SDA do not have internal pull-ups. A “high” level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. The choice of resistor value depends on many system factors such as load capacitance and trace length. A typical value of pull-up resistor for SM72445 ranges from 2 kΩ to 10 kΩ. For more information, refer to the I2C Bus specification for selecting the pull-up resistor value. The SCL and SDA outputs can operate while being pulled up to 5V and 3.3V.

I2C CONFIGURATION REGISTERS

The operation of the SM72445 can be configured through its I2C interface. Complete register settings for I2C lines are shown below.

| reg0 Register Description | | | | |
|---------------------------|-------|-------------|-----|--|
| Bits | Field | Reset Value | R/W | Bit Field Description |
| 55:40 | RSVD | 16'h0 | R | Reserved for future use. |
| 39:30 | ADC6 | 10'h0 | R | Analog Channel 6 (slew rate detection time constant, see adc config worksheet) |
| 29:20 | ADC4 | 10'h0 | R | Analog Channel 4 (iout_max: maximum allowed output current) |
| 19:10 | ADC2 | 10'h0 | R | Analog Channel 2 (operating mode, see adc_config worksheet) |
| 9:0 | ADC0 | 10'h0 | R | Analog Channel 0 (vout_max: maximum allowed output voltage) |

| reg1 Register Description | | | | |
|---------------------------|---------|-------------|-----|--|
| Bits | Field | Reset Value | R/W | Bit Field Description |
| 55:41 | RSVD | 15'h0 | R | Reserved for future use. |
| 40 | mppt_ok | 1'h0 | R | Internal mppt_start signal (test only) |
| 39:30 | Vout | 10'h0 | R | Voltage out |
| 29:20 | Iout | 10'h0 | R | Current out |
| 19:10 | Vin | 10'h0 | R | Voltage in |
| 9:0 | Iin | 10'h0 | R | Current in |

| reg3 Register Description | | | | |
|---------------------------|---------------------|-------------|-----|--|
| Bits | Field | Reset Value | R/W | Bit Field Description |
| 55:47 | RSVD | 9'd0 | R/W | Reserved |
| 46 | override_adcprog | 1'b0 | R/W | When set to 1'b1, the below override registers used instead of ADC |
| 45 | RSVD | 1'b0 | R/W | Reserved |
| 44:43 | RSVD | 2'd1 | R/W | Reserved |
| 42:40 | A2_override | 3'd0 | R/W | Register override alternative for the three MSBs of ADC2 (bits [9–7]) when reg3[46] is set. This allows frequency and panel mode configuration to be set through I2C |
| 39:30 | iout_max | 10'd1023 | R/W | Register override alternative when reg3[46] is set for maximum current threshold instead of ADC ch4 |
| 29:20 | vout_max | 10'd1023 | R/W | Register override alternative when reg3[46] is set for maximum voltage threshold instead of ADC ch0 |
| 19:17 | tdoff | 3'h3 | R/W | Dead time Off Time |
| 16:14 | tdon | 3'h3 | R/W | Dead time On time |
| 13:5 | dc_open | 9'hFF | R/W | Open loop duty cycle (test only) |
| 4 | pass_through_sel | 1'b0 | R/W | Overrides PM pin 28 and use reg3[3] |
| 3 | pass_through_manual | 1'b0 | R/W | Control Panel Mode when pass_through_sel bit is 1'b1 |
| 2 | bb_reset | 1'b0 | R/W | Soft reset |
| 1 | clk_oe_manual | 1'b0 | R/W | Enable the PLL clock to appear on pin 5 |
| 0 | Open Loop operation | 1'b0 | R/W | Open Loop operation (MPPT disabled, receives duty cycle command from reg 3b13:5); set to 1 and then assert & deassert bb_reset to put the device in openloop (test only) |

| reg4 Register Description | | | | |
|---------------------------|-------------|-------------|-----|-----------------------|
| Bits | Field | Reset Value | R/W | Bit Field Description |
| 55:32 | RSVD | 24'd0 | R/W | Reserved |
| 31:24 | Vout offset | 8'h0 | R/W | Voltage out offset |
| 23:16 | Iout offset | 8'h0 | R/W | Current out offset |
| 15:8 | Vin offset | 8'h0 | R/W | Voltage in offset |
| 7:0 | Iin offset | 8'h0 | R/W | Current in offset |

| reg5 Register Description | | | | |
|---------------------------|------------|-------------|-----|--------------------------------------|
| Bits | Field | Reset Value | R/W | Bit Field Description |
| 55:40 | RSVD | 15'd0 | R/W | Reserved |
| 39:30 | iin_hi_th | 10'd40 | R/W | Current in high threshold for start |
| 29:20 | iin_lo_th | 10'd24 | R/W | Current in low threshold for start |
| 19:10 | iout_hi_th | 10'd40 | R/W | Current out high threshold for start |
| 9:0 | iout_lo_th | 10'd24 | R/W | Current out low threshold for start |

The open loop operation allows the user to set a fixed operating duty cycle (buck or boost) on the converter. The unit will not sense current or voltage in this mode and will perform an internal reset when exiting open loop mode.

The `bb_reset` bit performs a limited reset of the IC. While this bit is set high, the unit will not output any driving signal and will not sense any input. When this bit is transitioned back to zero, the unit will go through its initialization phase according to the programming mode set and possible I2C overrides. The IC will NOT perform a sample of the A0–A6 input when the `bb_reset` bit is cleared.

To change the PWM frequency options the first time after power up, the following programming sequence must be used :

- set `bb_reset` bit (reg3[2]), set over-ride bit (reg3[46]), set to the desired PWM code (reg3[42:40])
- reset `bb_reset` bit, keep over-ride bit, keep the desired PWM code

To change PWM options subsequent to an earlier programming :

- set `bb_reset` bit, reset over-ride bit, set to the desired PWM code
- reset `bb_reset` bit, reset over-ride bit, keep the desired PWM code
- set `bb_reset` bit, set over-ride bit, keep the desired PWM code
- reset `bb_reset` bit, keep over-ride bit, keep the desired PWM code

The switching frequency will be returned to the default external resistor setting after each hard reset of the IC.

The “`tdoff`” and “`tdon`” (REG3[14:19]) parameters allow modification of the dead time. the dead time for the turning on of the synchronous rectifier (affecting buck and boost mode) will be set by $(td_on/256)*(1/f_switch)$. The default parameter for `td_on` is 3.

The dead time for the turning on of the main switch after the synchronous rectifier as turned off (affecting buck and boost mode) will be set by $(td_off/256)*(1/f_switch)$. The default parameter for `td_off` is 3. The dead time parameters are returned to their default value after each hard reset of the IC.

The offsets are 8 bit signed numbers which are added or subtracted to the results of the A/D converter and affect the sensed values displayed in Register 0 as well as the thresholds.

Using the I2C port, the user will be able to control the duty cycle of the PWM signal. Input and output voltage and current offsets can also be controlled using I2C on register 4. Control registers are available for additional flexibility.

The thresholds `iin_hi_th`, `iin_lo_th`, `iout_hi_th`, `iout_lo_th`, in reg5 are compared to the values read in by the ADC on the AIIN and AIOU pins. Scaling is set by the scaling of the analog signal fed into AIIN and AIOU. These 10–bit values determine the entry and exit conditions for MPPT. The startup high thresholds set the voltages at pin AIIN and AIOU above which the unit will begin transition from PM_Startup state to MPPT state. The low thresholds set the voltage below which the unit will transition back to PM_Startup (stand-by). The initial thresholds are a function of the value programmed in A6. As determined by [Table 2](#), if A6 was between 0 and 1.56V at start-up, the thresholds will be $0.023*VDDA$ and $0.039*VDDA$.

To run the system in Open Loop configuration, the Soft Reset bit must be set then cleared. The ADC channels are inactive when the device is used in Open Loop configuration.

COMMUNICATING WITH THE SM72445

The SCL line is an input, the SDA line is bidirectional, and the device address can be set by the I2C0, I2C1 and I2C2 pins. Three device address pins allow connection of up to 7 SM72445s to the same I2C master. A pull-up resistor (10kΩ) to a 5V supply is used to set a bit 1 on the device address. Device addressing for slaves are as follows:

| I2C0 | I2C1 | I2C2 | Hex |
|------|------|------|-----|
| 0 | 0 | 1 | 0x1 |
| 0 | 1 | 0 | 0x2 |
| 0 | 1 | 1 | 0x3 |
| 1 | 0 | 0 | 0x4 |
| 1 | 0 | 1 | 0x5 |
| 1 | 1 | 0 | 0x6 |
| 1 | 1 | 1 | 0x7 |

The data registers in the SM72445 are selected by the Command Register. The Command Register is offset from base address 0xE0. Each data register in the SM72445 falls into one of two types of user accessibility:

- 1) Read only (Reg0, Reg1)
- 2) Write/Read same address (Reg3, Reg4, Reg5)

There are 7 bytes in each register (56 bits), and data must be read and written in blocks of 7 bytes. [Figure 14](#) depicts the ordering of the bytes transmitted in each frame and the bits within each byte. In the read sequence depicted in [Figure 15](#) the data bytes are transmitted in Frames 5 through 11, starting from the LSByte, DATA1, and ending with MSByte, DATA7. In the write sequence depicted in [Figure 16](#), the data bytes are transmitted in Frames 4 through 11. Only the 100kHz data rate is supported. Please refer to “The I2C Bus Specification” version 2.1 (Doc#: 939839340011) for more documentation on the I2C bus.

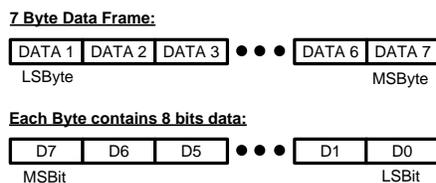


Figure 14. Endianness Diagram

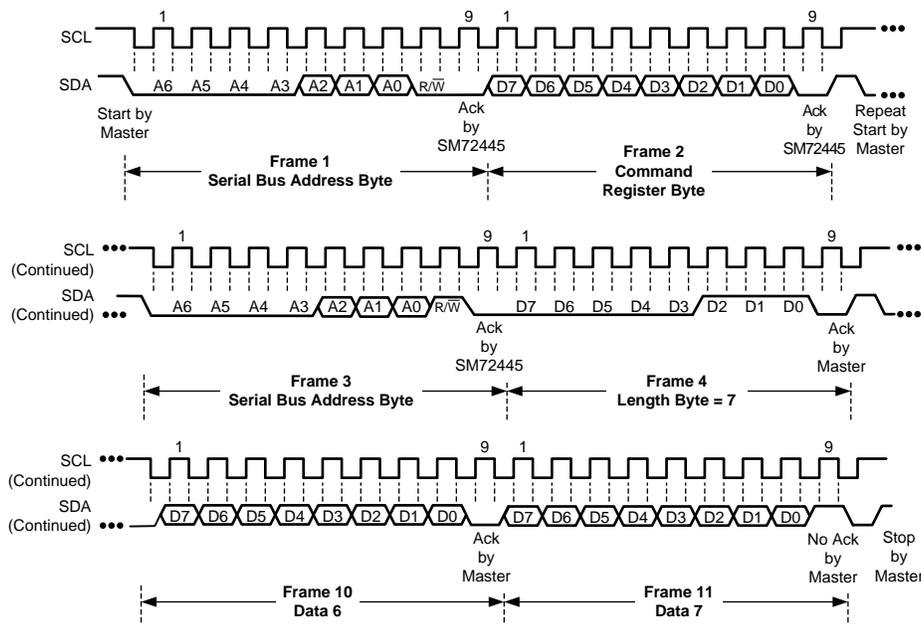


Figure 15. I2C Read Sequence

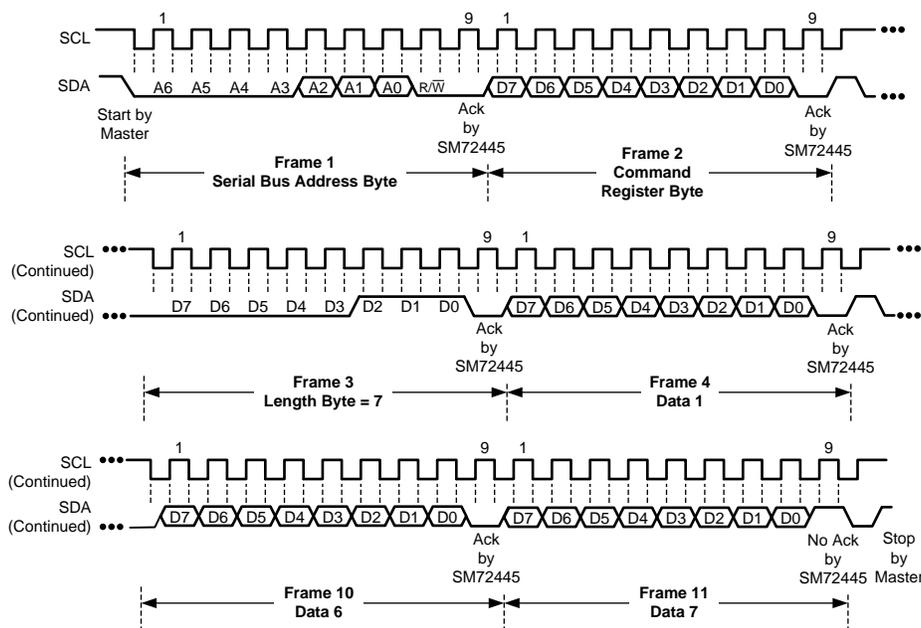


Figure 16. I2C Write Sequence

Noise coupling into digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV below GND, may prevent successful I2C communication with SM72445. I2C no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the I2C maximum frequency of communication is rather low (400 kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed board traces. Additional resistance can be added in series with the SDA and SCL lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SDA and SCL lines.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SM72445MT/NOPB | ACTIVE | TSSOP | PW | 28 | 48 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | SM72445 MT | Samples |
| SM72445MTE/NOPB | ACTIVE | TSSOP | PW | 28 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | SM72445 MT | Samples |
| SM72445MTX/NOPB | ACTIVE | TSSOP | PW | 28 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | SM72445 MT | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

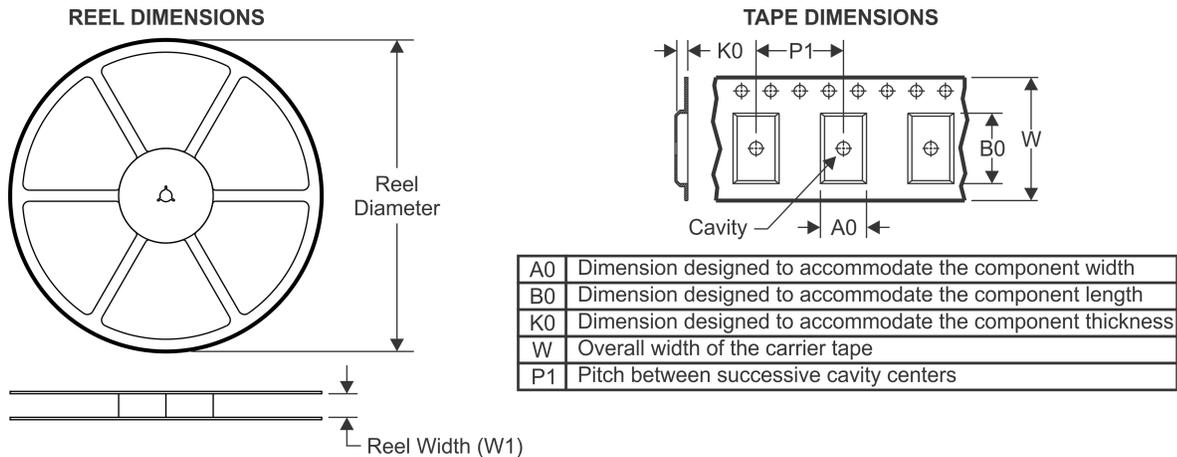
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

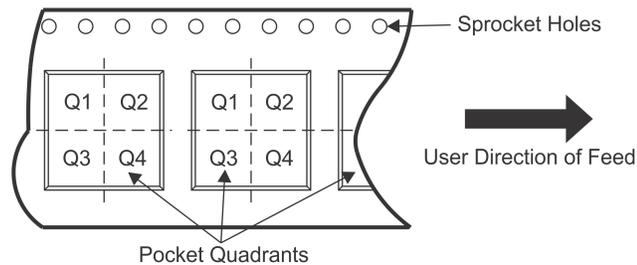
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

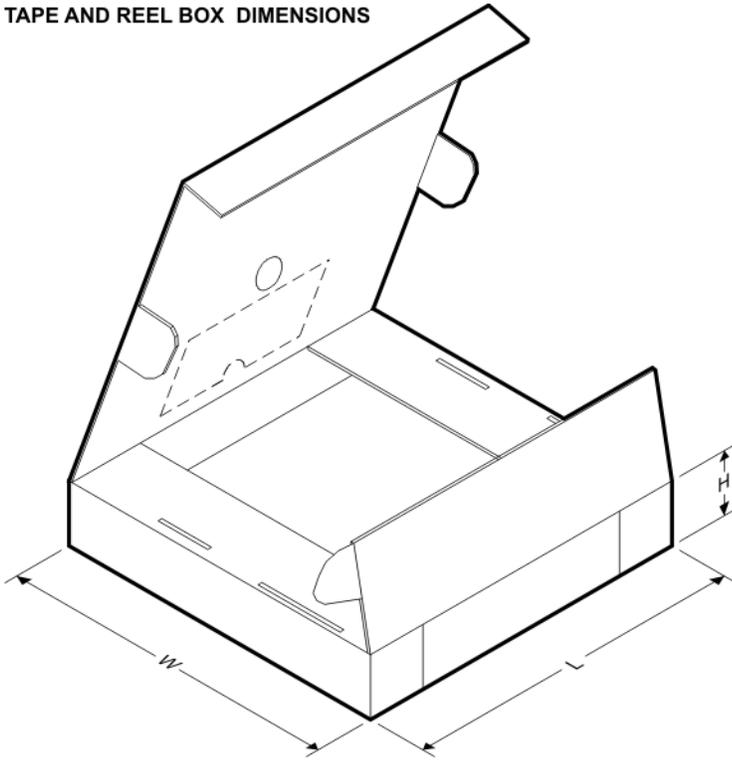


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SM72445MTE/NOPB | TSSOP | PW | 28 | 250 | 178.0 | 16.4 | 6.8 | 10.2 | 1.6 | 8.0 | 16.0 | Q1 |
| SM72445MTX/NOPB | TSSOP | PW | 28 | 2500 | 330.0 | 16.4 | 6.8 | 10.2 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


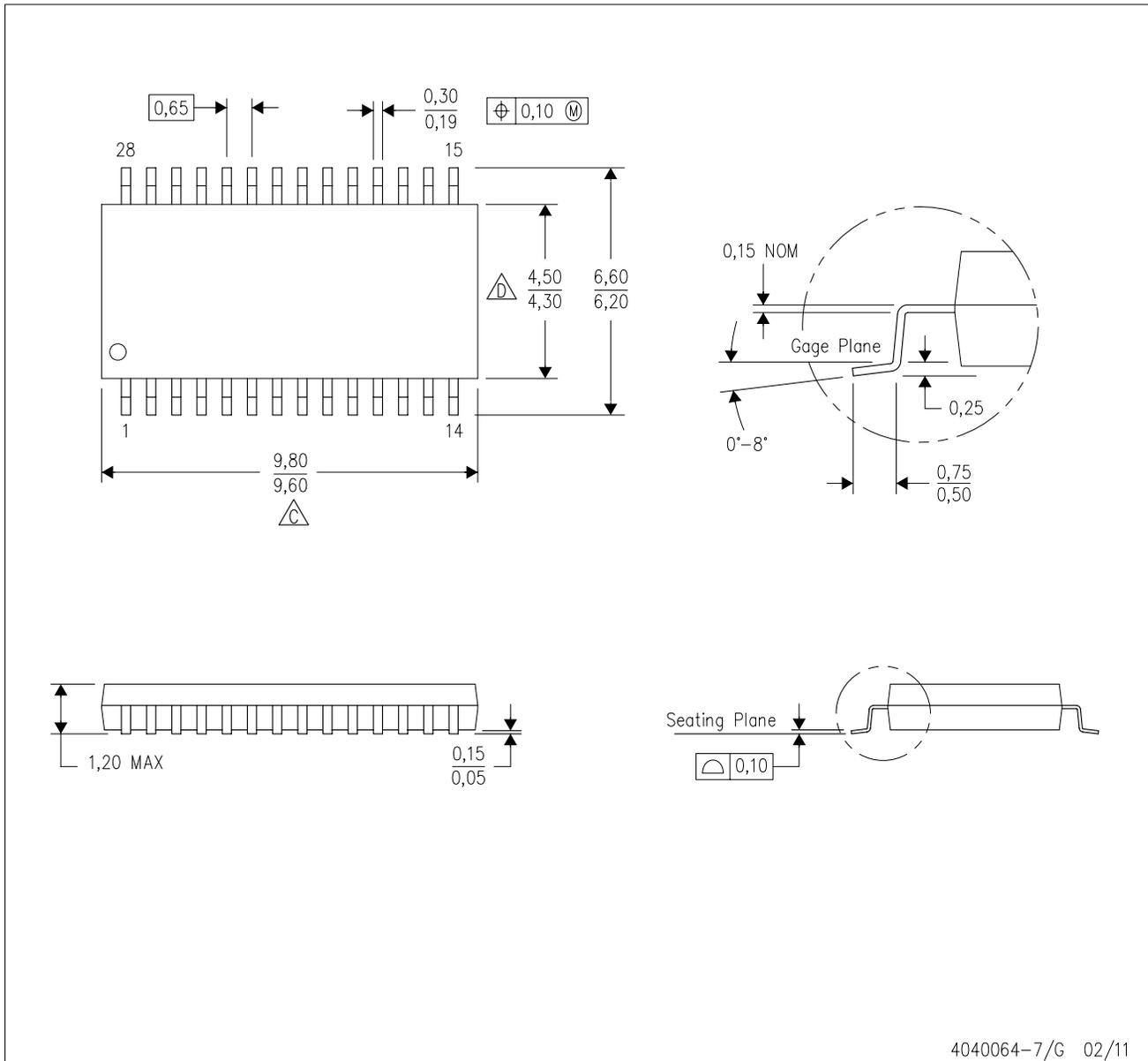
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SM72445MTE/NOPB | TSSOP | PW | 28 | 250 | 210.0 | 185.0 | 35.0 |
| SM72445MTX/NOPB | TSSOP | PW | 28 | 2500 | 367.0 | 367.0 | 38.0 |

MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.