NCV7356

CAN Transceiver, Single Wire

The NCV7356 is a physical layer device for a single wire data link capable of operating with various Carrier Sense Multiple Access with Collision Resolution (CSMA/CR) protocols such as the Bosch Controller Area Network (CAN) version 2.0. This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor and/or dedicated logic devices which use the network.

The network shall be able to operate in either the normal data rate mode or a high−speed data download mode for assembly line and service data transfer operations. The high−speed mode is only intended to be operational when the bus is attached to an off−board service node. This node shall provide temporary bus electrical loads which facilitate higher speed operation. Such temporary loads should be removed when not performing download operations.

The bit rate for normal communications is typically 33 kbit/s, for high−speed transmissions like described above a typical bit rate of 83 kbit/s is recommended. The NCV7356 features undervoltage lockout, timeout for faulty blocked input signals, output blanking time in case of bus ringing and a very low sleep mode current.

The device is compliant with GMW3089V2.4 General Motors Corporation specification.

Features

- Fully Compatible with J2411 Single Wire CAN Specification
- 60 μA (max) Sleep Mode Current
- Operating Voltage Range 5.0 to 27 V
- Up to 100 kbps High−Speed Transmission Mode
- Up to 40 kbps Bus Speed
- Selective BUS Wake−Up
- Logic Inputs Compatible with 3.3 V and 5 V Supply Systems
- Control Pin for External Voltage Regulators (14 Pin Package Only)
- Standby to Sleep Mode Timeout
- Low RFI Due to Output Wave Shaping
- Fully Integrated Receiver Filter
- Bus Terminals Short−Circuit and Transient Proof
- Loss of Ground Protection
- Protection Against Load Dump, Jump Start
- Thermal Overload and Short Circuit Protection
- ESD Protection of 4.0 kV on CANH Pin (2.0 kV on Any Other Pin)
- Undervoltage Lock Out
- Bus Dominant Timeout Feature
- Internally Fused Leads in SO−14 Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

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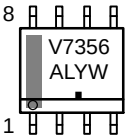
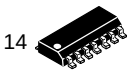
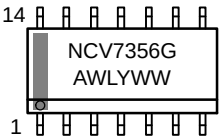
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751



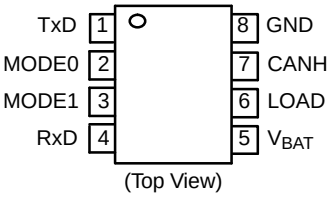


SOIC−14
D SUFFIX
CASE 751A

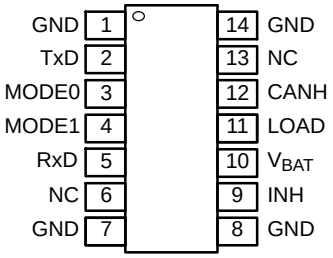


A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
▪ or G = Pb−Free Package

PIN CONNECTIONS



(Top View)

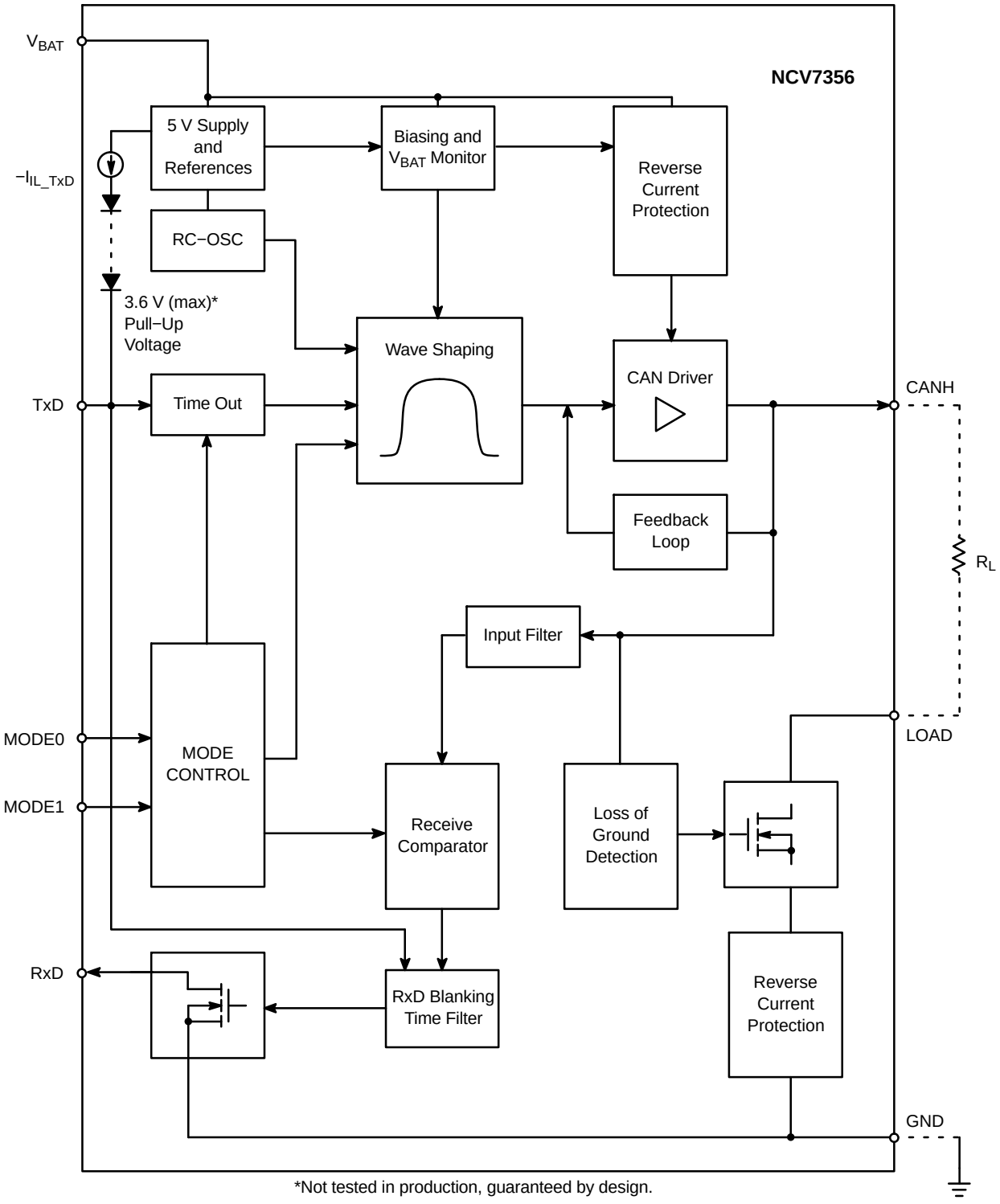


(Top View)

ORDERING INFORMATION

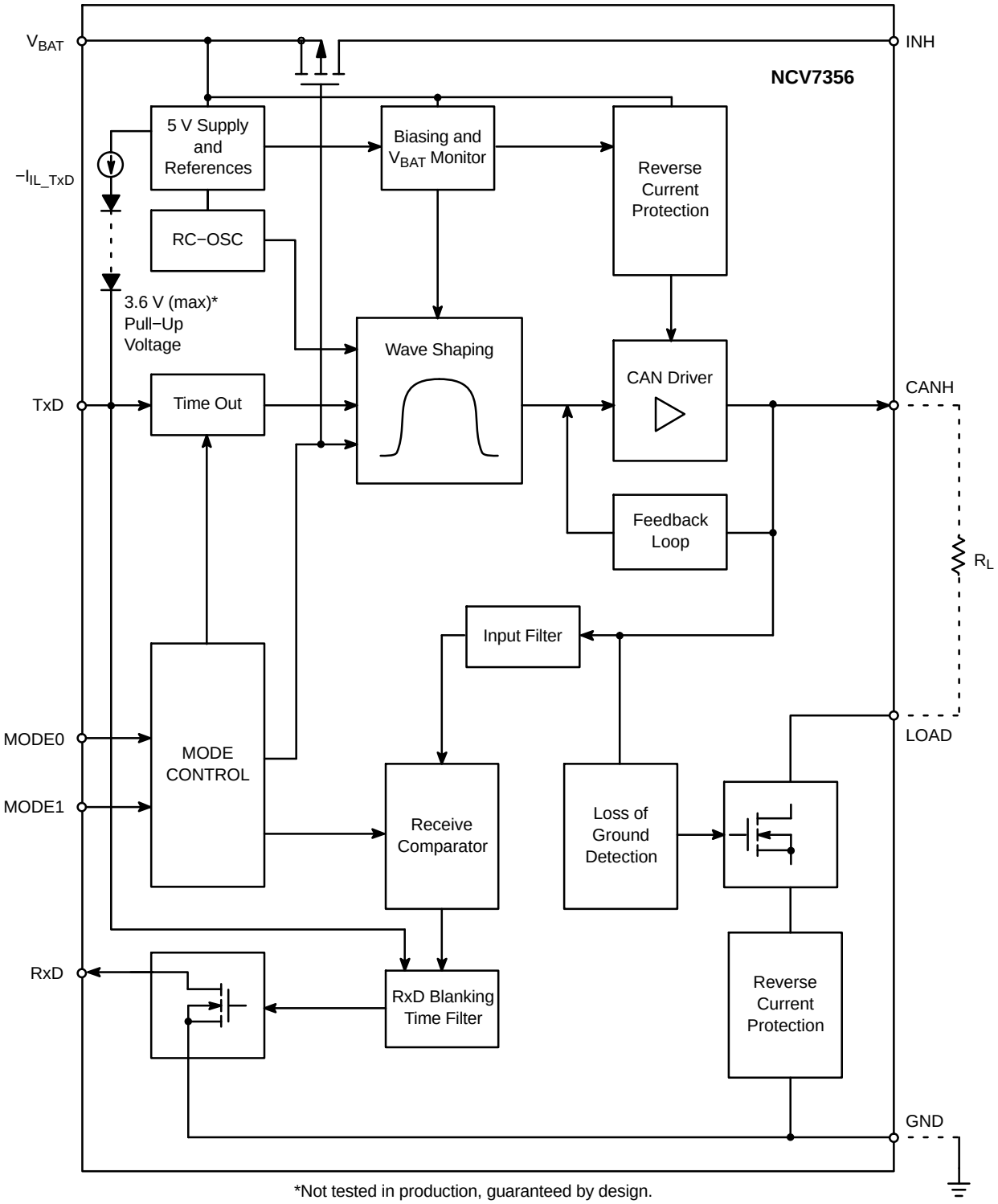
Device	Package	Shipping†
NCV7356D1G	SOIC−8 (Pb−Free)	98 Units / Rail
NCV7356D1R2G	SOIC−8 (Pb−Free)	2500 Tape & Reel
NCV7356D2G	SOIC−14 (Pb−Free)	55 Units / Rail
NCV7356D2R2G	SOIC−14 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



*Not tested in production, guaranteed by design.

Figure 1. 8−Pin Package Block Diagram



*Not tested in production, guaranteed by design.

Figure 2. 14−Pin Package Block Diagram

PACKAGE PIN DESCRIPTION

SOIC−8	SOIC−14	Symbol	Description
1	2	TxD	Transmit data from microprocessor to CAN.
2	3	MODE0	Operating mode select input 0.
3	4	MODE1	Operating mode select input 1.
4	5	RxD	Receive data from CAN to microprocessor.
5	10	V_{BAT}	Battery input voltage.
6	11	LOAD	Resistor load (loss of ground detection low side switch).
7	12	CANH	Single wire CAN bus pin.
8	1, 7, 8, 14	GND	Ground
−	6, 13	NC	No Connection (Note 1)
−	9	INH	Control pin for external voltage regulator (high voltage high side switch) (14 pin package only)

1. PWB terminal 13 can be connected to ground which will allow the board to be assembled with either the 8 pin package or the 14 pin package.

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
Supply Voltage, Normal Operation	V_{BAT}	−	−0.3	18	V
Short−Term Supply Voltage, Transient	$V_{BAT.LD}$	Load Dump; t < 500 ms	−	40	V (peak)
		Jump Start; t < 1.0 min	−	27	V
Transient Supply Voltage	$V_{BAT.TR1}$	ISO 7637/1 Pulse 1 (Note 2)	−50	−	V
Transient Supply Voltage	$V_{BAT.TR2}$	ISO 7637/1 Pulses 2 (Note 2)	−	100	V
Transient Supply Voltage	$V_{BAT.TR3}$	ISO 7637/1 Pulses 3A, 3B	−200	200	V
CANH Voltage	V_{CANH}	V_{BAT} < 27 V	−20	40	V
		V_{BAT} = 0 V	−40		
Transient Bus Voltage	$V_{CANHTR1}$	ISO 7637/1 Pulse 1 (Note 3)	−50	−	V
Transient Bus Voltage	$V_{CANHTR2}$	ISO 7637/1 Pulses 2 (Note 3)	−	100	V
Transient Bus Voltage	$V_{CANHTR3}$	ISO 7637/1 Pulses 3A, 3B (Note 3)	−200	200	V
DC Voltage on Pin LOAD	V_{LOAD}	Via RT > 2.0 kΩ	−40	40	V
DC Voltage on Pins TxD, MODE1, MODE0, RxD	V_{DC}	−	−0.3	7.0	V
ESD Capability of CANH (Note 4)	V_{ESDBUS}	Human Body Model (with respect to V_{BAT} and GND) Eq. to Discharge 100 pF with 1.5 kΩ	−4000	4000	V
ESD Capability of Any Other Pin (Note 4)	V_{ESD}	Human Body Model Eq. to Discharge 100 pF with 1.5 kΩ	−2000	2000	V
Maximum Latchup Free Current at Any Pin	I_{LATCH}	−	−500	500	mA
Storage Temperature	T_{STG}	−	−55	150	°C
Junction Temperature	T_J	−	−40	150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 s to 150 s above 217°C (Note 5)				260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. ISO 7637 test pulses are applied to V_{BAT} via a reverse polarity diode and >1.0 μF blocking capacitor.
3. ISO 7637 test pulses are applied to CANH via a coupling capacitance of 1.0 nF.
4. ESD measured per Q100−002 (EIA/JESD22−A114−A).
5. For additional information, please see or download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TYPICAL THERMAL CHARACTERISTICS

Parameter	Test Condition, Typical Value		Unit
	Min Pad Board	1″ Pad Board	
SOIC−8			
Junction−to−Lead (psi−JL7, Ψ_{JL8}) or Pins 6−7	57 (Note 6)	51 (Note 7)	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	187 (Note 6)	128 (Note 7)	°C/W
SOIC−14			
Junction−to−Lead (psi−JL8, Ψ_{JL8})	30 (Note 8)	30 (Note 9)	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	122 (Note 8)	84 (Note 9)	°C/W

6. 1 oz copper, 53 mm^2 coper area, 0.062″ thick FR4.
7. 1 oz copper, 716 mm^2 coper area, 0.062″ thick FR4.
8. 1 oz copper, 94 mm^2 coper area, 0.062″ thick FR4.
9. 1 oz copper, 767 mm^2 coper area, 0.062″ thick FR4.

ELECTRICAL CHARACTERISTICS (V_{BAT} = 5.0 to 27 V, T_A = −40 to +125°C, unless otherwise specified.)

Characteristic	Symbol	Condition		Min	Typ	Max	Unit
GENERAL							
Undervoltage Lock Out	V_{BATuv}	−		3.5	−	4.8	V
Supply Current, Recessive, All Active Modes	I_{BATN}	V_{BAT} = 18 V, TxD Open	Not High Speed Mode	−	5.0	6.0	mA
			High Speed Mode	−	−	8.0	
Normal Mode Supply Current, Dominant	I_{BATN} (Note 11)	V_{BAT} = 27 V, MODE0 = MODE1 = H, TxD = L, R_L = 200 Ω		−	30	35	mA
High−Speed Mode Supply Current, Dominant	I_{BATN} (Note 11)	V_{BAT} = 16 V, MODE0 = H, MODE1 = L, TxD = L, R_L = 75 Ω		−	70	75	mA
Wake−Up Mode Supply Current, Dominant	I_{BATW} (Note 11)	V_{BAT} = 27 V, MODE0 = L, MODE1 = H, TxD = L, R_L = 200 Ω		−	60	75	mA
Sleep Mode Supply Current (Note 10)	I_{BATS}	V_{BAT} = 13 V, T_A = 85°C, TxD, RxD, MODE0, MODE1 Open		−	30	60	μA
Thermal Shutdown (Note 11)	T_{SD}	−		155	−	180	°C
Thermal Recovery (Note 11)	T_{REC}	−		126	−	150	°C
CANH							
Bus Output Voltage	V_{oh}	R_L > 200 Ω, Normal Mode 6.0 V < V_{BAT} < 27 V		4.4	−	5.1	V
Bus Output Voltage Low Battery	V_{oh}	R_L > 200 Ω, Normal High−Speed Mode 5.0 V < V_{BAT} < 6.0 V		3.4	−	5.1	V
Bus Output Voltage High−Speed Mode	V_{oh}	R_L > 75 Ω, High−Speed Mode 8.0 V < V_{BAT} < 16 V		4.2	−	5.1	V
HV Fixed Wake−Up Output High Voltage	$V_{ohWuFix}$	Wake−Up Mode, R_L > 200 Ω, 11.4 V < V_{BAT} < 27 V		9.9	−	12.5	V
HV Offset Wake−Up Output High Voltage	$V_{ohWuOffset}$	Wake−Up Mode, R_L > 200 Ω, 5.0 V < V_{BAT} < 11.4 V		V_{BAT} −1.5	−	V_{BAT}	V
Recessive State Output Voltage	V_{ol}	Recessive State or Sleep Mode, R_L = 6.5 kΩ		−0.20	−	0.20	V
Bus Short Circuit Current	$-I_{CAN\_SHORT}$	V_{CANH} = 0 V, V_{BAT} = 27 V, TxD = 0 V		50	−	350	mA
Bus Leakage Current During Loss of Ground	I_{LKN_CAN} (Note 12)	Loss of Ground, V_{CANH} = 0 V		−50	−	10	μA
Bus Leakage Current, Bus Positive	I_{LKP_CAN}	TxD High		−10	−	10	μA
Bus Input Threshold	V_{ih}	Normal, High−Speed Mode, HVWU 6.0 ≤ V_{BAT} ≤ 27 V		2.0	2.1	2.2	V
Bus Input Threshold Low Battery	V_{ihlb}	Normal, V_{BAT} = 5.0 V to 6.0 V		1.6	1.7	2.2	V
Fixed Wake−Up from Sleep Input High Voltage Threshold	$V_{ihWuFix}$ (Note 11)	Sleep Mode, V_{BAT} > 10.9 V		6.6	−	7.9	V
Offset Wake−Up from Sleep Input High Voltage Threshold	$V_{ihWuOffset}$ (Note 11)	Sleep Mode		V_{BAT} −4.3	−	V_{BAT} −3.25	V
LOAD							
Voltage on Switched Ground Pin	V_{LOAD_1mA}	I_{LOAD} = 1.0 mA		−	−	0.1	V
Voltage on Switched Ground Pin	V_{LOAD}	I_{LOAD} = 5.0 mA		−	−	0.5	V
Voltage on Switched Ground Pin	V_{LOAD_LOB}	I_{LOAD} = 7.0 mA, V_{BAT} = 0 V		−	−	1.0	V
Load Resistance During Loss of Battery	R_{LOAD_LOB}	V_{BAT} = 0		R_L −10%	−	R_L +35%	Ω

10. Characterization data supports I_{BATS} < 65 μA with conditions V_{BAT} = 18 V, T_A = 125°C
11. Thresholds not tested in production, guaranteed by design.
12. Leakage current in case of loss of ground is the summary of both currents I_{LKN_CAN} and I_{LKN_LOAD}.

ELECTRICAL CHARACTERISTICS (continued) (V_{BAT} = 5.0 to 27 V, T_A = −40 to +125°C, unless otherwise specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
TXD, MODE0, MODE1						
High Level Input Voltage	V_{ih}	6.0 < V_{BAT} < 27 V	2.0	−	−	V
Low Level Input Voltage	V_{il}	6.0 < V_{BAT} < 27 V	−	−	0.8	V
TxD Pullup Current	$-I_{IL\_TXD}$	TxD = L, MODE0 and 1 = H 5.0 < V_{BAT} < 27 V	10	−	50	μA
MODE0 and 1 Pulldown Resistor	R_{MODE_pd}		10	−	50	kΩ
RXD						
Low Level Output Voltage	V_{ol_rxd}	I_{RxD} = 2.0 mA	−	−	0.4	V
High Level Output Leakage	I_{ih_rxd}	V_{RxD} = 5.0 V	−10	−	10	μA
RxD Output Current	Irxd	V_{RxD} = 5.0 V	−	−	70	mA
INH (14 Pin Package Only)						
High Level Output Voltage	V_{oh_INH}	I_{INH} = −180 μA	V_{BAT} −0.8	V_{BAT} −0.5	V_{BAT}	V
Leakage Current	I_{INH_lk}	MODE0 = MODE1 = L, INH = 0 V	−5.0	−	5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

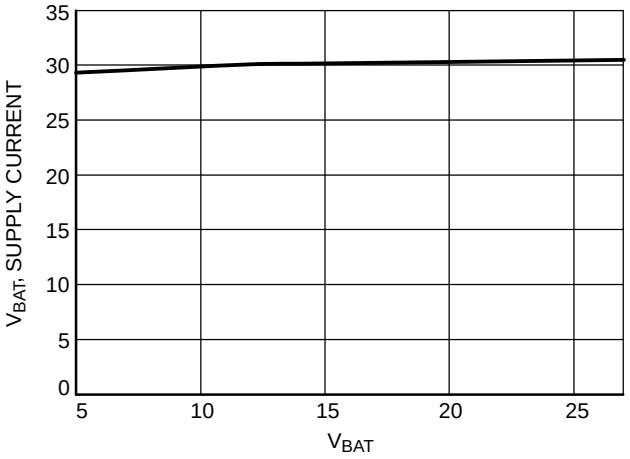


Figure 3. Normal Mode Supply Current Dominant vs. V_{BAT}

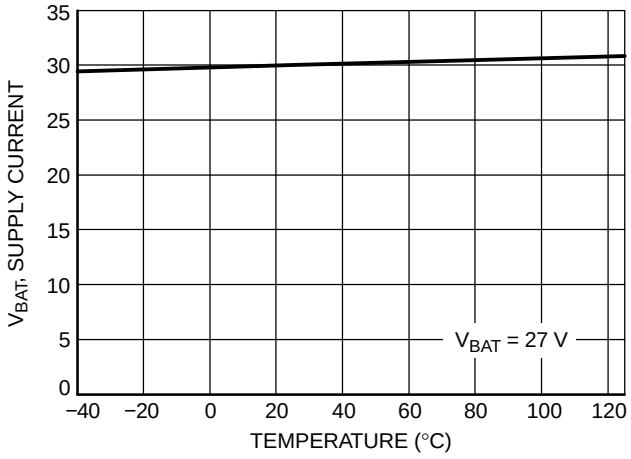


Figure 4. Normal Mode Supply Current Dominant vs. Temperature

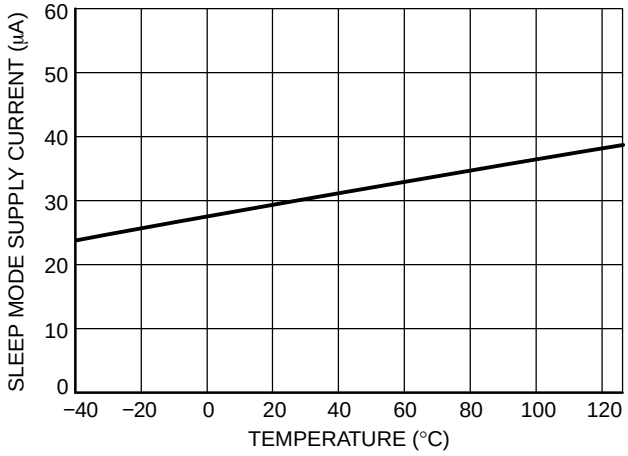


Figure 5. Sleep Mode Supply Current vs. Temperature

TIMING MEASUREMENT LOAD CONDITIONS

Normal and High Voltage Wake−Up Mode		High−Speed Mode
min load / min tau	3.3 kΩ / 540 pF	Additional 140 Ω tool resistance to ground in parallel
min load / max tau	3.3 kΩ / 1.2 nF	
max load / min tau	200 Ω / 5.0 nF	Additional 120 Ω tool resistance to ground in parallel
max load / max tau	200 Ω / 20 nF	

ELECTRICAL CHARACTERISTICS (5.0 V ≤ V_{BAT} ≤ 27 V, −40°C ≤ T_A ≤ 125°C, unless otherwise specified.)
AC CHARACTERISTICS (See Figures 6, 7, and 8)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Transmit Delay in Normal and Wake−Up Mode, Bus Rising Edge (Notes 13, 14)	t_{Tr}	Min and Max Loads per Timing Measurement Load Conditions	2.0	−	6.3	μs
Transmit Delay in Wake−Up Mode to V_{ihWU}, Bus Rising Edge (Notes 13, 15)	t_{TWUr}	Min and Max Loads per Timing Measurement Load Conditions	2.0	−	18	μs
Transmit Delay in Normal Mode, Bus Falling Edge (Notes 16, 17)	t_{Tf}	Min and Max Loads per Timing Measurement Load Conditions	1.8	−	10	μs
Transmit Delay in Wake−Up Mode, Bus Falling Edge (Notes 16, 17)	t_{TWU1f}	Min and Max Loads per Timing Measurement Load Conditions	3.0	−	13.7	μs
Transmit Delay in High−Speed Mode, Bus Rising Edge (Notes 13, 18)	t_{THSr}	Min and Max Loads per Timing Measurement Load Conditions	0.1	−	1.5	μs
Transmit Delay in High−Speed Mode, Bus Falling Edge (Notes 17, 19)	t_{THSf}	Min and Max Loads per Timing Measurement Load Conditions	0.04	−	3.0	μs
Receive Delay, All Active Modes (Note 20)	t_{DR}	CANH High to Low Transition	0.3	−	1.0	μs
Receive Delay, All Active Modes (Note 20)	t_{RD}	CANH Low to High Transition	0.3	−	1.0	μs
Input Minimum Pulse Length, All Active Modes (Note 18)	t_{mpDR} t_{mpRD}	CANH High to Low Transition CANH Low to High Transition	0.1 0.1	− −	1.0 1.0	μs
Wake−Up Filter Time Delay	t_{WUF}	See Figure 7	10	−	70	μs
Receive Blanking Time, After TxD L−H Transition	t_{rb}	See Figure 8	0.5	−	6.0	μs
TxD Timeout Reaction Time	t_{tout}	Normal and High−Speed Mode	−	17	−	ms
TxD Timeout Reaction Time	t_{toutwu}	Wake−Up Mode	−	17	−	ms
Delay from Normal to High−Speed and High Voltage Wake−Up Mode	t_{dnhs}	−	−	−	30	ms
Delay from High−Speed and High Voltage Wake−Up to Normal Mode	t_{dhsn}	−	−	−	30	ms
Delay from Normal to Standby Mode	t_{dsby}	V_{BAT} = 6.0 V to 27 V	−	−	500	μs
Delay from Sleep to Normal Mode	t_{dsnwu}	V_{BAT} = 6.0 V to 27 V	−	−	50	ms
Delay from Sleep to High Voltage Mode	t_{dshv}	V_{BAT} = 6.0 V to 27 V	−	−	50	ms
Delay from Standby to Sleep Mode (Note 21)	t_{dsleep}	V_{BAT} = 6.0 V to 27 V	100	250	500	ms

13. Minimum signal delay time is measured from the TxD voltage threshold to CANH = 1.0 V. τ load should be min per the Timing Measurement Load Conditions table.
14. Maximum signal delay time is measured from the TxD voltage threshold to CANH = 3.5 V at V_{BAT} = 27 V, CANH = 2.8 V at V_{BAT} = 5.0 V. τ load should be max per the Timing Measurement Load Conditions table.
15. Maximum signal delay time is measured from the TxD voltage threshold to CANH = 9.2 V. $V_{ihwumax}$ = $V_{ihwufix}$, max + V_{goff} = 7.9 V + 1.3 V = 9.2 V. τ load should be max per the Timing Measurement Load Conditions table.
16. Minimum signal delay time is measured from the TxD voltage threshold to CANH = 3.5 V at V_{BAT} = 27 V, CANH = 2.8 V at V_{BAT} = 5.0 V. τ load should be min per the Timing Measurement Load Conditions table.
17. Maximum signal delay time is measured from the TxD voltage threshold to CANH = 1 V. τ load should be max per the Timing Measurement Load Conditions table.
18. Maximum signal delay time is measured from the TxD voltage threshold to CANH = 3.5 V. τ load should be max per the Timing Measurement Load Conditions table.
19. Minimum signal delay time is measured from the TxD voltage threshold to CANH = 3.5 V. τ load should be min per the Timing Measurement Load Conditions table.
20. Receive delay time is measured from the rising / falling edge crossing of the nominal V_{ih} value on CANH to the falling ($V_{cmos\_il\_max}$) / rising ($V_{cmos\_ih\_min}$) edge of RxD. This parameter is tested by applying a square wave signal to CANH. The minimum slew rate for the bus rising and falling edges is 50 V/μs. The low level on bus is always 0 V. For normal mode and high−speed mode testing the high level on bus is 4 V. For HVWU mode testing the high level on bus is V_{BAT} − 2 V. Relaxation of this non−critical parameter from 0.15 μs to 0.10 μs may be addressed in future revisions of GMW3089.
21. Tested on 14 Pin package only.

BUS LOADING REQUIREMENTS

Characteristic	Symbol	Min	Typ	Max	Unit
Number of System Nodes	–	2	–	32	–
Network Distance Between Any Two ECU Nodes	Bus Length	–	–	60	m
Node Series Inductor Resistance (If required)	R_{ind}	–	–	3.5	Ω
Ground Offset Voltage	V_{goff}	–	–	1.3	V
Ground Offset Voltage, Low Battery	$V_{gofflowbat}$	–	0.1 x V_{BAT}	0.7	V
Device Capacitance (Unit Load)	C_{ul}	135	150	300	pF
Network Total Capacitance	C_{tl}	396	–	19000	pF
Device Resistance (Unit Load)	R_{ul}	6435	6490	6565	Ω
Device Resistance (Min Load)	R_{min}	2000	–	–	Ω
Network Total Resistance	R_{tl}	200	–	4596	Ω
Network Time Constant (Note 22)	τ	1.0	–	4.0	μs
Network Time Constant in High−Speed Mode	τ	–	–	1.5	μs
High−Speed Mode Network Resistance to GND	R_{load}	75	–	135	Ω

22. The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emission. The maximum value is selected to ensure proper communication modes. Not all combinations of R and C are possible.

TIMING DIAGRAMS

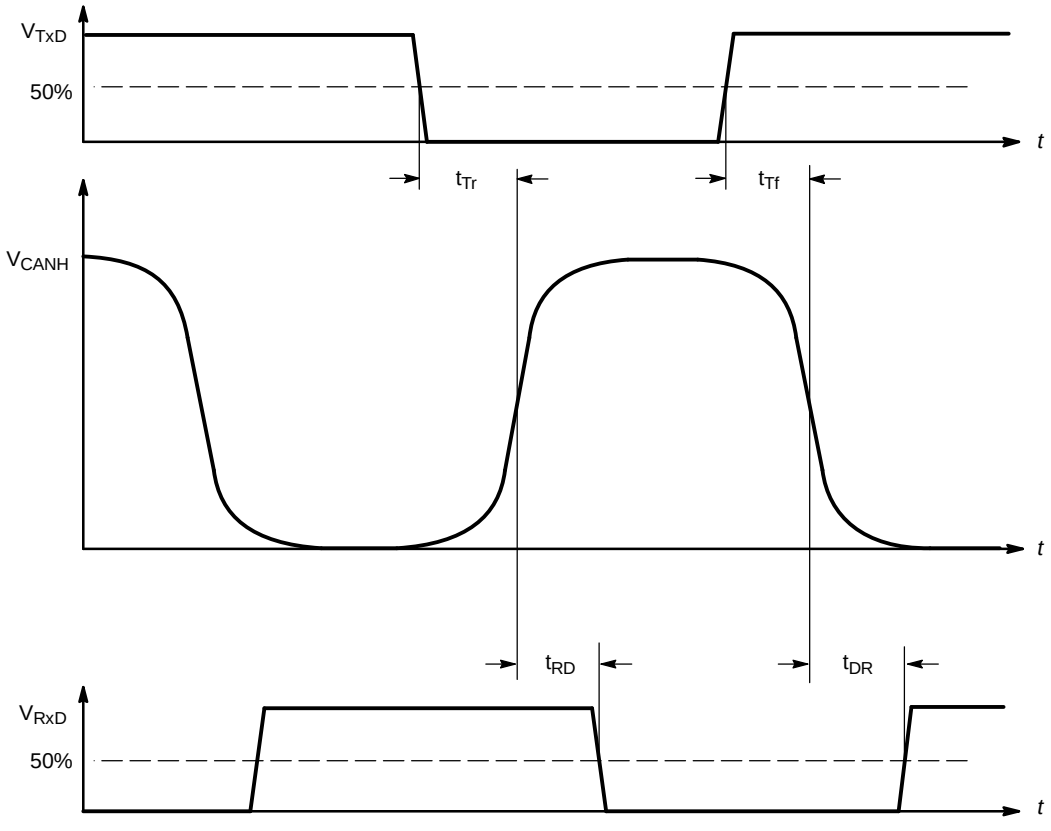


Figure 6. Input/Output Timing

TIMING DIAGRAMS

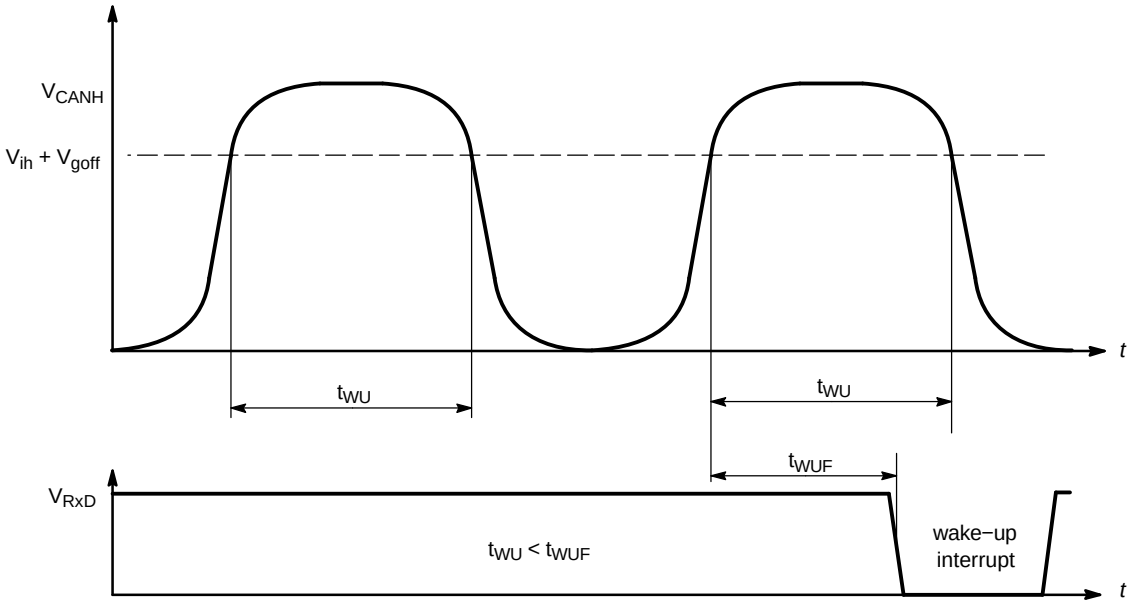


Figure 7. Wake−Up Filter Time Delay

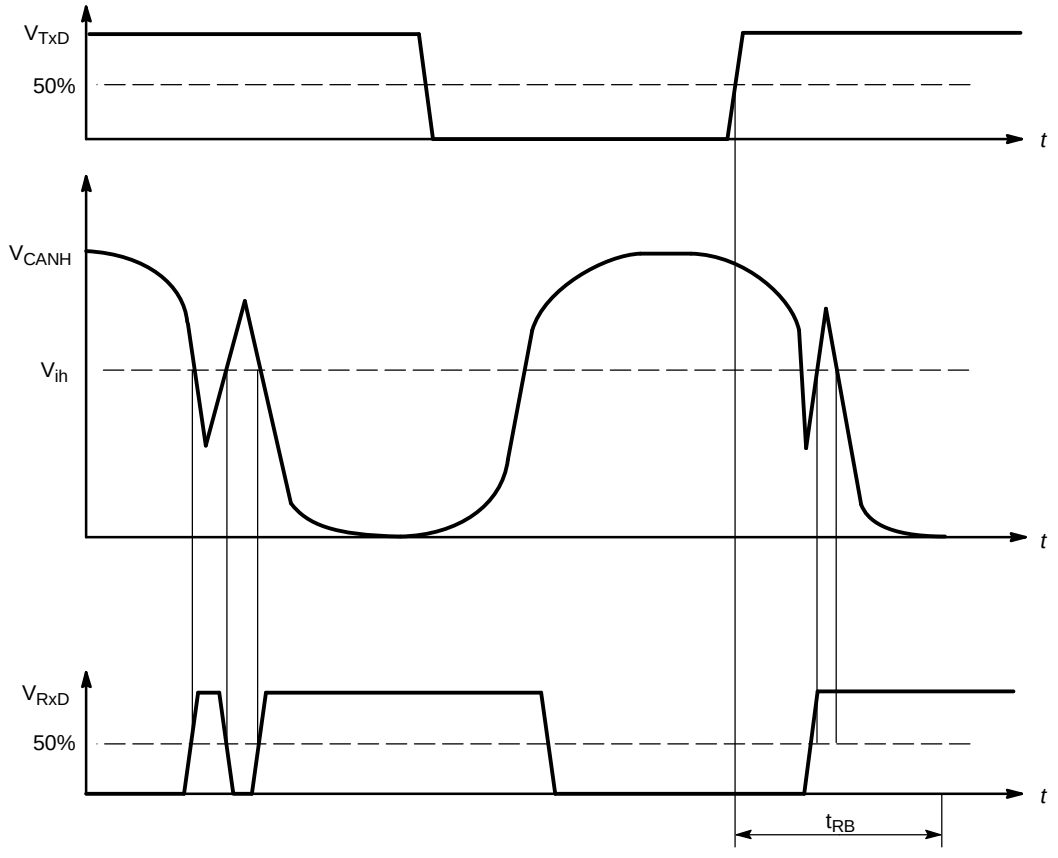


Figure 8. Receive Blanking Time

FUNCTIONAL DESCRIPTION

TxD Input Pin

TxD Polarity

- TxD = logic 1 (or floating) on this pin produces an undriven or recessive bus state (low bus voltage)
- TxD = logic 0 on this pin produces either a bus normal or a bus high voltage dominant state depending on the transceiver mode state (high bus voltage)

If the TxD pin is driven to a logic low state while the sleep mode (Mode 0 = 0 and Mode 1 = 0) is activated, the transceiver can not drive the CANH pin to the dominant state.

The transceiver provides an internal pull−up current on the TxD pin (only in active modes [High−Speed Mode, High Voltage Wake−Up, and Normal Mode]) which will cause the transmitter to default to the bus recessive state when TxD is not driven. The internal current source circuitry limits the voltage pull−up level to be compatible with 3.3 V logic. The TxD pull−up current source is not active in Sleep Mode.

TxD input signals are standard CMOS logic levels.

Timeout Feature

In case of a faulty blocked dominant TxD input signal, the CANH output is switched off automatically after the specified TxD timeout reaction time to prevent a dominant bus.

The transmission is continued by next TxD L to H transition without delay.

MODE0 and MODE1 Pins

The transceiver provides a weak internal pulldown current on each of these pins which causes the transceiver to default to sleep mode when they are not driven. The mode input signals are standard CMOS logic level for 3.3 V and 5 V supply voltages. See Electrical Characteristics table for timing limitations for mode changes.

MODE0	MODE1	Mode
L	L	Sleep Mode
H	L	High−Speed Mode
L	H	High Voltage Wake−Up
H	H	Normal Mode

Sleep Mode

Transceiver is in low power state, waiting for wake−up via high voltage signal or by mode pins change to any state other than 0,0. In this state, the CANH pin is not in the dominant state regardless of the state of the TxD pin.

High−Speed Mode

This mode allows high−speed download with bit rates up to 100 Kbit/s. The output wave shapingaping circuit is disabled in this mode. Bus transmitter drive circuits for those nodes which are required to communicate in high−speed mode are able to drive reduced bus resistance in this mode.

High Voltage Wake−Up Mode

This bus includes a selective node awake capability, which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake−up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non communicating low power “sleep” state. Communication at the lower, normal voltage levels shall not disturb the sleeping nodes.

Normal Mode

Transmission bit rate in normal communication is 33 Kbits/s. In normal transmission mode the NCV7356 supports controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the RC time constant of the total bus load.

RxD Output Pin

Logic data as sensed on the single wire CAN bus.

RxD Polarity

- RxD = logic 1 on this pin indicates a bus recessive state (low bus voltage)
- RxD = logic 0 on this pin indicates a bus normal or high voltage bus dominant state

RxD in Sleep Mode

RxD does not pass signals to the microprocessor while in sleep mode until a valid wake−up bus voltage level is received or the MODE0 and MODE 1 pins are not 0, 0 respectively. When the valid wake−up bus voltage signal awakens the transceiver, the RxD pin signals an interrupt (logic 0). If there is no mode change within 250 ms (typ), the transceiver re−enters the sleep mode.

When not in sleep mode all valid bus signals will be sent out on the RxD pin.

RxD will be placed in the undriven or off state when in sleep mode.

RxD Typical Load

Resistance: 2.7 kΩ

Capacitance: < 25 pF

Bus LOAD Pin

Bus LOAD Pin Description

The bus LOAD pin provides a network load impedance program point for the CAN bus. The value of the resistor between the CANH and LOAD pins can be adjusted to provide adequate impedance for the bus loading requirements as dictated by the Single Wire CAN Specification (J2411).

The resistor between CANH and LOAD pins provides a pull down impedance for the CANH pin. The CANH driver is a pull−up amplifier with no sink capability.

The bus LOAD pin also provides the detection circuitry for loss of ground detection to insure there are no loading effects on the bus should the ground connection be lost to the NCV7356 device. During a system loss of ground event, CANH with the 6.49 kΩ resistor between CANH and LOAD will affect the bus with only between −50 μA and 10 μA of current (Bus Leakage Current During Loss of Ground).

Resistor ground connection with internal open−on−loss−of−ground protection

When the ECU experiences a loss of ground condition, this pin is switched to a high impedance state.

The ground connection through this pin is not interrupted in any transceiver operating mode including the sleep mode. The ground connection only is interrupted when there is a valid loss of ground condition.

This pin provides the bus load resistor with a path to ground which contributes less than 0.1 V to the bus offset voltage when sinking the maximum current through one unit load resistor. This path exists in all operating modes, including the sleep mode.

The transceiver's maximum bus leakage current contribution to V_{ol} from the LOAD pin when in a loss of ground state is 50 μA over all operating temperatures and $3.5 < V_{BAT} < 27$ V.

V_{BAT} Input Pin

Vehicle Battery Voltage

The transceiver is fully operational as described in the Electrical Characteristics Table over the range $6.0\ V < V_{BAT} < 18\ V$ as measured between the GND pin and the V_{BAT} pin.

For $5.0\ V < V_{Bat} < 6.0\ V$, the bus operates in normal mode with reduced dominant output voltage and reduced receiver input voltage. High voltage wake−up is not possible (dominant output voltage is the same as in normal or high−speed mode).

The transceiver operates in normal mode when $18\ V < V_{Bat} < 27\ V$ at 85°C for one minute.

CAN BUS

Input/Output Pin

The CANH pin is composed of a pull−up amplifier (no sink capability) for driving the single−wire CAN bus. It is designed to drive a 200 Ω load when operating in normal mode and can operate higher 75 Ω loads for High−Speed Mode. The minimum output driver capability is 50 mA, but output shorts to ground can reach 350mA.

Normal CANH output voltages are between 4.4 V and 5.1 V. These amplitudes increase to between 9.9 V and 12.5 V for selective system IC selection in Wake−Up Mode.

The CANH pin also acts as a bus read amplifier. The Bus Wake−Up from Sleep Input Voltage Threshold is between 6.6 V and 7.9 V, but to maintain normal communication, the threshold is 2.1 V.

Wave Shaping in Normal and High Voltage Wake−Up Mode

Wave shaping is incorporated into the transmitter to minimize EMI radiated emissions. An important contributor to emissions is the rise and fall times during output transitions at the "corners" of the voltage waveform. The resultant waveform is one half of a sin wave of frequency 50−65 kHz at the rising waveform edge and one quarter of this sin wave at falling or trailing edge.

Wave Shaping in High−Speed Mode

Wave shaping control of the rising and falling waveform edges are disabled during high−speed mode. EMI emissions requirements are waived during this mode. The waveform rise time in this mode is less than 1.0 μs.

Short Circuits

If the CAN BUS pin is shorted to ground for any duration of time, the current is limited as specified in the Electrical Characteristics Table until an overtemperature shutdown circuit disables the output high side drive source transistor preventing damage to the IC.

Loss of Ground

In case of a valid loss of ground condition, the LOAD pin is switched into high impedance state. The CANH transmission is continued until the undervoltage lock out voltage threshold is detected.

Loss of Battery

In case of loss of battery (V_{BAT} = 0 or open) the transceiver does not disturb bus communication. The maximum reverse current into the power supply system (V_{BAT}) doesn't exceed 500 μA.

INH Pin (14 pin package only)

The INH pin is a high−voltage highside switch used to control the ECU's regulated microcontroller power supply. After power−on, the transceiver automatically enters an intermediate standby mode, the INH output will go high (up to V_{BAT}) turning on the external voltage regulator. The external regulator provides power to the ECU. If there is no mode change within 250 ms (typ), the transceiver re−enters the sleep mode and the INH output goes to logic 0 (floating).

When the transceiver has detected a valid wake−up condition (bus HVWU traffic which exceeds the wake−up filter time delay) the INH output will become high (up to

V_{BAT}) again and the same procedure starts as described after power−on. In case of a mode change into any active mode, the sleep timer is stopped and INH stays high (up to V_{BAT}). If the transceiver enters the sleep mode, INH goes to logic 0 (floating) after 250 ms (typ) when no wake−up signal is present.

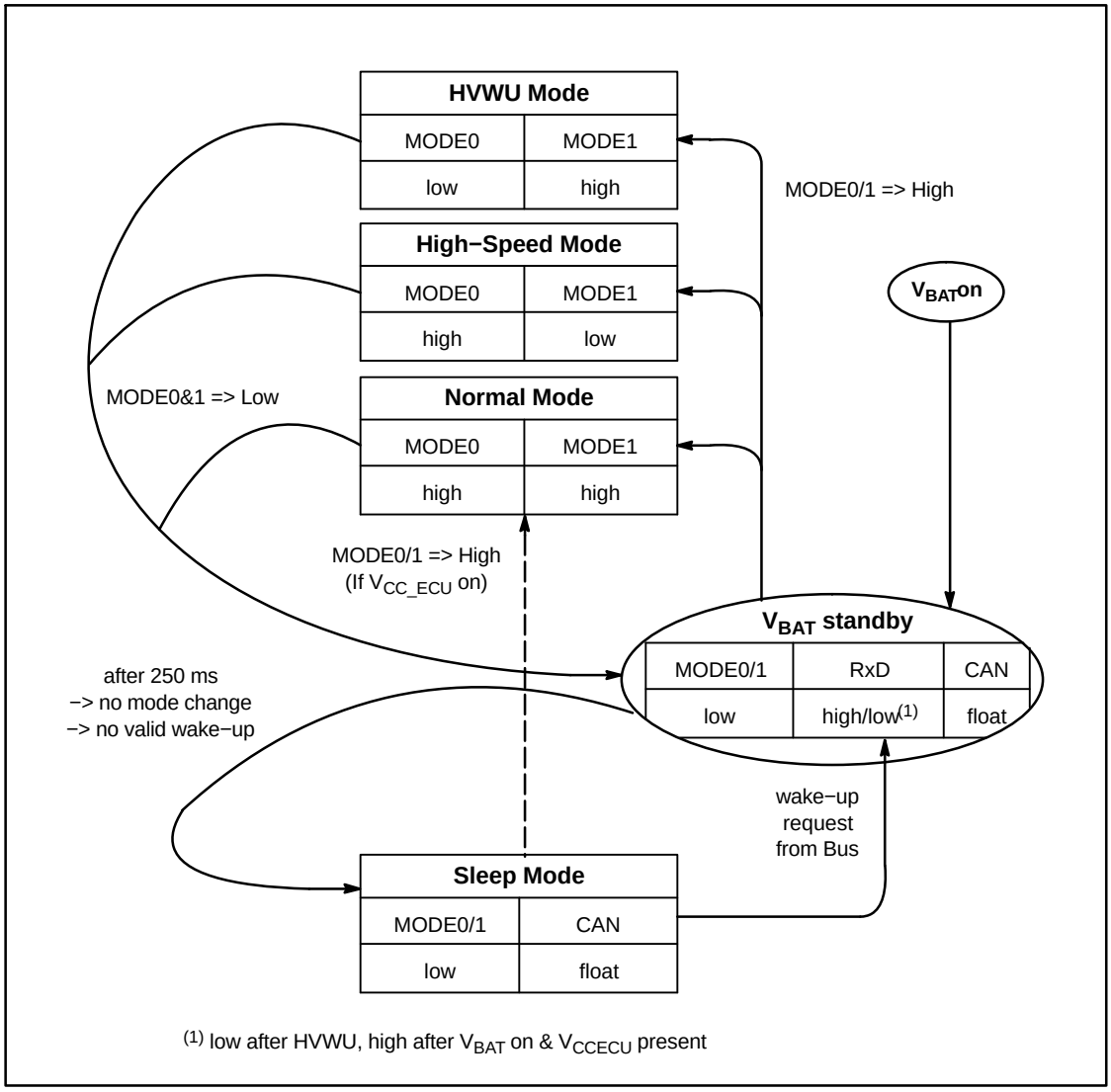


Figure 9. State Diagram, 8 Pin Package

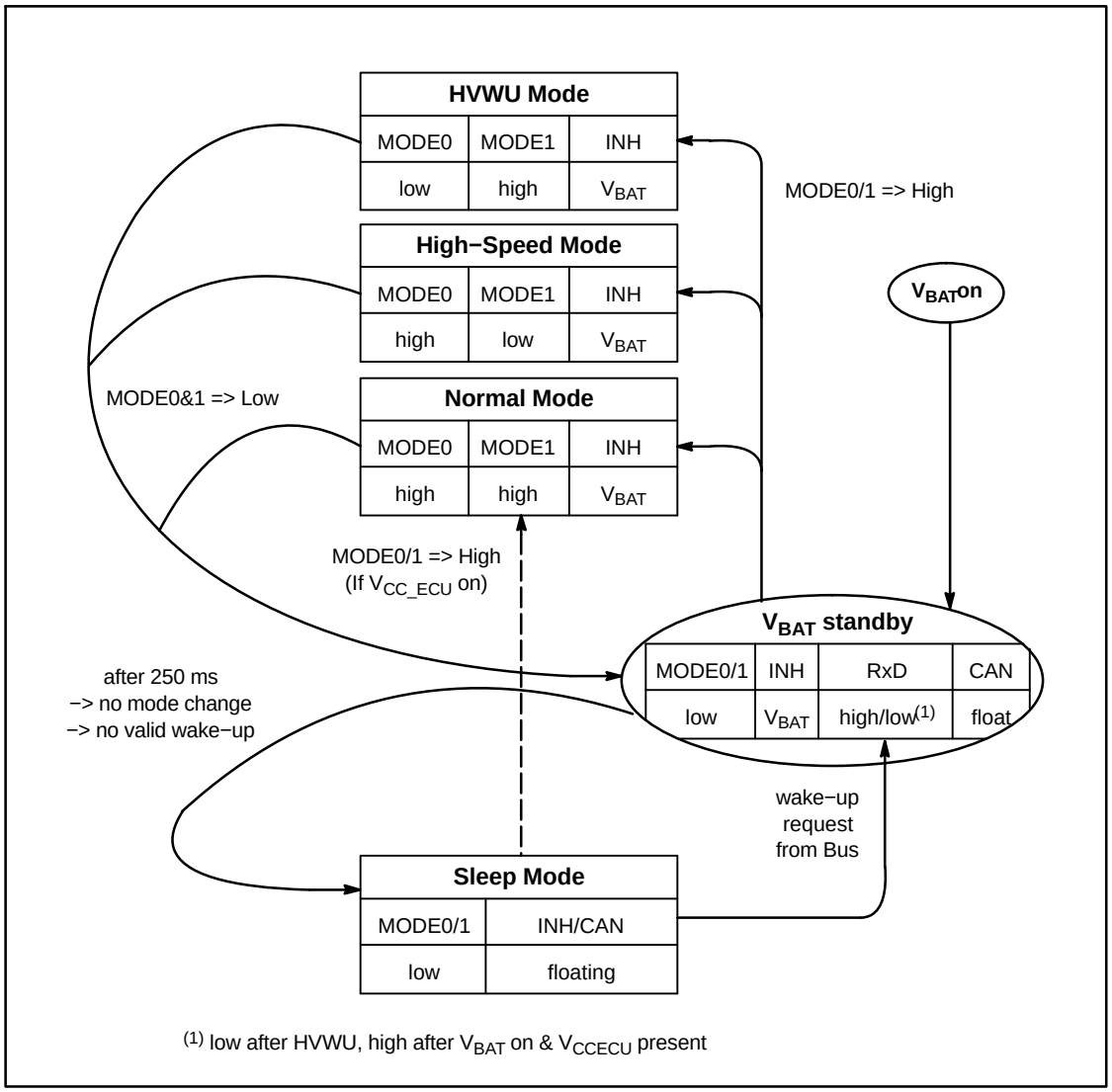
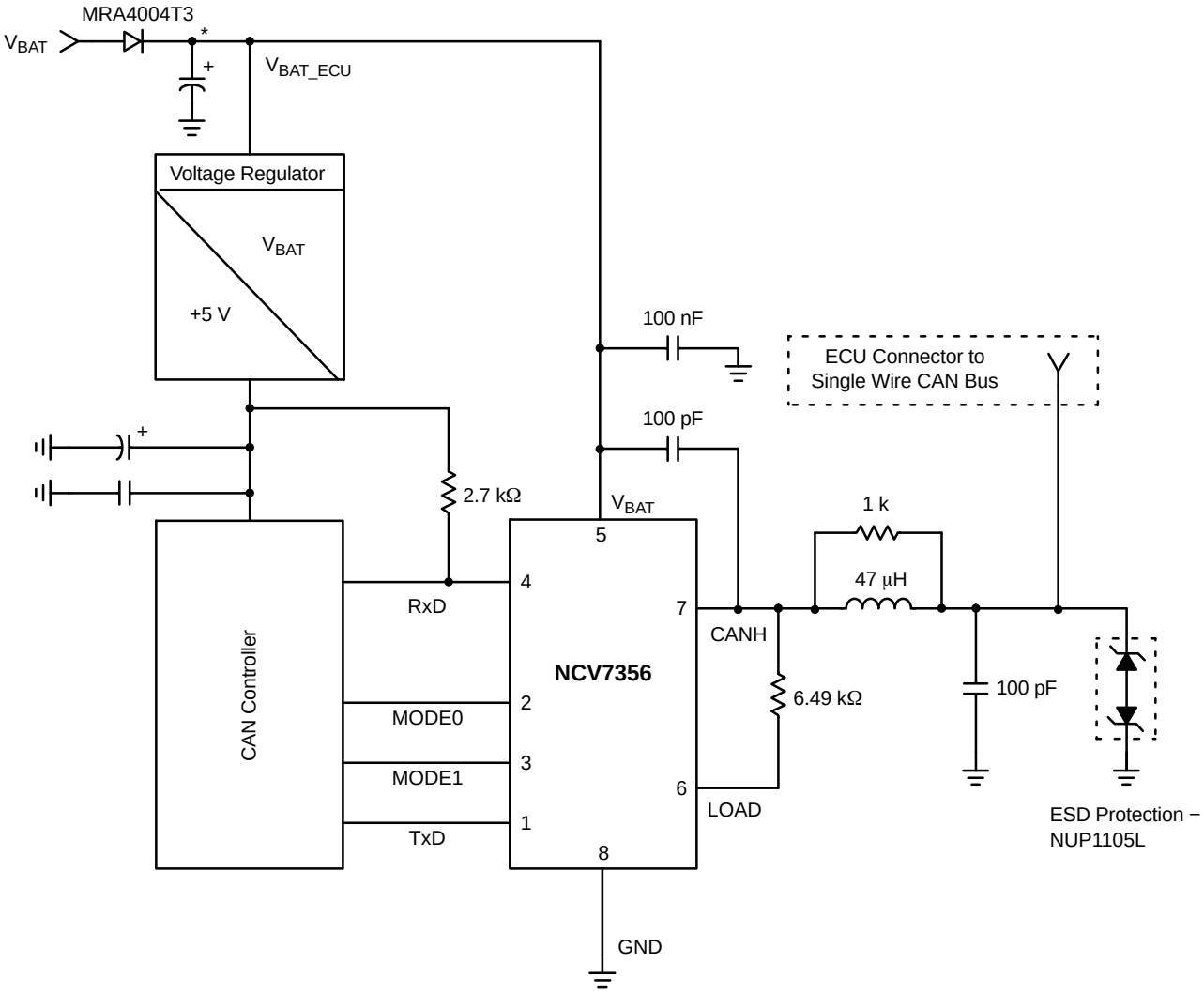
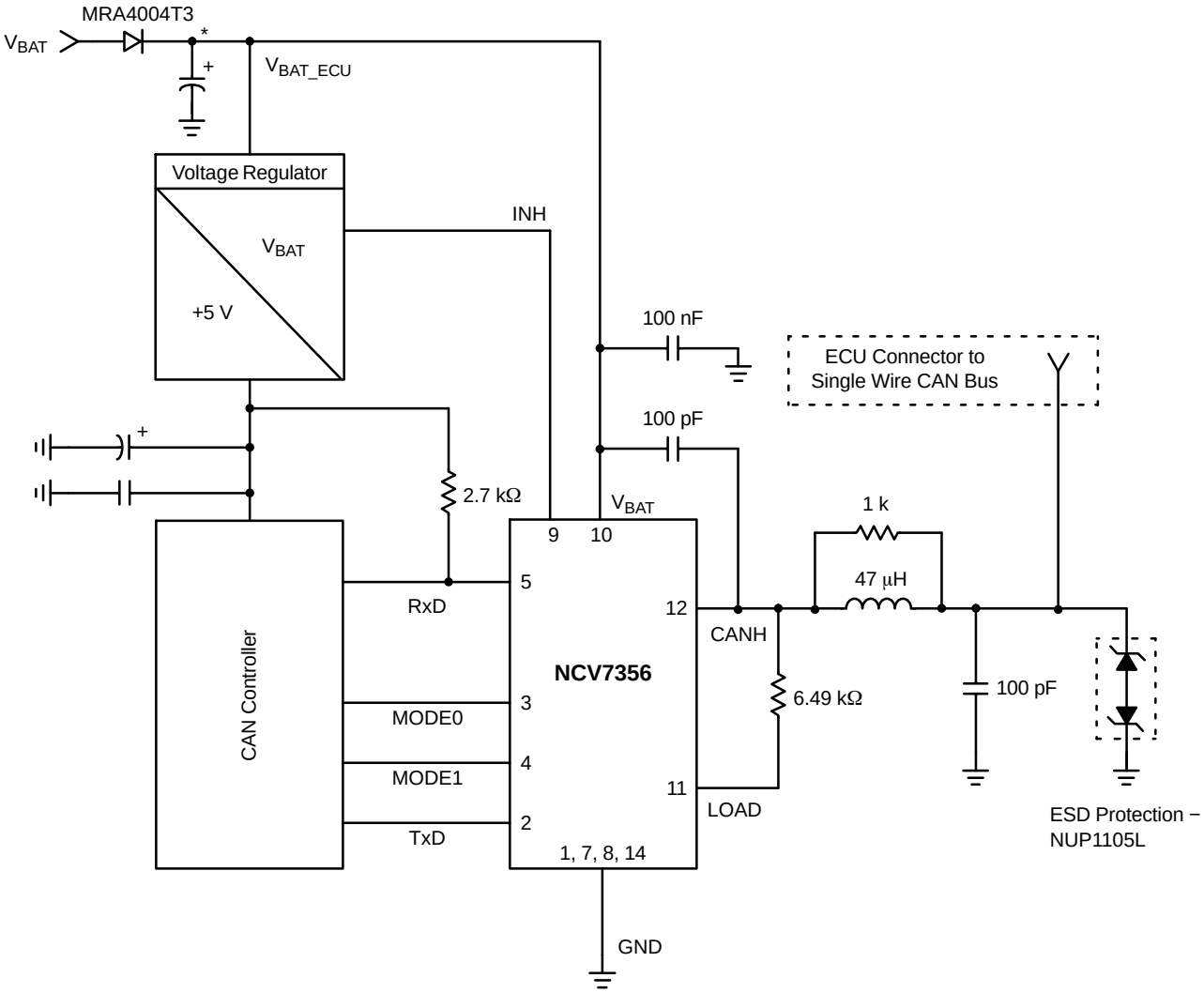


Figure 10. State Diagram, 14 Pin Package



*Recommended capacitance at V_{BAT_ECU} > 1.0 μF (immunity to ISO7637/1 test pulses)

Figure 11. Application Circuitry, 8 Pin Package



*Recommended capacitance at V_{BAT_ECU} > 1.0 μF (immunity to ISO7637/1 test pulses)

Figure 12. Application Circuitry, 14 Pin Package

SOIC−8 Thermal Information

Parameter	Test Condition, Typical Value		Unit
	Min Pad Board (Note 23)	**1″ Pad Board** (Note 24)	
Junction−to−Lead (psi−JL7, Ψ_{JL8}) or Pins 6−7	57	51	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	187	128	°C/W

23. 1 oz copper, 53 mm^2 coper area, 0.062″ thick FR4.
24. 1 oz copper, 716 mm^2 coper area, 0.062″ thick FR4.

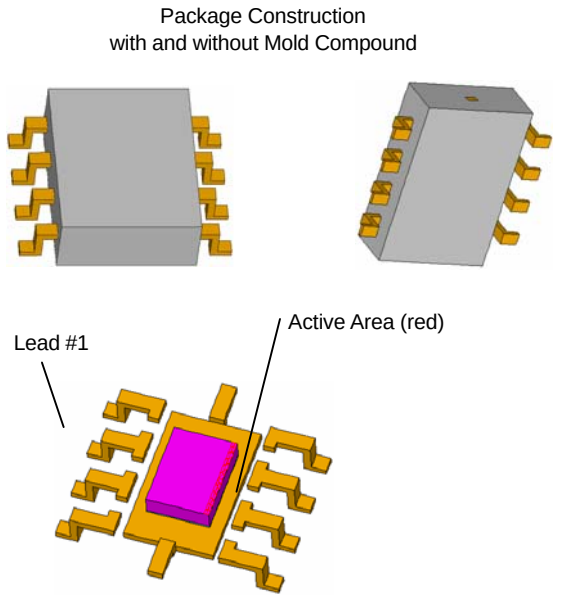


Figure 13. Internal construction of the package simulation.

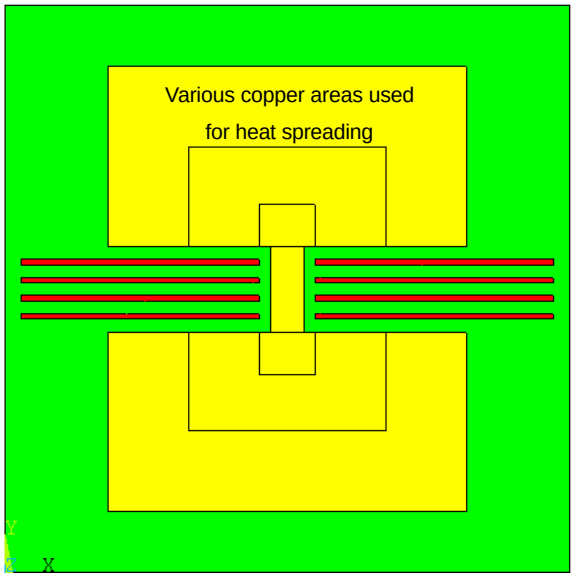


Figure 14. Min pad is shown as the red traces. 1″ pad includes the yellow area. Internal construction is shown for later reference.

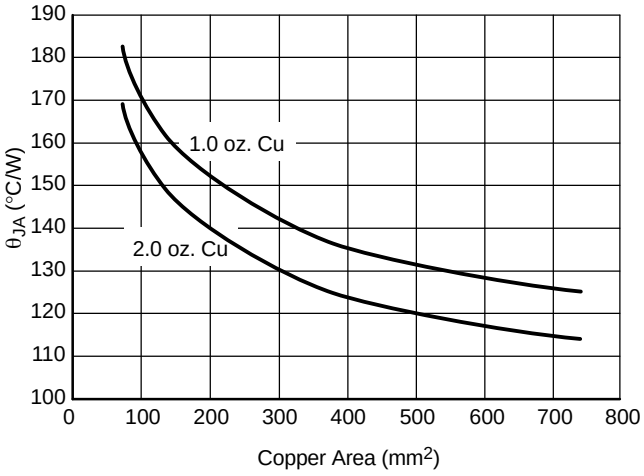


Figure 15. SOIC−8, θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

Table 1. SOIC−8 Thermal RC Network Models*

53 mm²	719 mm²	Copper Area	53 mm2	719 mm²	Copper Area
Cauer Network			Foster Network		
C's	C's	Units	Tau	Tau	Units
5.86E−06	**5.86E−06**	W−s/C	1.00E−06	1.00E−06	sec
2.29E−05	**2.29E−05**	W−s/C	1.00E−05	1.00E−05	sec
6.98E−05	**6.97E−05**	W−s/C	1.00E−04	1.00E−04	sec
3.68E−04	**3.68E−04**	W−s/C	1.99E−04	1.99E−04	sec
3.75E−04	**3.74E−04**	W−s/C	1.00E−03	1.00E−03	sec
1.57E−03	**1.56E−03**	W−s/C	1.64E−02	1.64E−02	sec
2.05E−02	**2.24E−02**	W−s/C	5.60E−01	5.60E−01	sec
9.13E−02	7.35E−02	W−s/C	4.50E+00	4.50E+00	sec
2.64E−01	1.22E+00	W−s/C	7.61E+01	7.61E+01	sec
1.66E+01	9.74E+00	W−s/C	3.00E+01	3.00E+01	sec
R's	R's		R's	R's	
0.22	**0.22**	C/W	1.30E−01	1.30E−01	C/W
0.50	**0.50**	C/W	2.82E−01	2.82E−01	C/W
1.30	**1.30**	C/W	8.91E−01	8.91E−01	C/W
1.80	**1.79**	C/W	0.17	0.18	C/W
0.95	**0.96**	C/W	1.88	1.88	C/W
7.43	**7.37**	C/W	7.15	7.24	C/W
31.19	**31.59**	C/W	19.80	16.27	C/W
59.97	47.70	C/W	30.1	54.7	C/W
75.79	28.63	C/W	14.1	23.3	C/W
4.41	6.15	C/W	109.0	21.3	C/W

*Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 130 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Both Foster and Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

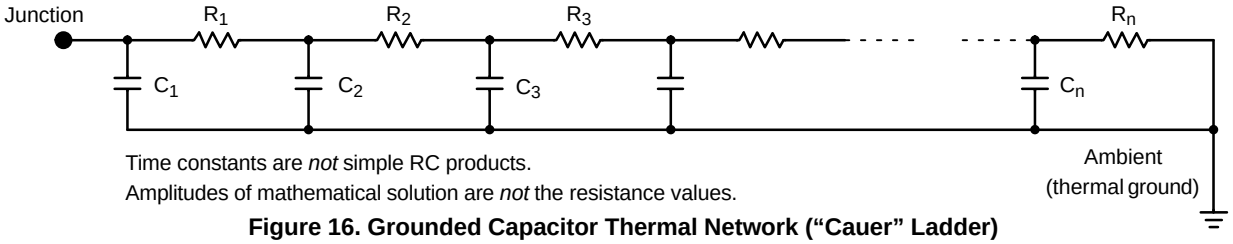


Figure 16. Grounded Capacitor Thermal Network (“Cauer” Ladder)

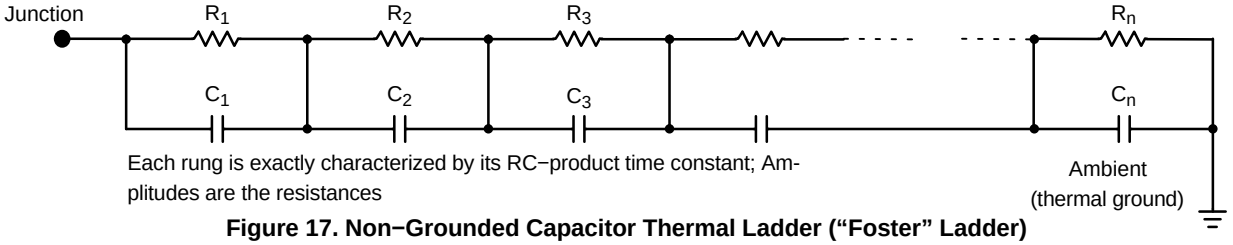


Figure 17. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

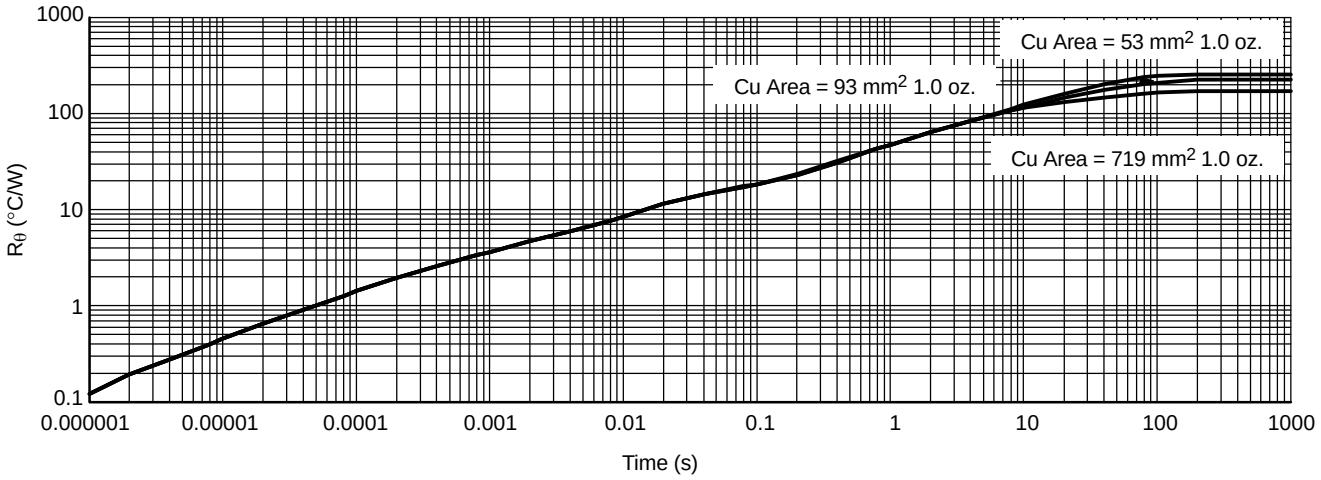


Figure 18. SOIC−8 Single Pulse Heating Curve

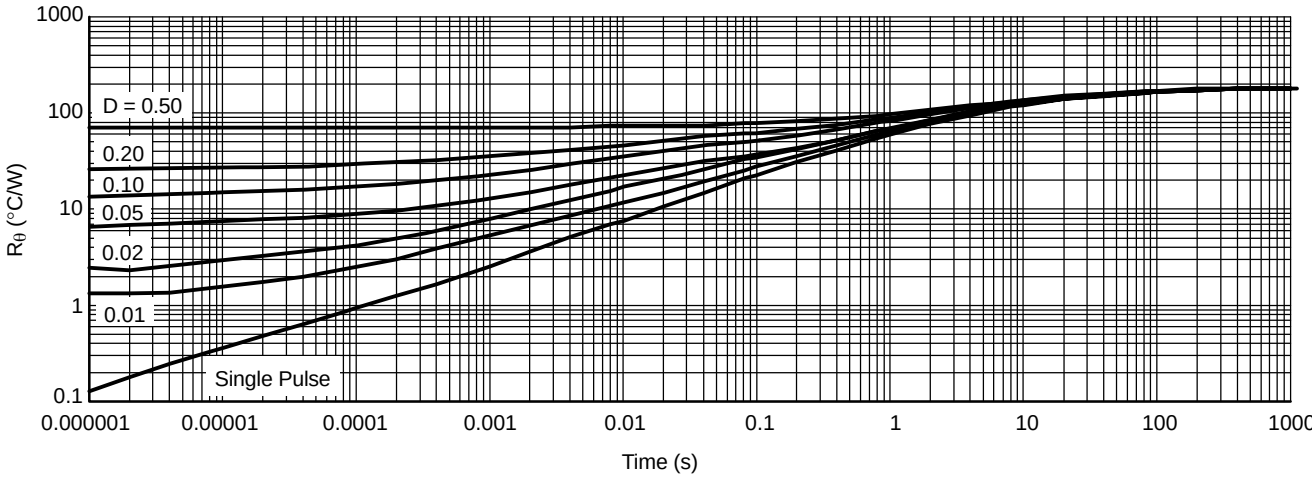


Figure 19. SOIC−8 Thermal Duty Cycle Curves on 1″ Spreader Test Board

SOIC−14 Thermal Information

Parameter	Test Condition, Typical Value		Unit
	Min Pad Board (Note 25)	1″ Pad Board (Note 26)	
Junction−to−Lead (psi−JL8, Ψ_{JL8})	30	30	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	122	84	°C/W

25. 1 oz copper, 94 mm^2 coper area, 0.062″ thick FR4.
26. 1 oz copper, 767 mm^2 coper area, 0.062″ thick FR4.

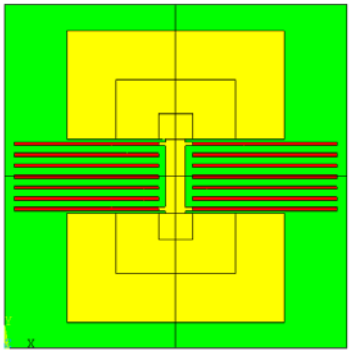


Figure 21. Min pad is shown as the red traces. 1 inch pad includes the yellow area. Pin 1, 7, 8 and 14 are connected to flag internally to the package and externally to the heat spreading area.

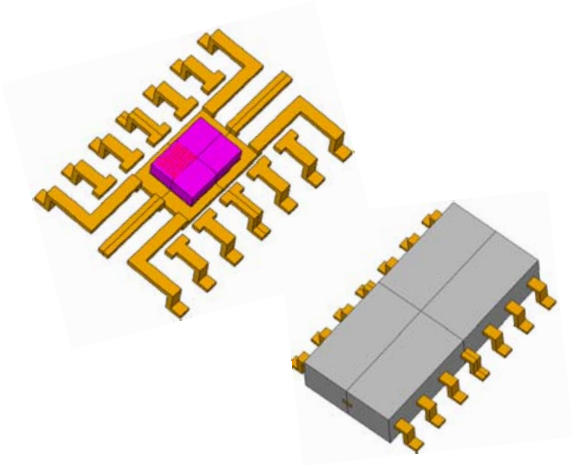


Figure 20. Internal construction of the package simulation.

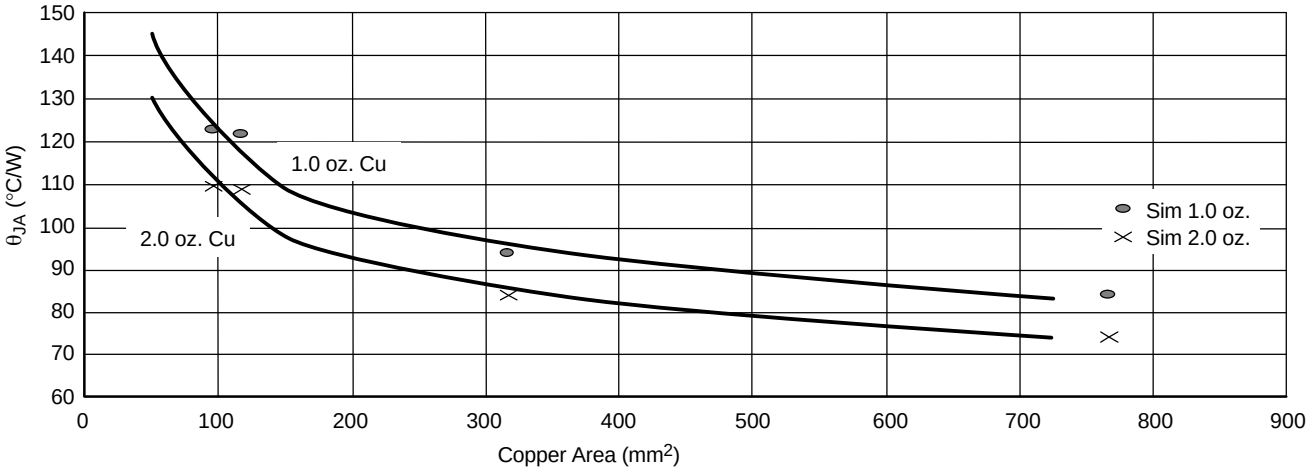


Figure 22. SOIC−14, θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

Table 2. SOIC−14 Thermal RC Network Models*

96 mm²	767 mm²	Copper Area	96 mm²	767 mm²	Copper Area
Cauer Network			Foster Network		
C's	C's	Units	Tau	Tau	Units
3.12E−05	**3.12E−05**	W−s/C	**1.00E−06**	**1.00E−06**	sec
1.21E−04	**1.21E−04**	W−s/C	**1.00E−05**	**1.00E−05**	sec
3.53E−04	**3.50E−04**	W−s/C	**1.00E−04**	**1.00E−04**	sec
1.19E−03	**1.19E−03**	W−s/C	0.028	0.001	sec
4.86E−03	**5.05E−03**	W−s/C	0.001	0.009	sec
2.17E−02	**7.16E−03**	W−s/C	0.280	0.047	sec
8.94E−02	**3.51E−02**	W−s/C	2.016	0.875	sec
0.304	0.262	W−s/C	16.64	7.53	sec
1.71	2.43	W−s/C	59.47	68.4	sec
	411	W−s/C		92.221	sec
R's	**R's**		**R's**	**R's**	
0.041	**0.041**	°C/W	**2.44E−02**	**2.44E−02**	°C/W
0.095	**0.096**	°C/W	**5.28E−02**	**5.28E−02**	°C/W
0.279	**0.281**	°C/W	**1.67E−01**	**1.67E−01**	°C/W
1.154	**0.995**	°C/W	3.5	0.7	°C/W
5.621	**6.351**	°C/W	0.7	0.1	°C/W
13.180	**1.910**	°C/W	8.7	5.8	°C/W
23.823	**21.397**	°C/W	15.9	16.4	°C/W
53.332	27.150	°C/W	31.9	27.1	°C/W
24.794	25.276	°C/W	61.3	29.0	°C/W
	0.218	°C/W		4.3	°C/W

*Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 24.4 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Both Foster and Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

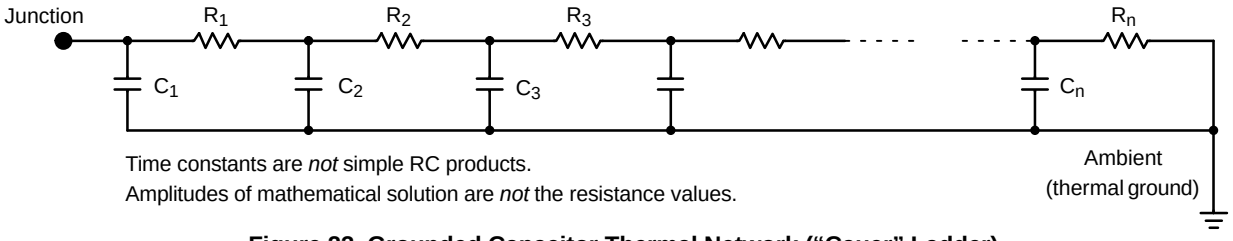


Figure 23. Grounded Capacitor Thermal Network ("Cauer" Ladder)

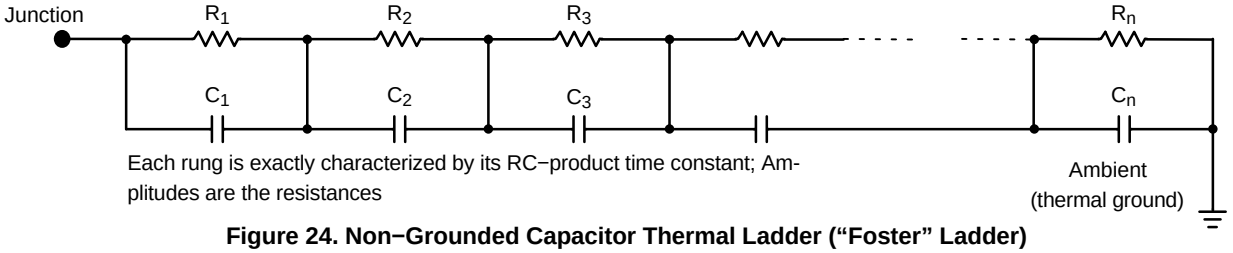


Figure 24. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)

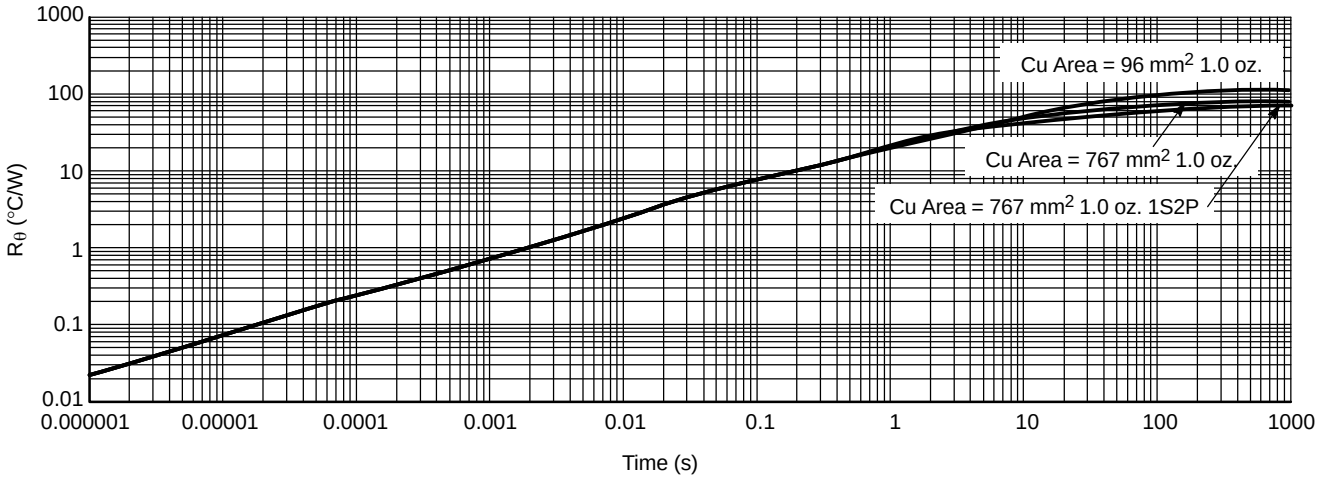


Figure 25. SOIC−14 Single Pulse Heating

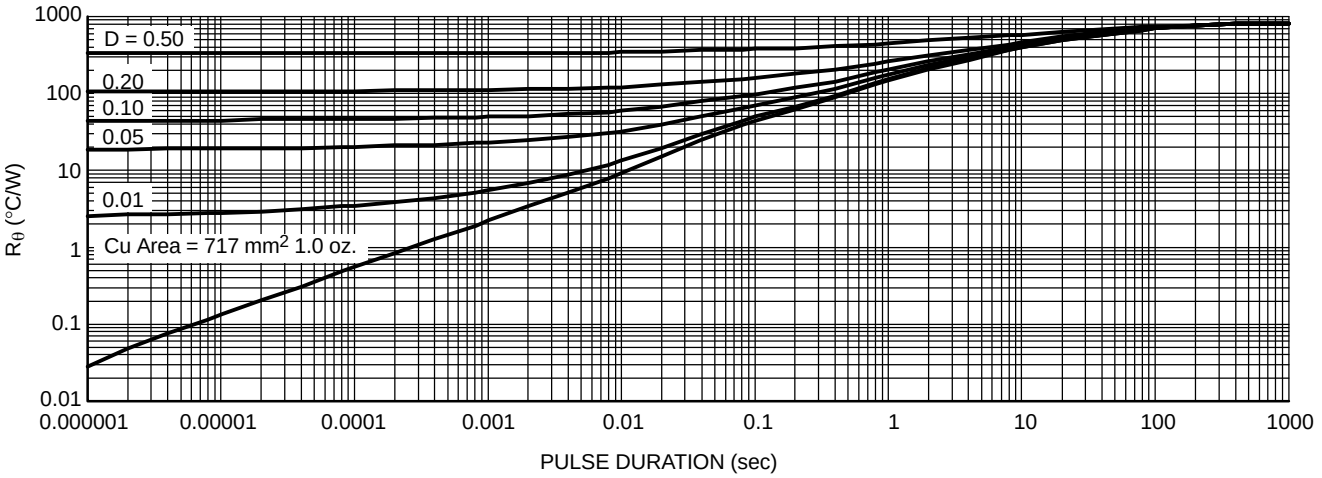
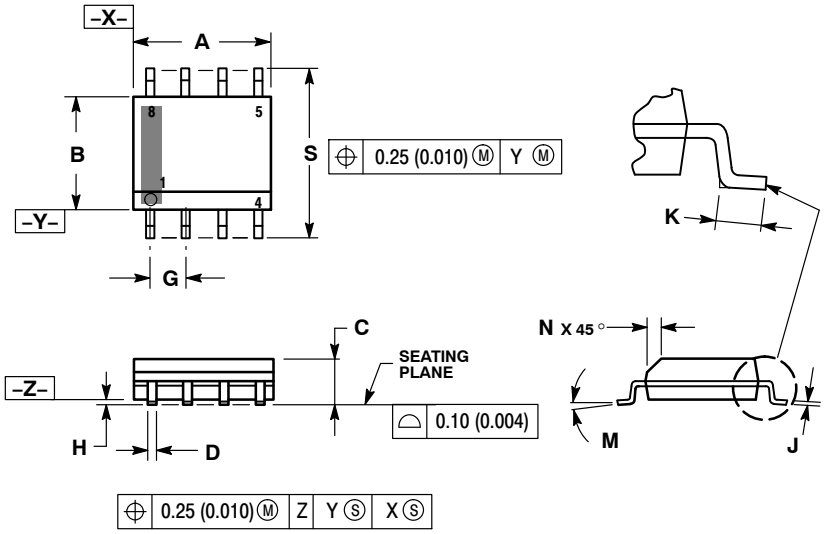


Figure 26. SOIC−14 Thermal Duty Cycle Curves on 1″ Spreader Test Board

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

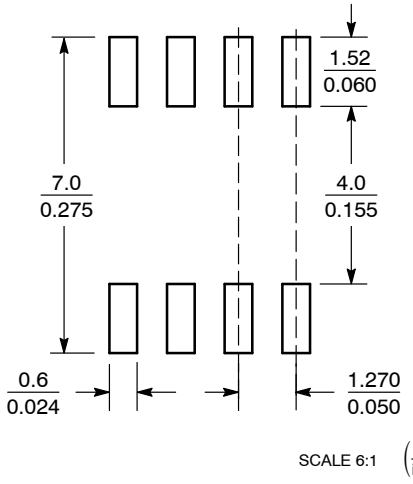
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

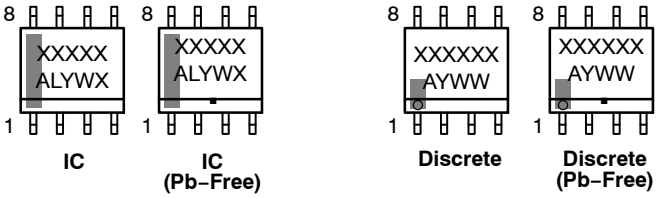
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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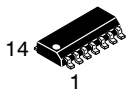
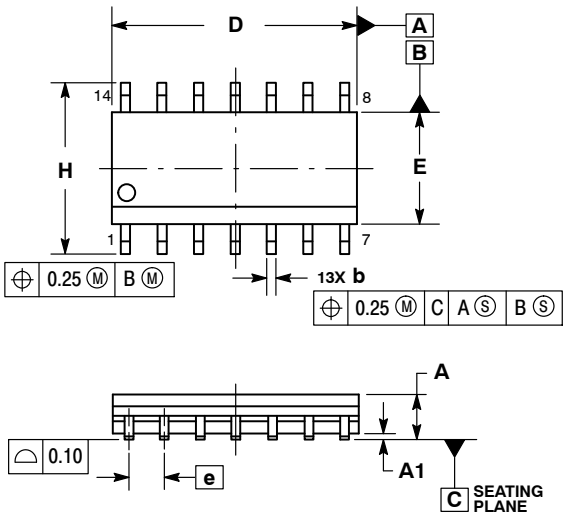
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

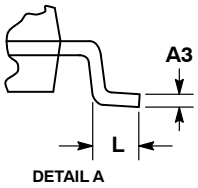


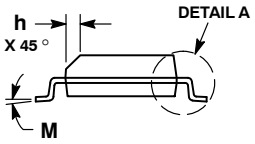
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



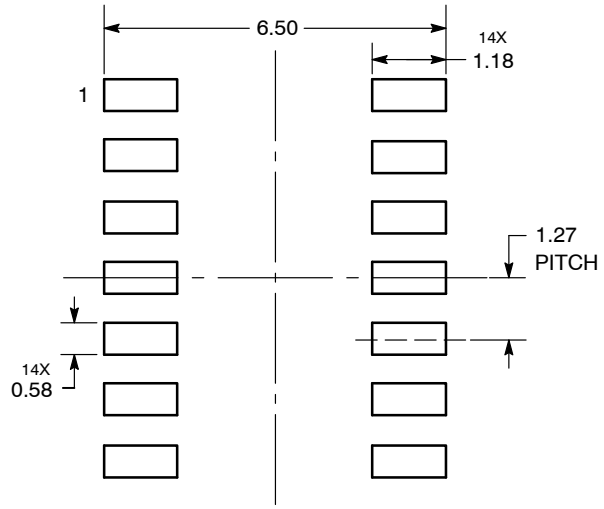




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

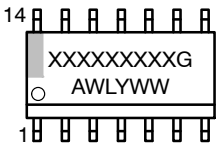
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

ADDITIONAL INFORMATION

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