# LP38842-ADJ 1.5A Ultra Low Dropout Adjustable Linear Regulators
## *Stable with Ceramic Output Capacitors*

**Check for Samples: LP38842-ADJ**

## FEATURES

- **Ideal for Conversion From 1.8V or 1.5V Inputs**
- **Designed for Use With Low ESR Ceramic Capacitors**
- **Ultra Low Dropout Voltage (115mV at 1.5A typ)**
- **0.56V to 1.5V Adjustable Output Range**
- **Load Regulation of 0.1%/A (typ)**
- **30nA Quiescent Current in Shutdown (typ)**
- **Low Ground Pin Current at all Loads**
- **Over Temperature/Over Current Protection**
- **Available in 8 Lead SO PowerPAD Package**
- **−40°C to +125°C Junction Temperature Range**
- **UVLO Disables Output When $V_{BIAS}$ < 3.8V**

## APPLICATIONS

- **ASIC Power Supplies In:**
  - **Desktops, Notebooks, and Graphics Cards, Servers**
  - **Gaming Set Top Boxes, Printers and Copiers**
- **Server Core and I/O Supplies**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulators**

## DESCRIPTION

The LP38842-ADJ is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in the SO PowerPAD package.

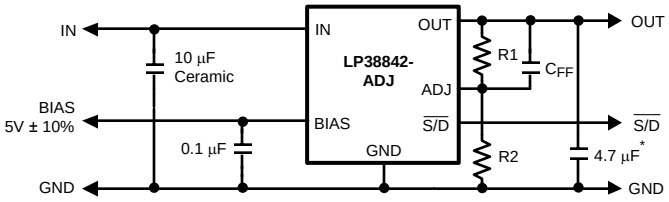
**Dropout Voltage:** 115 mV (typ) at 1.5A load current.

**Quiescent Current:** 30 mA (typ) at full load.

**Shutdown Current:** 30 nA (typ) when S/D pin is low.

**Precision Reference Voltage:** 1.5% room temperature accuracy.

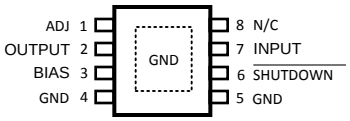
## TYPICAL APPLICATION CIRCUIT




* Minimum value required if Tantalum capacitor is used (see Application Hints).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## CONNECTION DIAGRAM

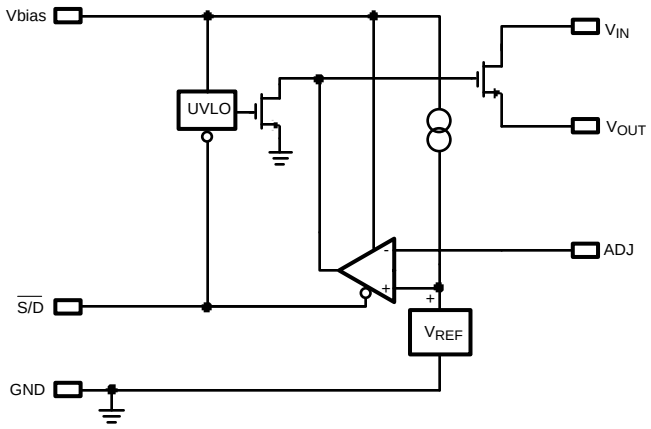



**SO PowerPAD-8, Top View**

### PIN DESCRIPTION

| Pin Name | Description |
|---|---|
| BIAS | The bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET. |
| OUTPUT | The regulated output voltage is connected to this pin. |
| GND | This is both the power and analog ground for the IC. Note that both pin three and the tab of the TO-220 and TO-263 packages are at ground potential. Pin three and the tab should be tied together using the PC board copper trace material and connected to circuit ground. |
| INPUT | The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage. |
| SHUTDOWN | This provides a low power shutdown function which turns the regulated output OFF. Tie to $V_{BIAS}$ if this function is not used. |
| ADJ | The adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see TYPICAL APPLICATION CIRCUIT). |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (1)

**If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 5 seconds) | 260°C |
| ESD Rating<br>Human Body Model (2)<br>Machine Model (3) | <br>2 kV<br>200V |
| Power Dissipation (4) | Internally Limited |
| $V_{IN}$ Supply Voltage (Survival) | −0.3V to +6V |
| $V_{BIAS}$ Supply Voltage (Survival) | −0.3V to +7V |
| Shutdown Input Voltage (Survival) | −0.3V to +7V |
| $V_{ADJ}$ | -0.3V to +6V |
| $I_{OUT}$ (Survival) | Internally Limited |
| Output Voltage (Survival) | −0.3V to +6V |
| Junction Temperature | −40°C to +150°C |

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but **do not** ensure specific performance limits. For specifications, see ELECTRICAL CHARACTERISTICS(). Specifications do not apply when operating the device outside of its rated operating conditions.
(2) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
(3) The machine model is a 220 pF capacitor discharged directly into each pin.
(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

## Operating Ratings

| | |
|---|---|
| $V_{IN}$ Supply Voltage | ($V_{OUT}$ + $V_{DO}$) to 5.5V |
| Shutdown Input Voltage | 0 to +5.5V |
| $I_{OUT}$ | 1.5A |
| Operating Junction Temperature Range | −40°C to +125°C |
| $V_{BIAS}$ Supply Voltage | 4.5V to 5.5V |
| $V_{OUT}$ | 0.56V to 1.5V |

## ELECTRICAL CHARACTERISTICS(1)

Limits in standard typeface are for $T_J$ = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN}$ = $V_O$(NOM) + 1V, $V_{BIAS}$ = 4.5V, $I_L$ = 10 mA, $C_{IN}$ = 10 µF CER, $C_{OUT}$ = 22 µF CER, $V_{S/D}$ = $V_{BIAS}$. Min/Max limits are specified through testing, statistical correlation, or design.

| Symbol | Parameter | Conditions | MIN | TYP (2) | MAX | Units |
|---|---|---|---|---|---|---|
| $V_{ADJ}$ | Adjust Pin Voltage | 10 mA < $I_L$ < 1.5A<br>$V_O$(NOM) + 1V ≤ $V_{IN}$ ≤ 5.5V<br>4.5V ≤ $V_{BIAS}$ ≤ 5.5V | 0.552<br>**0.543** | 0.56 | 0.568<br>**0.577** | V |
| $I_{ADJ}$ | Adjust Pin Bias Current | 10 mA < $I_L$ < 1.5A<br>$V_O$(NOM) + 1V ≤ $V_{IN}$ ≤ 5.5V<br>4.5V ≤ $V_{BIAS}$ ≤ 5.5V | | 1 | | µA |
| $\Delta V_O/\Delta V_{IN}$ | Output Voltage Line Regulation (3) | $V_O$(NOM) + 1V ≤ $V_{IN}$ ≤ 5.5V | | 0.01 | | %/V |
| $\Delta V_O/\Delta I_L$ | Output Voltage Load Regulation (4) | 10 mA < $I_L$ < 1.5A | | 0.1 | 0.4<br>**1.1** | %/A |
| $V_{DO}$ | Dropout Voltage (5) | $I_L$ = 1.5A | | 115 | 175<br>**315** | mV |
| $I_Q(V_{IN})$ | Quiescent Current Drawn from $V_{IN}$ Supply | 10 mA < $I_L$ < 1.5A | | 30 | 35<br>**40** | mA |
| | | $V_{\overline{S/D}}$ ≤ 0.3V | | 0.06 | 1<br>**30** | µA |
| $I_Q(V_{BIAS})$ | Quiescent Current Drawn from $V_{BIAS}$ Supply | 10 mA < $I_L$ < 1.5A | | 2 | 4<br>**6** | mA |
| | | $V_{\overline{S/D}}$ ≤ 0.3V | | 0.03 | 1<br>**30** | µA |
| UVLO | $V_{BIAS}$ Voltage Where Regulator Output Is Enabled | | | 3.8 | | V |
| $I_{SC}$ | Short-Circuit Current | $V_{OUT}$ = 0V | | 4 | | A |
| **Shutdown Input** | | | | | | |
| $V_{SDT}$ | Output Turn-off Threshold | Output = ON | | 0.7 | **1.3** | V |
| | | Output = OFF | **0.3** | 0.7 | | |
| Td (OFF) | Turn-OFF Delay | $R_{LOAD}$ X $C_{OUT}$ << Td (OFF) | | 20 | | µs |
| Td (ON) | Turn-ON Delay | $R_{LOAD}$ X $C_{OUT}$ << Td (ON) | | 15 | | |
| $I_{\overline{S/D}}$ | $\overline{S/D}$ Input Current | $V_{\overline{S/D}}$ =1.3V | | 1 | | µA |
| | | $V_{\overline{S/D}}$ ≤ 0.3V | | −1 | | |
| $\theta_{J-A}$ | Junction to Ambient Thermal Resistance | SO PowerPAD-8 Package (6) | | 43 | | °C/W |
| **AC Parameters** | | | | | | |
| PSRR ($V_{IN}$) | Ripple Rejection for $V_{IN}$ Input Voltage | $V_{IN}$ = $V_{OUT}$ +1V, f = 120 Hz | | 80 | | dB |
| | | $V_{IN}$ = $V_{OUT}$ + 1V, f = 1 kHz | | 65 | | |
| PSRR ($V_{BIAS}$) | Ripple Rejection for $V_{BIAS}$ Voltage | $V_{BIAS}$ = $V_{OUT}$ + 3V, f = 120 Hz | | 58 | | |
| | | $V_{BIAS}$ = $V_{OUT}$ + 3V, f = 1 kHz | | 58 | | |
| | Output Noise Density | f = 120 Hz | | 1 | | µV/root−Hz |
| $e_n$ | Output Noise Voltage<br>$V_{OUT}$ = 1.5V | BW = 10 Hz − 100 kHz | | 150 | | µV (rms) |
| | | BW = 300 Hz − 300 kHz | | 90 | | |

(1) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.
(2) Typical numbers represent the most likely parametric norm for 25°C operation.
(3) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(4) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(5) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.
(6) For optimum heat dissipation, the ground pad must be soldered to a copper plane or connected using vias to an internal copper plane.

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_J$ = 25°C, $C_{IN}$ = 10 µF CER, $C_{OUT}$ = 22 µF CER, $C_{BIAS}$ = 1 µF CER, $\overline{S/D}$ Pin is tied to $V_{BIAS}$, $V_{OUT}$ = 1.2V, $I_L$ = 10mA, $V_{BIAS}$ = 5V, $V_{IN}$ = $V_{OUT}$ + 1V.

**$V_{BIAS}$ Transient Response**

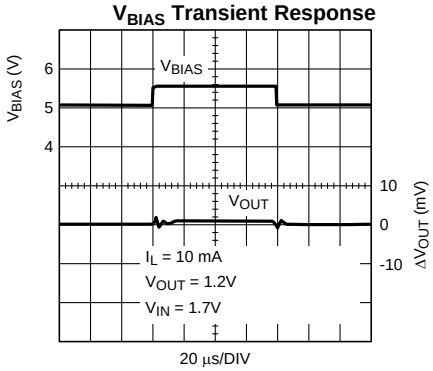



**Figure 1.**

**Load Transient Response**

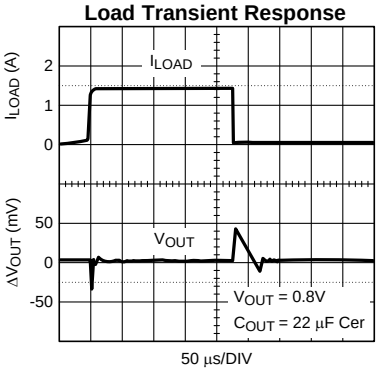



**Figure 2.**

**Load Transient Response**

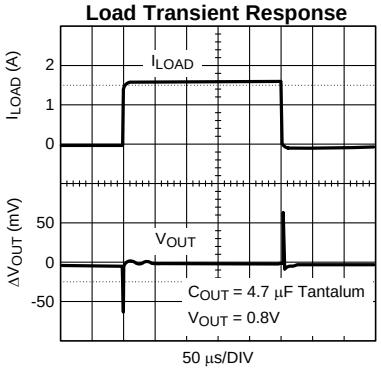



**Figure 3.**

**Dropout Voltage Over Temperature**

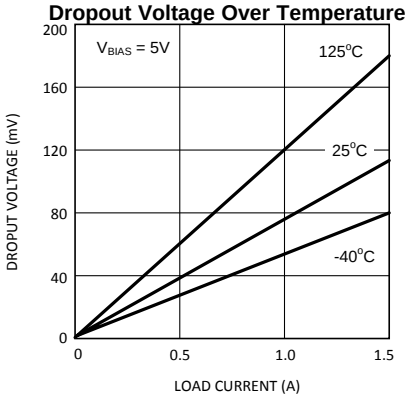



**Figure 4.**

**$V_{BIAS}$ PSRR**

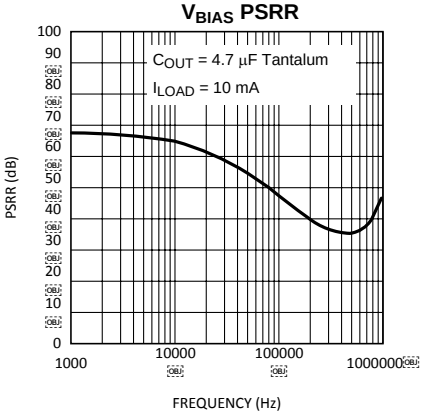



**Figure 5.**

**$V_{BIAS}$ PSRR**

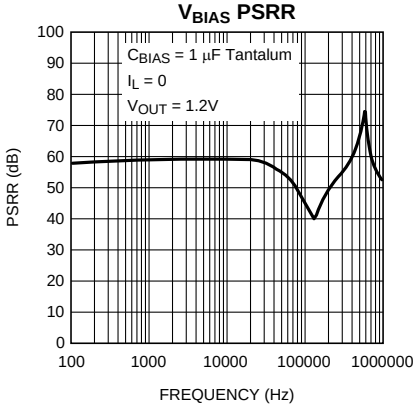



**Figure 6.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_J$ = 25°C, $C_{IN}$ = 10 µF CER, $C_{OUT}$ = 22 µF CER, $C_{BIAS}$ = 1 µF CER, $\overline{S/D}$ Pin is tied to $V_{BIAS}$, $V_{OUT}$ = 1.2V, $I_L$ = 10mA, $V_{BIAS}$ = 5V, $V_{IN}$ = $V_{OUT}$ + 1V.

**$V_{IN}$ PSRR**

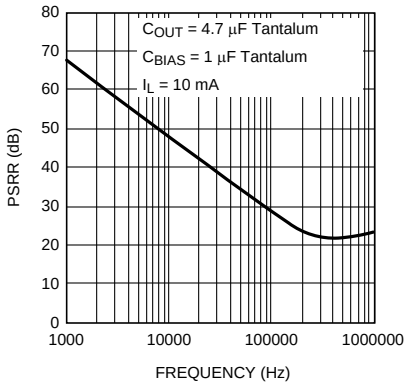



**Figure 7.**

**Output Noise Voltage**

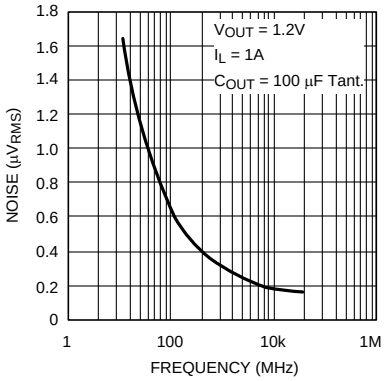



**Figure 8.**

**$V_{ADJ}$ / $I_{ADJ}$ vs Temperature**

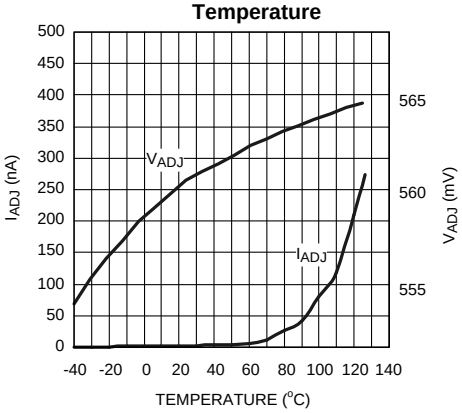



**Figure 9.**

## Application Hints

### SETTING THE OUTPUT VOLTAGE (Refer to TYPICAL APPLICATION CIRCUIT)

The output voltage is set using the resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + R1 / R2) \quad (1)$$

The value of resistor R2 must be 10k or less for proper operation.

### EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the TYPICAL APPLICATION CIRCUIT.

### OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

### INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of $C_{IN}$ may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

### FEED FORWARD CAPACITOR (Refer to TYPICAL APPLICATION CIRCUIT)

A capacitor placed across R1 can provide some additional phase margin and improve transient response. The capacitor $C_{FF}$ and R1 form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1) \quad (2)$$

For best effect, select $C_{FF}$ so the zero frequency is approximately 70 kHz. The phase lead provided by $C_{FF}$ drops as the output voltage gets closer to 0.56V (and R1 reduces in value). The reason is that $C_{FF}$ also forms a pole whose frequency is given by:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times R1 // R2) \quad (3)$$

As R1 reduces, the two equations come closer to being equal and the pole and zero begin to cancel each other out which removes the beneficial phase lead of the zero.

### BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

### BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

## UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 3.8V.

## SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. The $\overline{S/D}$ pin must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

## POWER DISSIPATION/HEATSINKING

Heatsinking for the SO PowerPAD-8 package is accomplished by allowing heat to flow through the ground slug on the bottom of the package into the copper on the PC board. The heat slug must be soldered down to a copper plane to get good heat transfer. It can also be connected through vias to internal copper planes. Since the heat slug is at ground potential, traces must not be routed under it which are not at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

## REVISION HISTORY

| Changes from Original (April 2013) to Revision A | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 8 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP38842MR-ADJ/NOPB | ACTIVE | SO PowerPAD | DDA | 8 | 95 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | -40 to 125 | L38842 MRADJ | Samples |
| LP38842MRX-ADJ/NOPB | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-3-260C-168 HR | | L38842 MRADJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

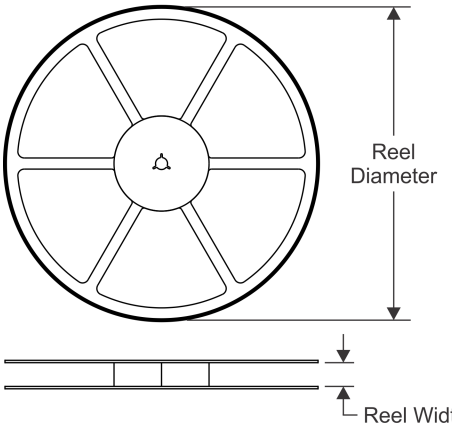
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

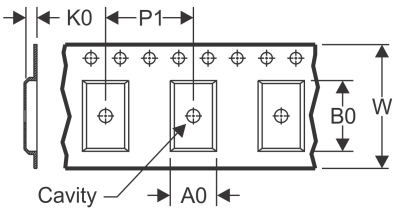
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

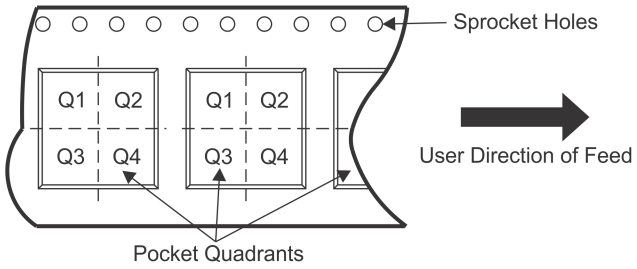



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

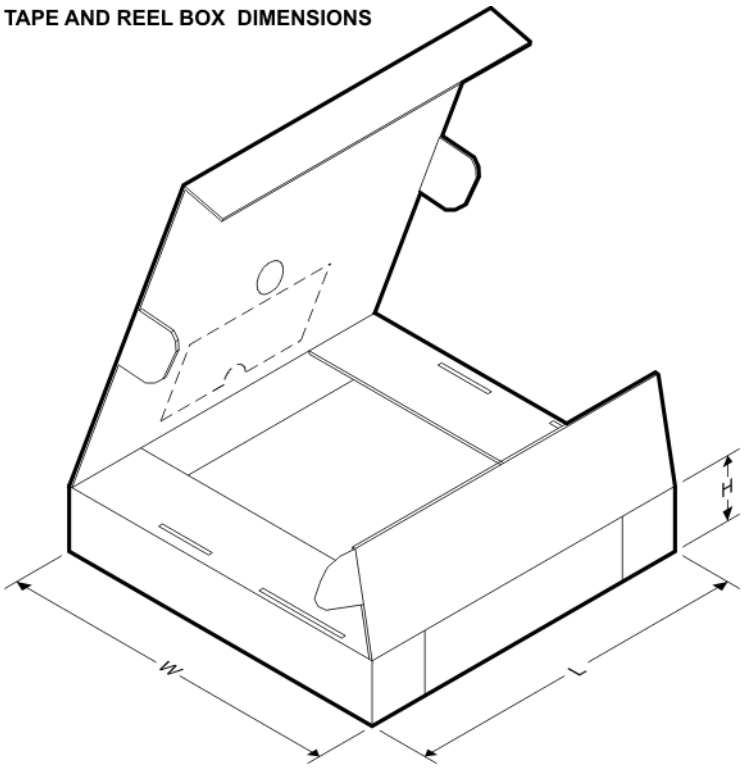
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP38842MRX-ADJ/NOPB | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

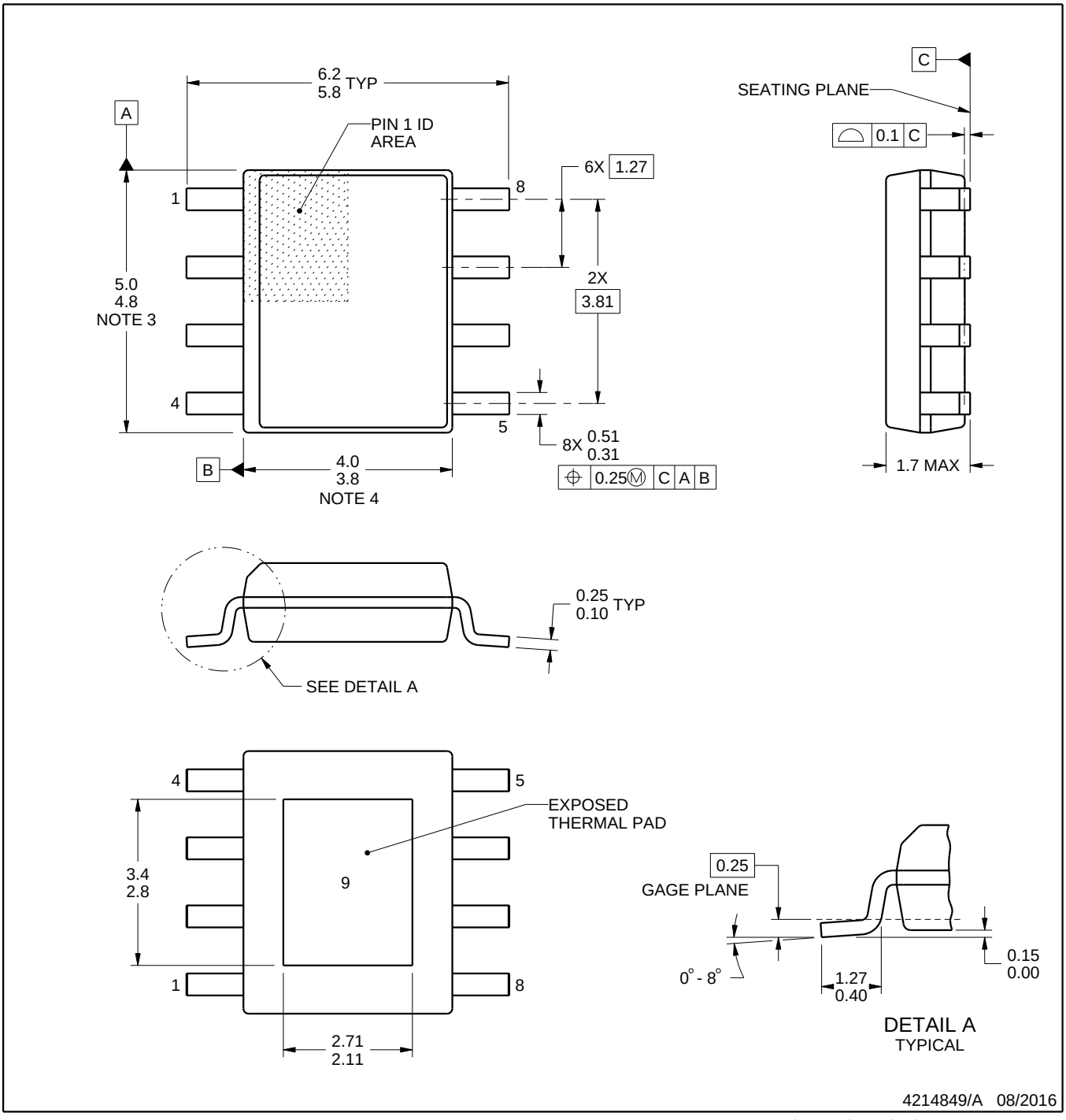
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP38842MRX-ADJ/NOPB | SO PowerPAD | DDA | 8 | 2500 | 367.0 | 367.0 | 35.0 |

# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

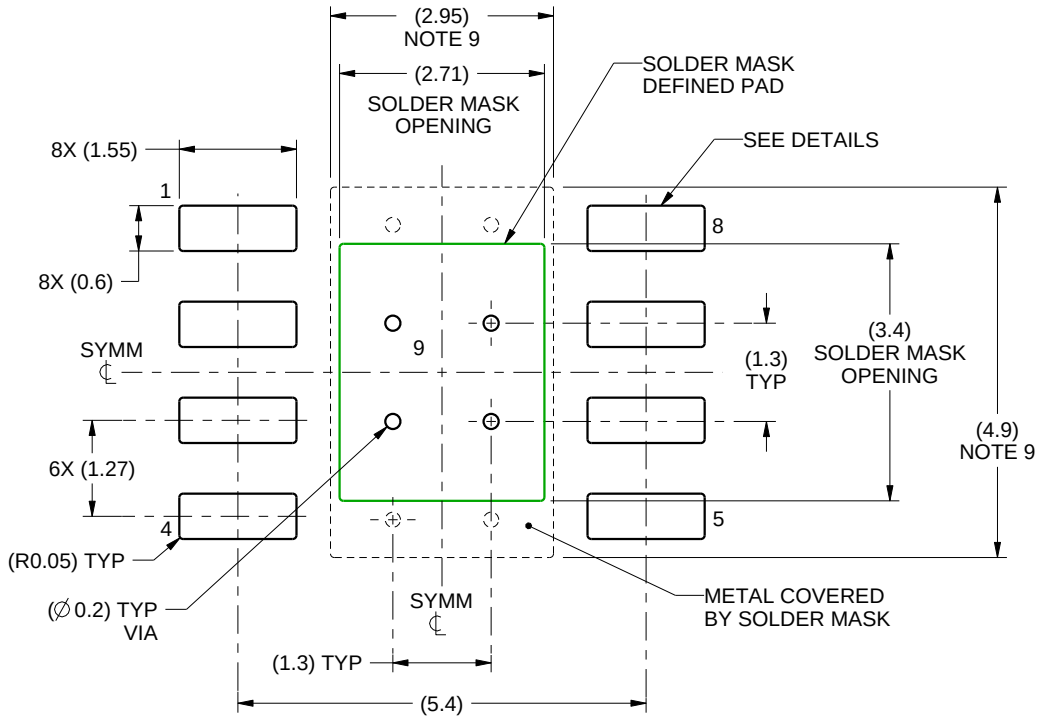
PLASTIC SMALL OUTLINE



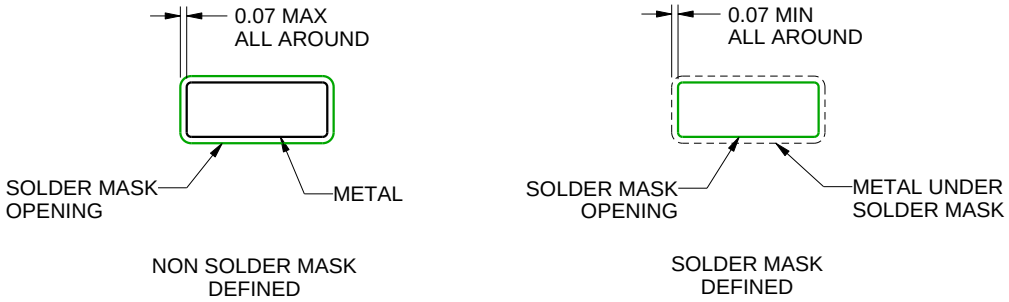

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

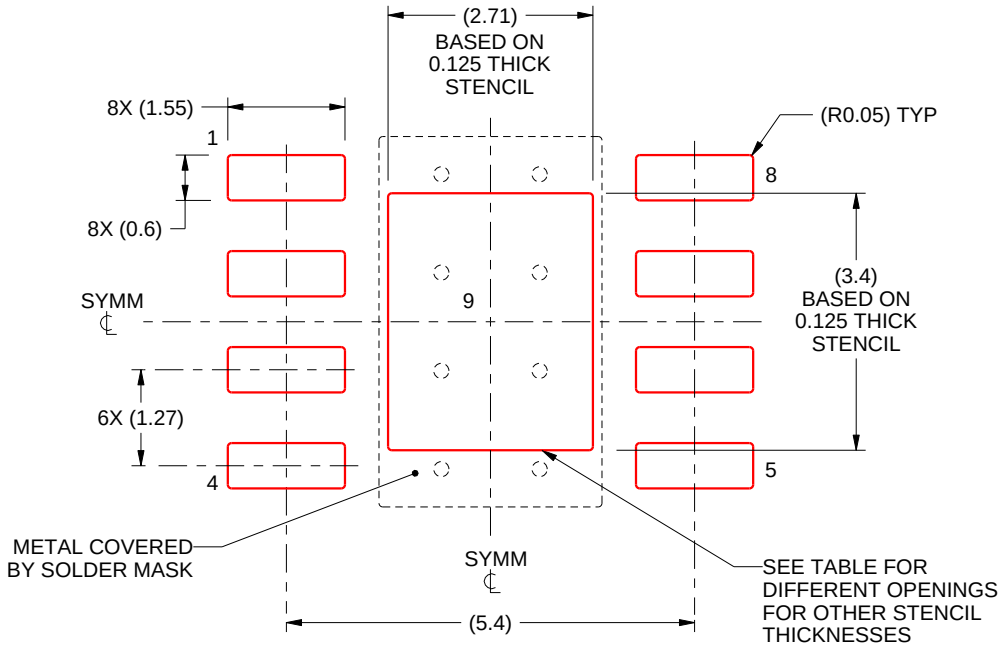
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265