



DAC7724 DAC7725

For most current data sheet and other product information, visit www.burr-brown.com

12-Bit Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER: 250mW max**
- **SINGLE SUPPLY OUTPUT RANGE: +10V**
- **DUAL SUPPLY OUTPUT RANGE: $\pm 10V$**
- **SETTLING TIME: 10 μ s to 0.012%**
- **12-BIT LINEARITY AND MONOTONICITY: $-40^{\circ}C$ to $+85^{\circ}C$**
- **RESET TO MID-SCALE (DAC7724) OR ZERO-SCALE (DAC7725)**
- **DATA READBACK**
- **DOUBLE-BUFFERED DATA INPUTS**

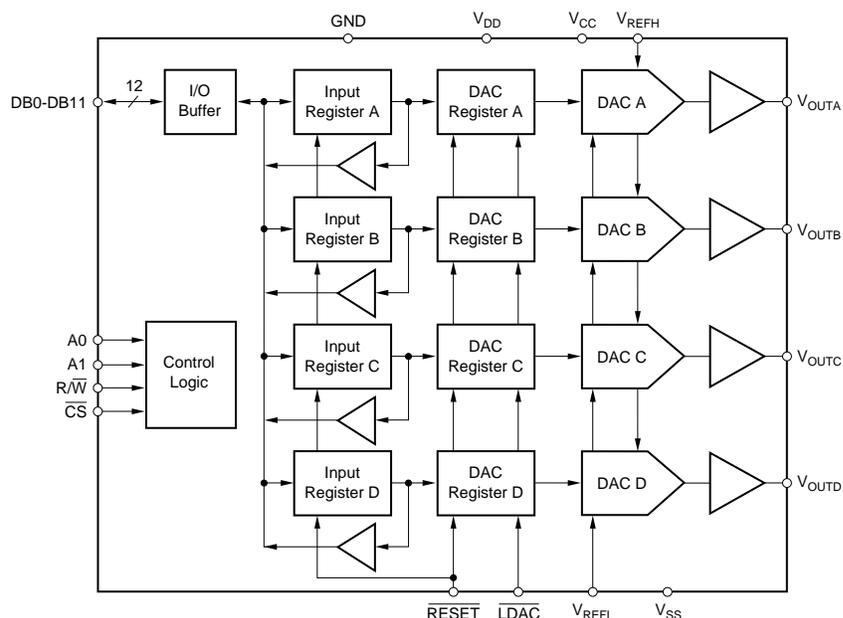
APPLICATIONS

- **PROCESS CONTROL**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**

DESCRIPTION

The DAC7724 and DAC7725 are 12-bit quad voltage output digital-to-analog converters with guaranteed 12-bit monotonic performance over the specified temperature range. They accept 12-bit parallel input data, have double-buffered DAC input logic (allowing simultaneous update of all DACs), and provide a readback mode of the internal input registers. An asynchronous reset clears all registers to a mid-scale of 800_H (DAC7724) or to a zero-scale of 000_H (DAC7725). The DAC7724 and DAC7725 can operate from a single +15V supply, or from +15V and -15V supplies.

Low power and small size per DAC make the DAC7724 and DAC7725 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7724 and DAC7725 are available in a PLCC-28 or a SO-28 package, and offer guaranteed specifications over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
 Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATION (DUAL SUPPLY)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +15\text{V}$, $V_{DD} = +5\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, $V_{REFL} = -10\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7724N, U DAC7725N, U			DAC7724NB, UB DAC7725NB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error				± 2			± 1	LSB ⁽¹⁾
Linearity Matching ⁽²⁾				± 2			± 1	LSB
Differential Linearity Error				± 1			± 1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*		*	Bits
Zero-Scale Error	Code = 000 _H			± 2			*	LSB
Zero-Scale Drift			1			*		ppm/ $^{\circ}\text{C}$
Zero-Scale Matching ⁽²⁾				± 2			± 1	LSB
Full-Scale Error	Code = FFF _H			± 2			*	LSB
Full-Scale Matching ⁽²⁾				± 2			± 1	LSB
Power Supply Sensitivity	At Full Scale		10			*		ppm/V
ANALOG OUTPUT								
Voltage Output ⁽³⁾		V_{REFL}		V_{REFH}	*		*	V
Output Current		± 5			*		*	mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			± 20			*		mA
Short-Circuit Duration	To V_{SS} , V_{CC} , or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		$V_{REFL} + 1.25$		+10	*		*	V
V_{REFL} Input Range		-10		$V_{REFH} - 1.25$	*		*	V
Ref High Input Current		-0.5		3.0	*		*	mA
Ref Low Input Current		-3.5		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time	To $\pm 0.012\%$, 20V Output Step		8	10		*	*	μs
Channel-to-Channel Crosstalk	Full-Scale Step		0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	$f = 10\text{kHz}$		65			*		nV/ $\sqrt{\text{Hz}}$
DIGITAL INPUT/OUTPUT								
Logic Family		TTL-Compatible CMOS			*			
Logic Levels								
V_{IH}	$I_{IH} \leq \pm 10\mu\text{A}$	2.4		$V_{DD} + 0.3$	*		*	V
V_{IL}	$I_{IL} \leq \pm 10\mu\text{A}$	-0.3		0.8	*		*	V
V_{OH}	$I_{OH} = -0.8\text{mA}$	3.6		V_{DD}	*		*	V
V_{OL}	$I_{OL} = 1.6\text{mA}$	0.0		0.4	*		*	V
Data Format		Straight Binary				*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		+4.75		+5.25	*		*	V
V_{CC}		+14.25		+15.75	*		*	V
V_{SS}		-14.25		-15.75	*		*	V
I_{DD}			50			*	*	μA
I_{CC}			6	8.5		*	*	mA
I_{SS}		-8	-6		*	*	*	mA
Power Dissipation			180	250		*	*	mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$

NOTES: (1) LSB means Least Significant Bit, when V_{REFH} equals +10V and V_{REFL} equals -10V, then one LSB equals 4.88mV. (2) All DAC outputs will match within the specified error band. (3) Ideal output voltage, does not take into account zero or full-scale error.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATION (SINGLE SUPPLY)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +15\text{V}$, $V_{DD} = +5\text{V}$, $V_{SS} = \text{GND}$, $V_{REFH} = +10\text{V}$, $V_{REFL} = 0\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7724N, U DAC7725N, U			DAC7724NB, UB DAC7725NB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error ⁽¹⁾				± 2			± 1	LSB ⁽²⁾
Linearity Matching ⁽³⁾				± 2			± 1	LSB
Differential Linearity Error				± 1			± 1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 004 _H			± 4			*	LSB
Zero-Scale Drift			2			*		ppm/ $^{\circ}\text{C}$
Zero-Scale Matching ⁽³⁾				± 4			± 2	LSB
Full-Scale Error	Code = FFF _H			± 4			*	LSB
Full-Scale Matching ⁽³⁾				± 4			± 2	LSB
Power Supply Sensitivity	At Full Scale		20			*		ppm/V
ANALOG OUTPUT								
Voltage Output ⁽⁴⁾		V_{REFL}		V_{REFH}	*		*	V
Output Current		± 5			*			mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			± 20			*		mA
Short-Circuit Duration	To V_{CC} or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		$V_{\text{REFL}} + 1.25$		+10	*		*	V
V_{REFL} Input Range		0		$V_{\text{REFH}} - 1.25$	*		*	V
Ref High Input Current		-0.3		1.5	*		*	mA
Ref Low Input Current		-2.0		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time ⁽⁵⁾	To $\pm 0.012\%$, 10V Output Step		8	10		*	*	μs
Channel-to-Channel Crosstalk			0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	$f = 10\text{kHz}$		65			*		$\text{nV}/\sqrt{\text{Hz}}$
DIGITAL INPUT/OUTPUT								
Logic Family		TTL-Compatible CMOS			*			
Logic Levels								
V_{IH}	$I_{\text{IH}} \leq \pm 10\mu\text{A}$	2.4		$V_{\text{DD}} + 0.3$	*		*	V
V_{IL}	$I_{\text{IL}} \leq \pm 10\mu\text{A}$	-0.3		0.8	*		*	V
V_{OH}	$I_{\text{OH}} = -0.8\text{mA}$	3.6		V_{DD}	*		*	V
V_{OL}	$I_{\text{OL}} = 1.6\text{mA}$	0.0		0.4	*		*	V
Data Format		Straight Binary				*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		+4.75		+5.25	*		*	V
V_{CC}		14.25		15.75	*		*	V
I_{DD}			50			*	*	μA
I_{CC}			3.0			*	*	mA
Power Dissipation			45			*		mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$

NOTES: (1) If $V_{SS} = 0\text{V}$, specification applies at code 004_H and above. (2) LSB means Least Significant Bit, when V_{REFH} equals +10V and V_{REFL} equals 0V, then one LSB equals 2.44mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) Full-scale positive 10V step and negative step from code FFF_H to 004_H.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC} to V_{SS}	-0.3V to +32V
V_{CC} to GND	-0.3V to +16V
V_{SS} to GND	+0.3V to -16V
V_{DD} to GND	-0.3V to 6V
V_{REFH} to GND	-9V to +11V
V_{REFL} to GND ($V_{SS} = -15V$)	-11V to +9V
V_{REFL} to GND ($V_{SS} = 0V$)	-0.3V to +9V
V_{REFH} to V_{REFL}	-1V to +22V
Digital Input Voltage to GND	-0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to GND	-0.3V to $V_{DD} + 0.3V$
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

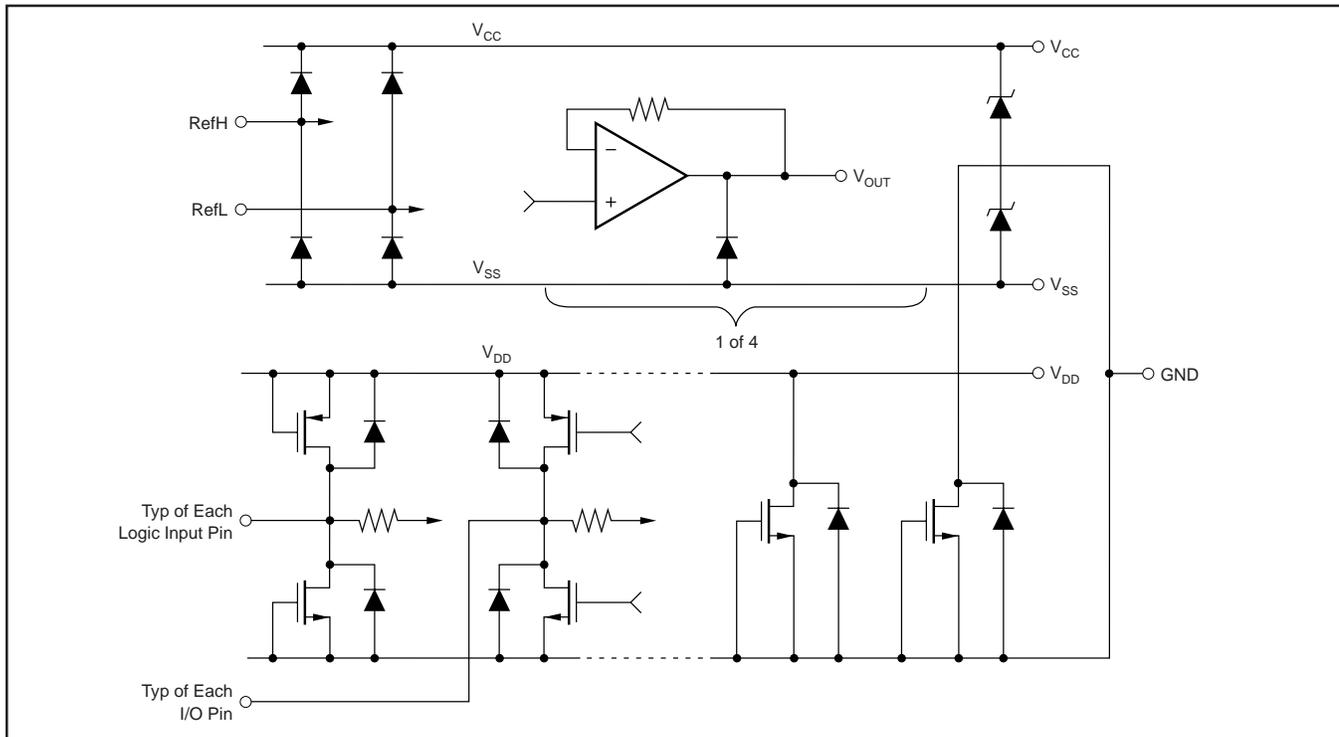
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

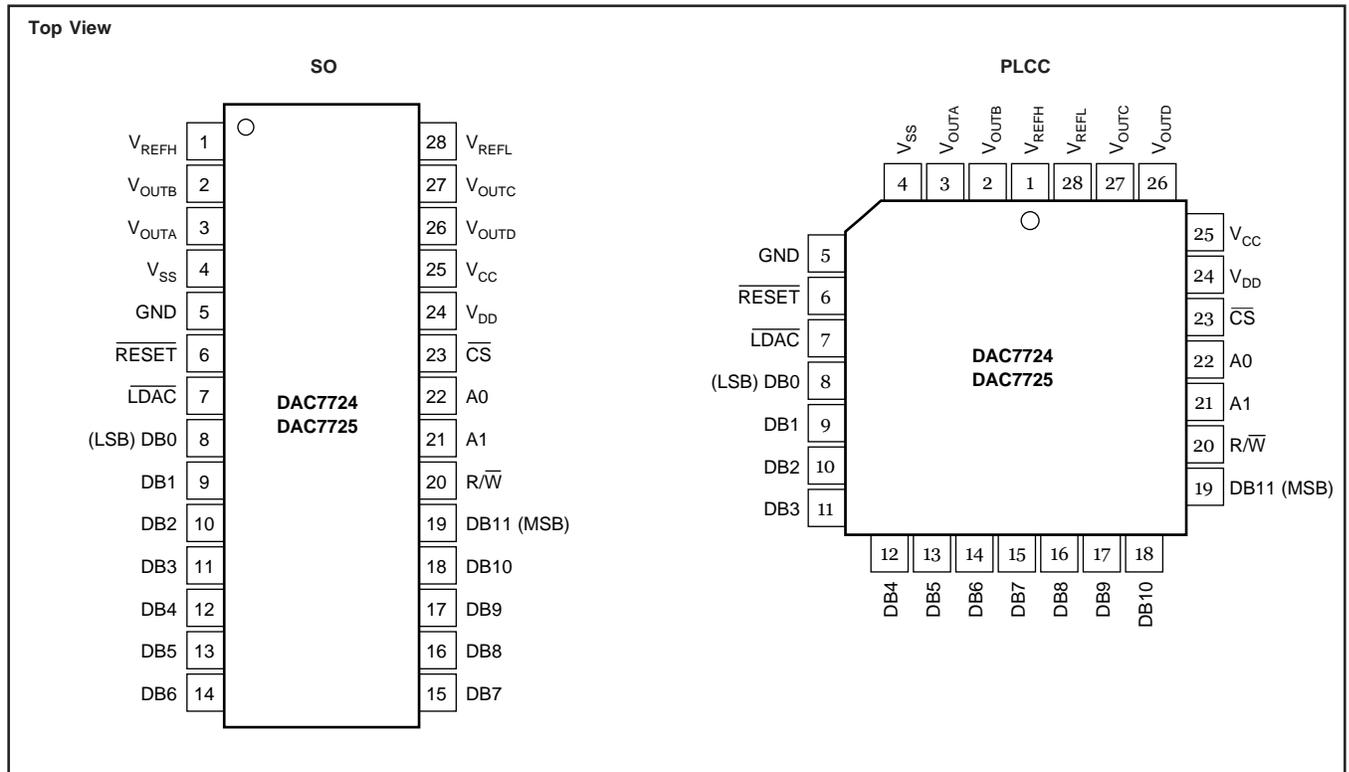
PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
DAC7724N	±2	±1	PLCC-28	251	-40°C to +85°C	DAC7724N	Rails
"	"	"	"	"	"	DAC7724N/750	Tape and Reel
DAC7724NB	±1	±1	PLCC-28	251	-40°C to +85°C	DAC7724NB	Rails
"	"	"	"	"	"	DAC7724NB/750	Tape and Reel
DAC7724U	±2	±1	SO-28	217	-40°C to +85°C	DAC7724U	Rails
"	"	"	"	"	"	DAC7724U/1K	Tape and Reel
DAC7724UB	±1	±1	SO-28	217	-40°C to +85°C	DAC7724UB	Rails
"	"	"	"	"	"	DAC7724UB/1K	Tape and Reel
DAC7725N	±2	±1	PLCC-28	251	-40°C to +85°C	DAC7725N	Rails
"	"	"	"	"	"	DAC7725N/750	Tape and Reel
DAC7725NB	±1	±1	PLCC-28	251	-40°C to +85°C	DAC7725NB	Rails
"	"	"	"	"	"	DAC7725NB/750	Tape and Reel
DAC7725U	±2	±1	SO-28	217	-40°C to +85°C	DAC7725U	Rails
"	"	"	"	"	"	DAC7725U/1K	Tape and Reel
DAC7725UB	±1	±1	SO-28	217	-40°C to +85°C	DAC7725UB	Rails
"	"	"	"	"	"	DAC7725UB/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /750 indicates 750 devices per reel). Ordering 750 pieces of "DAC7724/750" will get a single 750-piece Tape and Reel.

ESD PROTECTION CIRCUITS



PIN CONFIGURATIONS



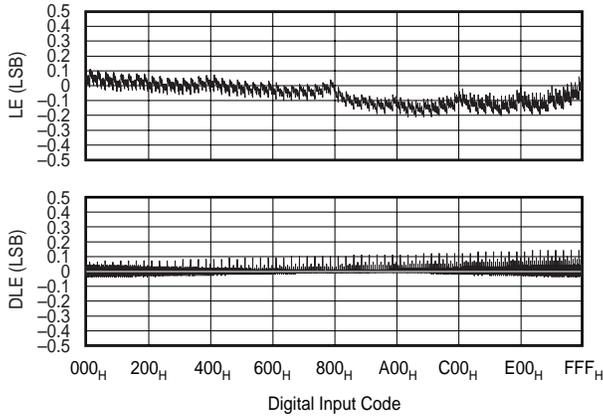
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
2	V_{OUTB}	DAC B Voltage Output.
3	V_{OUTA}	DAC A Voltage Output.
4	V_{SS}	Negative Analog Supply Voltage, 0V or -15V.
5	GND	Ground.
6	\overline{RESET}	Asynchronous Reset Input. Sets DAC and input registers to either mid-scale (800 _H , DAC7724) or zero-scale (000 _H , DAC7725) when LOW.
7	\overline{LDAC}	Load DAC Input. All DAC Registers are transparent when LOW.
8	DB0	Data Bit 0. Least significant bit of 12-bit word.
9	DB1	Data Bit 1
10	DB2	Data Bit 2
11	DB3	Data Bit 3
12	DB4	Data Bit 4
13	DB5	Data Bit 5
14	DB6	Data Bit 6
15	DB7	Data Bit 7
16	DB8	Data Bit 8
17	DB9	Data Bit 9
18	DB10	Data Bit 10
19	DB11	Data Bit 11. Most significant bit of 12-bit word.
20	R/\overline{W}	Read/Write Control Input (read = HIGH, write = LOW).
21	A1	Register/DAC Select (C or D = HIGH, A or B = LOW).
22	A0	Register/DAC Select (B or D = HIGH, A or C = LOW).
23	\overline{CS}	Chip Select Input.
24	V_{DD}	Positive Digital Supply, +5V.
25	V_{CC}	Positive Analog Supply Voltage, +15V nominal.
26	V_{OUTD}	DAC D Voltage Output.
27	V_{OUTC}	DAC C Voltage Output.
28	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.

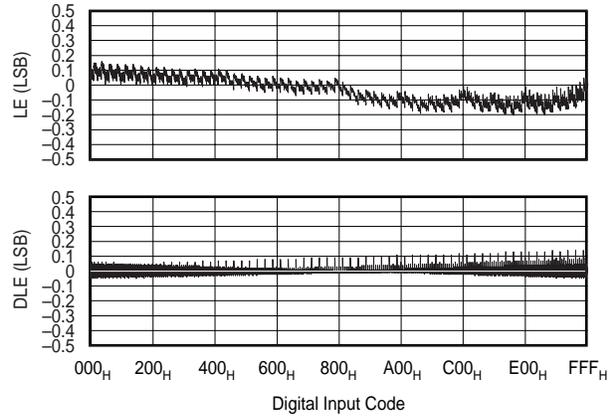
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

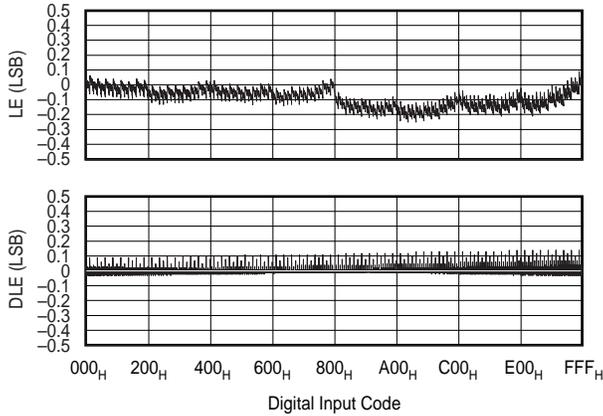
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



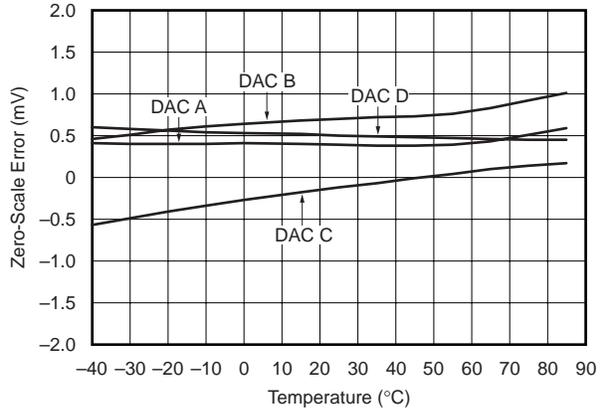
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



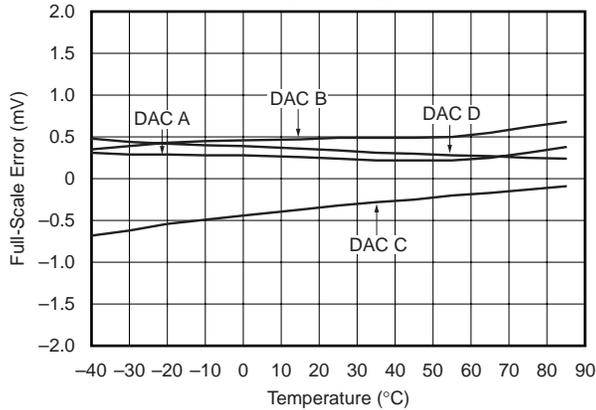
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel -40°C
(Typical of Each Output Channel)



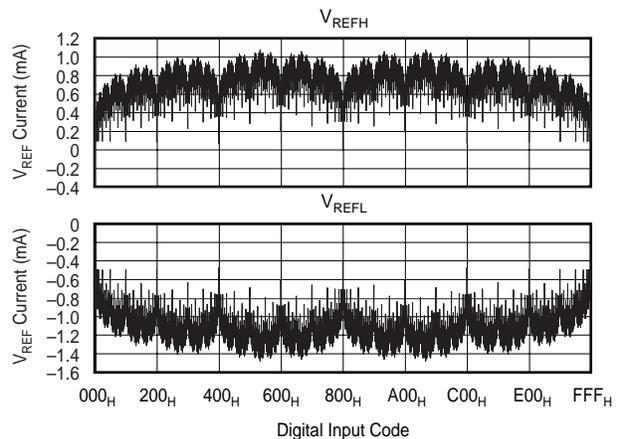
ZERO-SCALE ERROR vs TEMPERATURE
(Code 004_H)



FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)

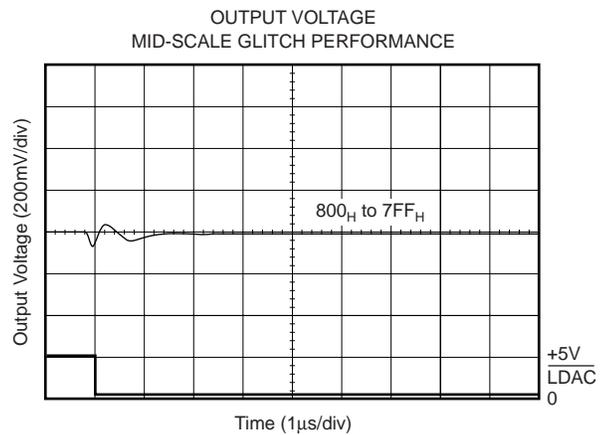
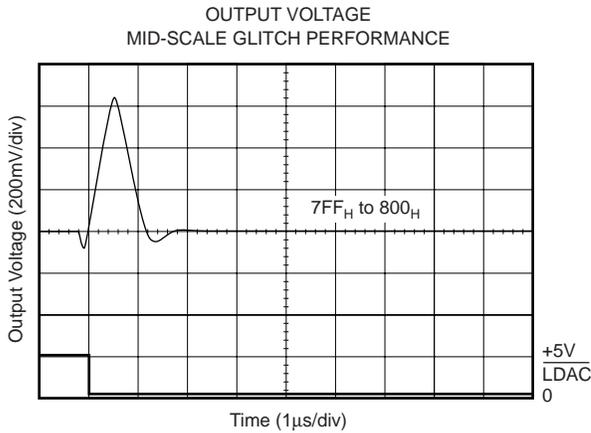
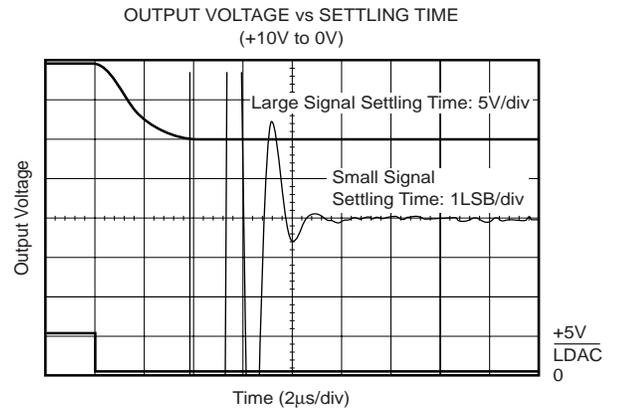
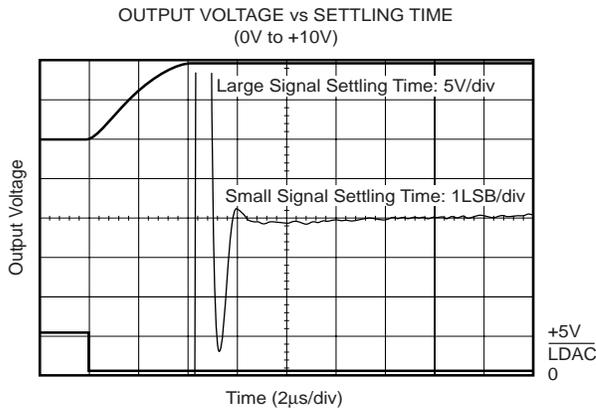
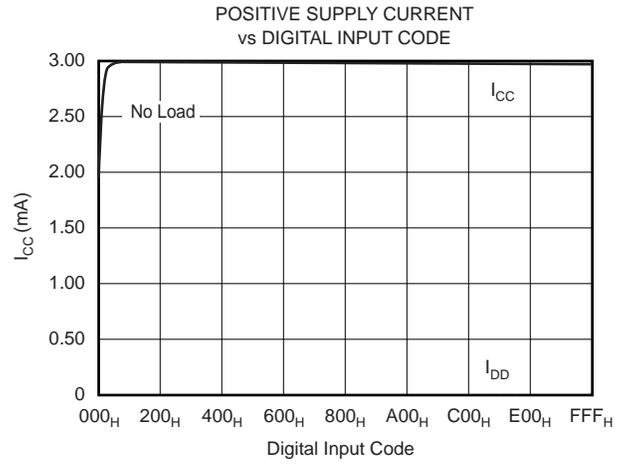
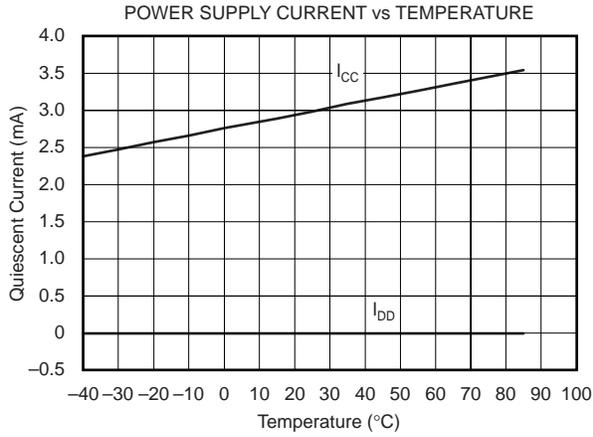


CURRENT vs CODE
All DACs Sent to Indicated Code



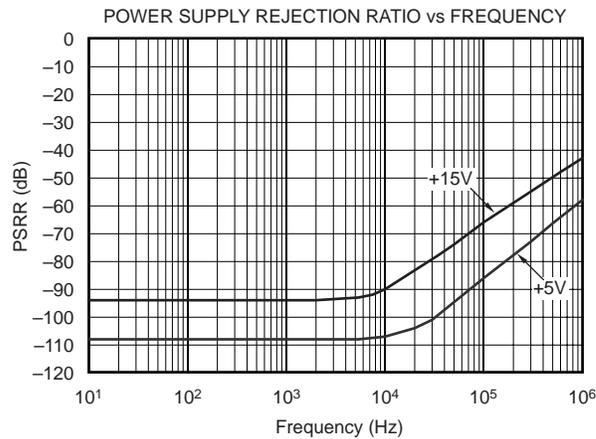
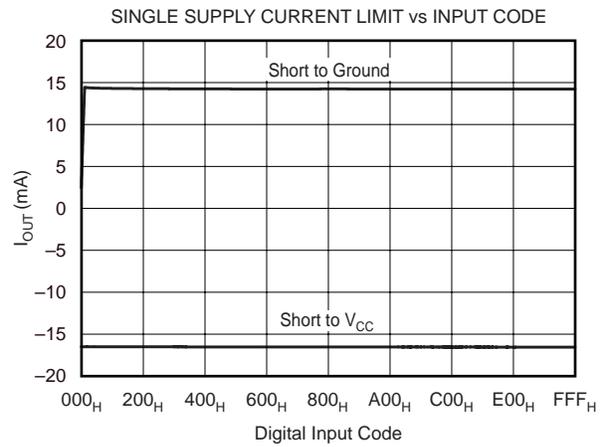
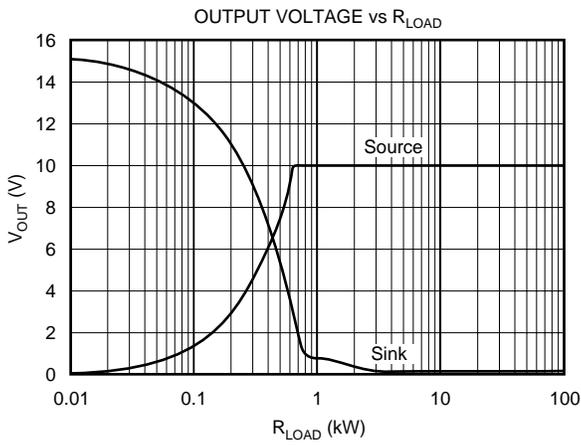
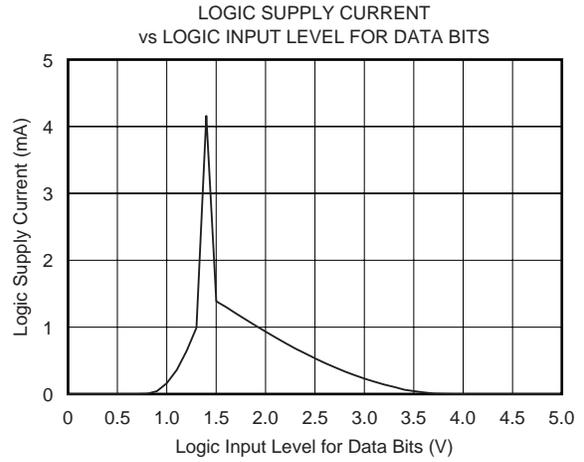
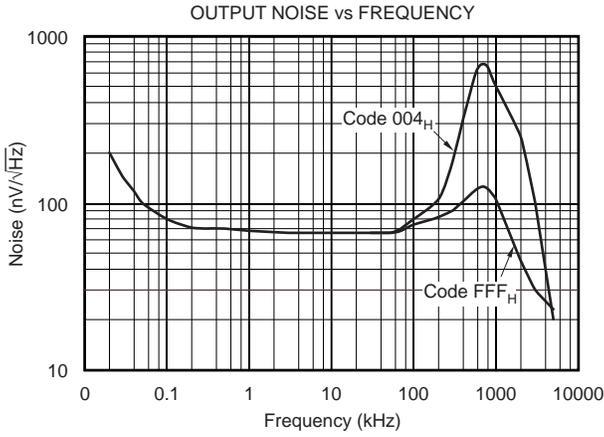
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

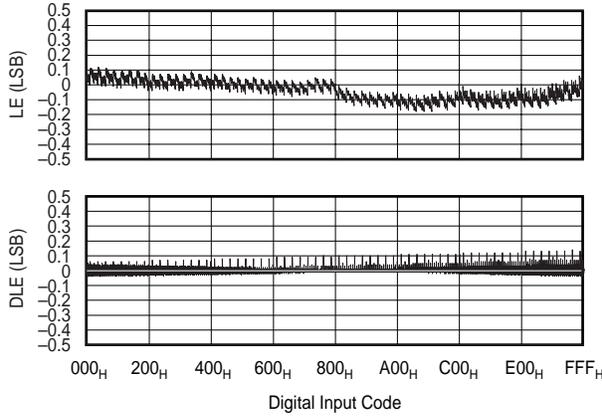
At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +10V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



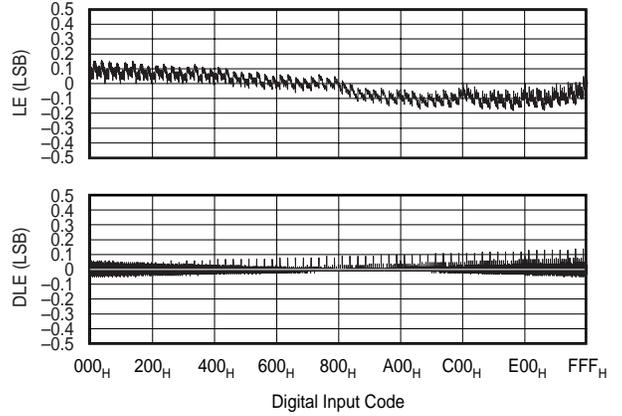
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, representative unit, unless otherwise specified.

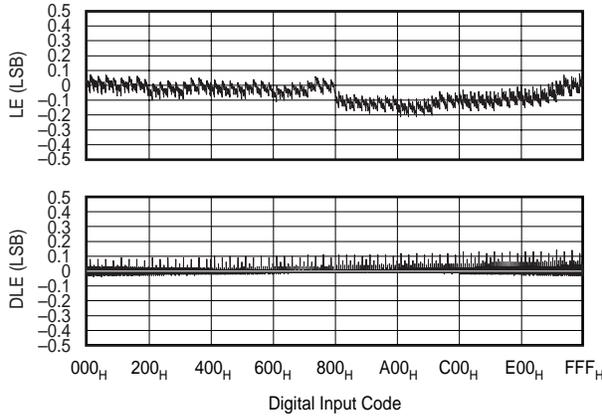
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



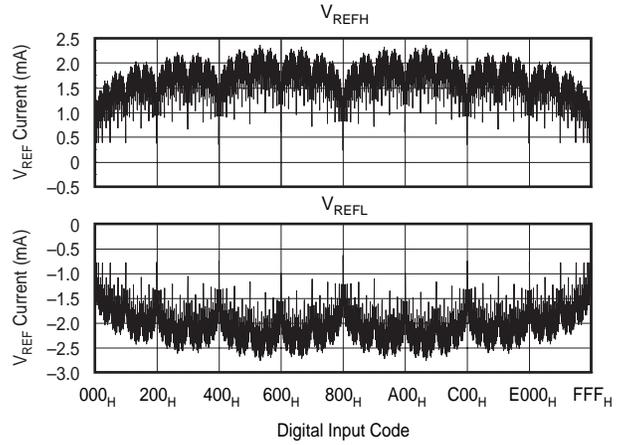
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



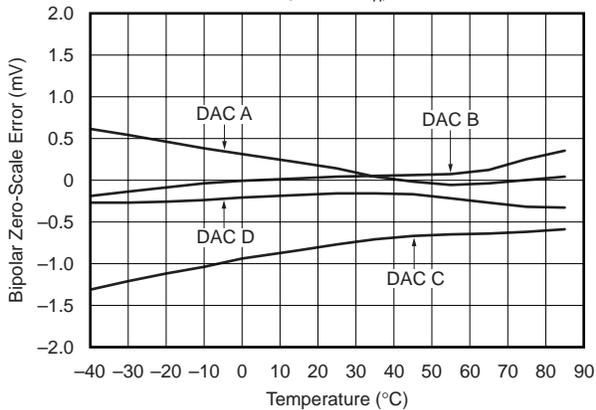
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel -40°C
(Typical of Each Output Channel)



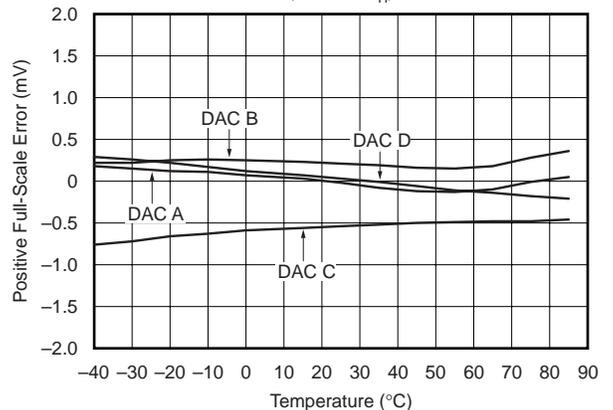
CURRENT vs CODE
All DACs Sent to Indicated Code



BIPOLAR ZERO-SCALE ERROR vs TEMPERATURE
(Code 800_H)

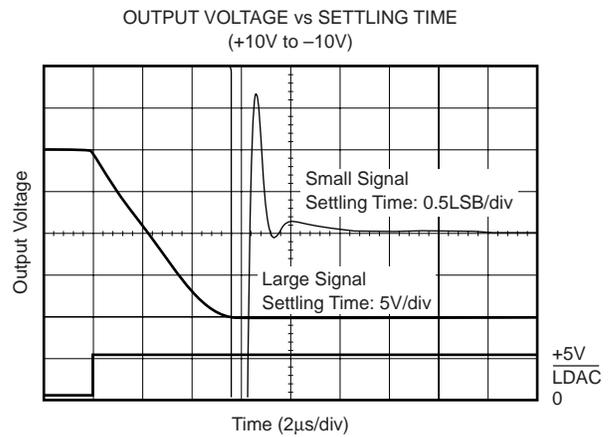
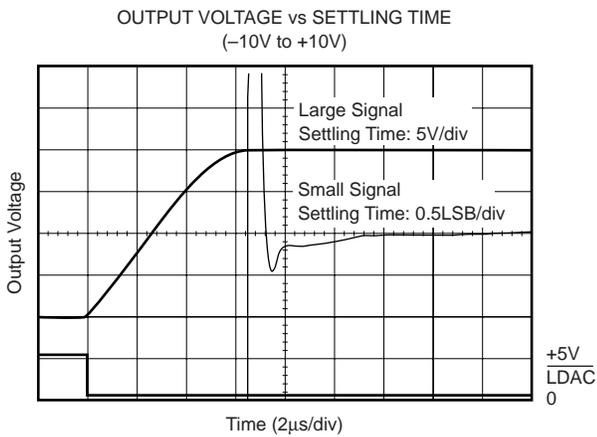
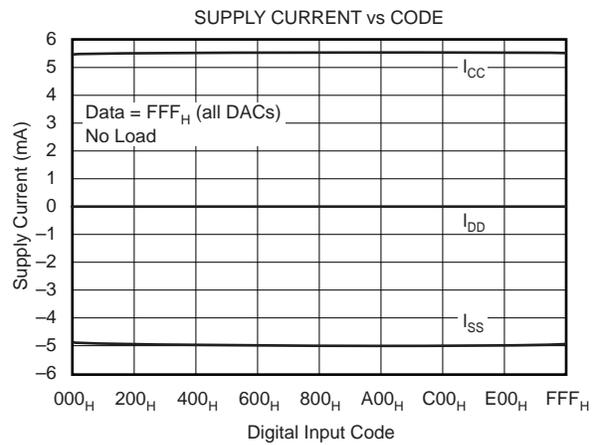
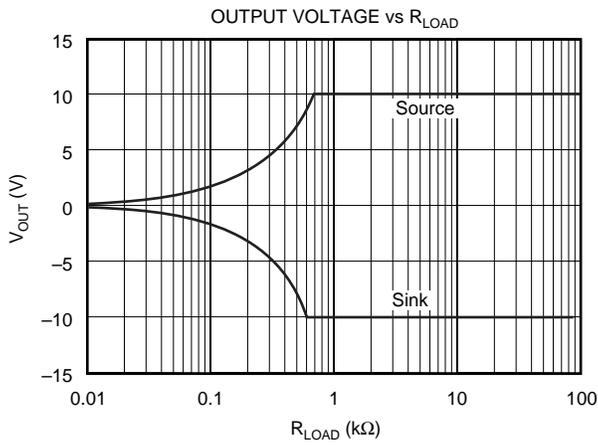
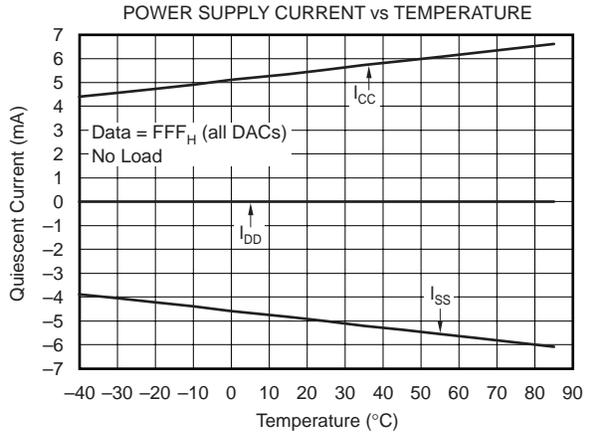
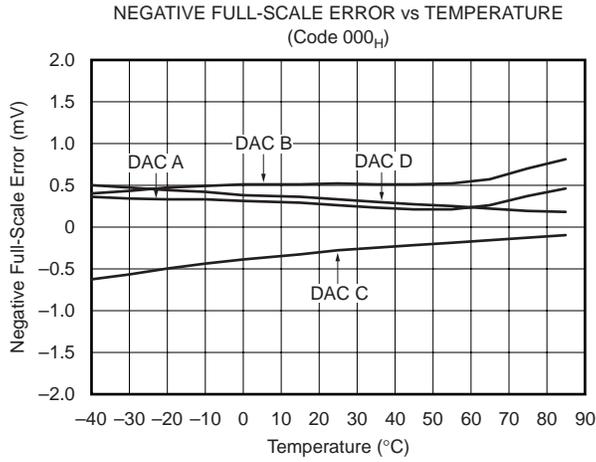


POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



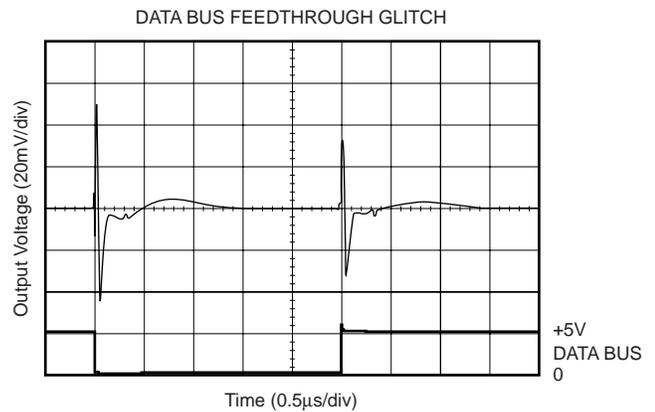
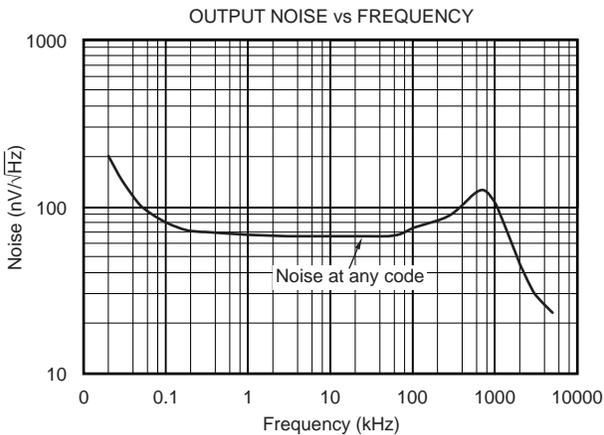
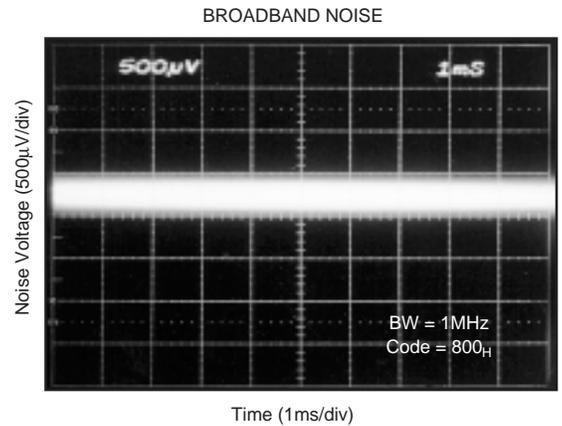
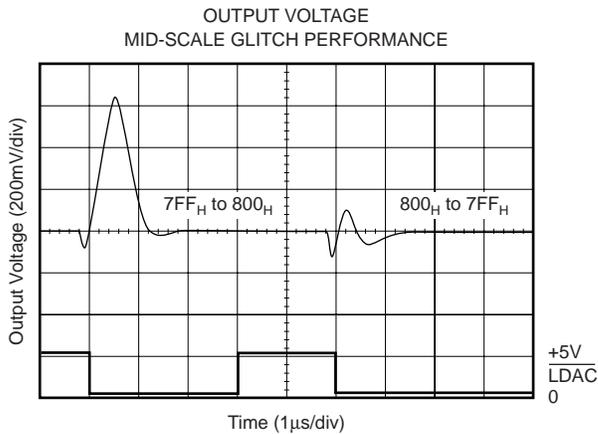
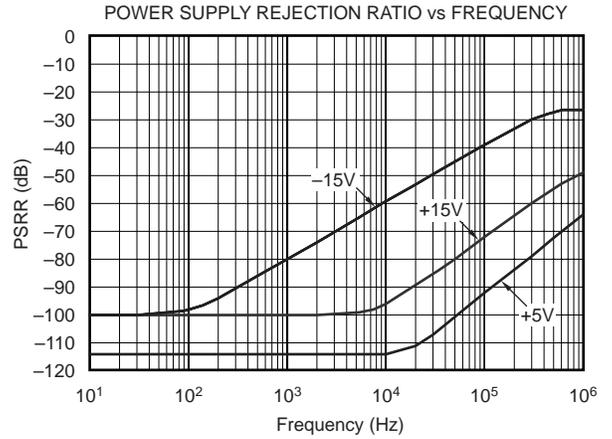
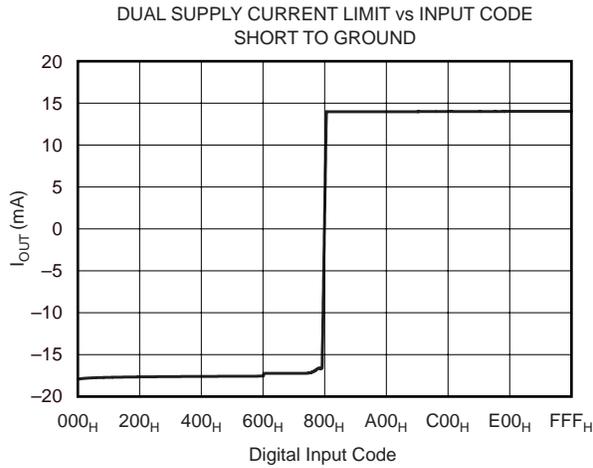
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7724 and DAC7725 are quad voltage output, 12-bit digital-to-analog converters (DACs). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer, as shown in Figure 1. Each DAC has its own R-2R ladder network and output op-amp, but all share the reference voltage inputs. The minimum voltage output (“zero-scale”) and maximum voltage

output (“full-scale”) are set by the external voltage references (V_{REFL} and V_{REFH} , respectively). The digital input is a 12-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from a single +15V supply or a dual $\pm 15V$ supply. Each device offers a reset function which immediately sets all DAC registers and DAC output voltages to mid-scale (DAC7724, code 800_H) or to zero-scale (DAC7725, code 000_H). See Figures 2 and 3 for the basic operation of the DAC7724/25.

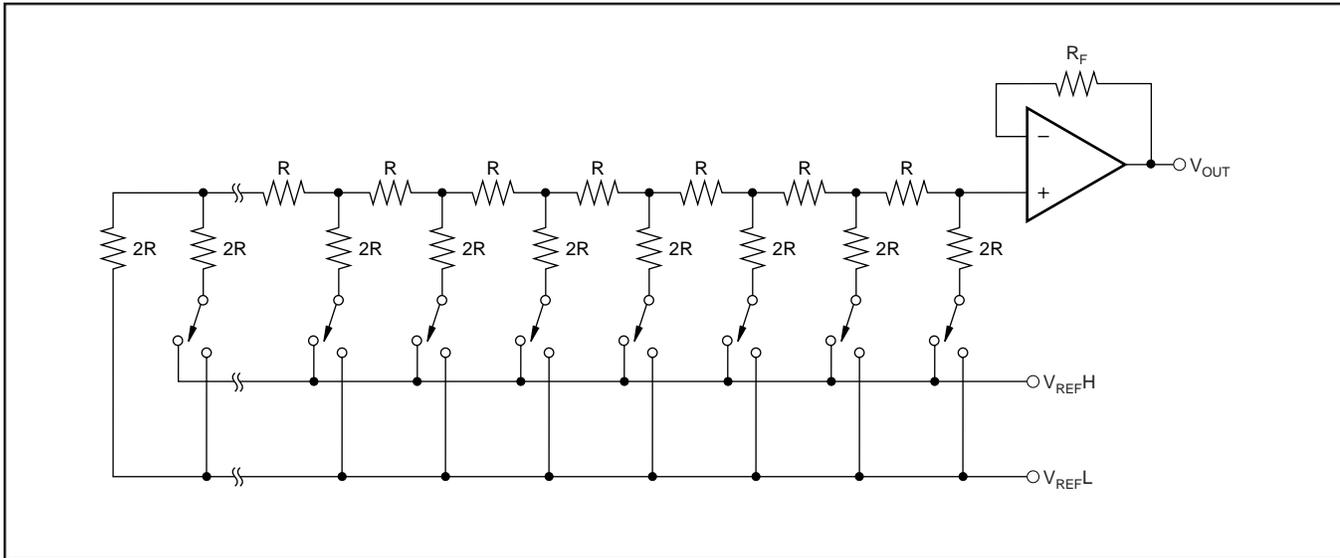


FIGURE 1. DAC7724/25 Architecture.

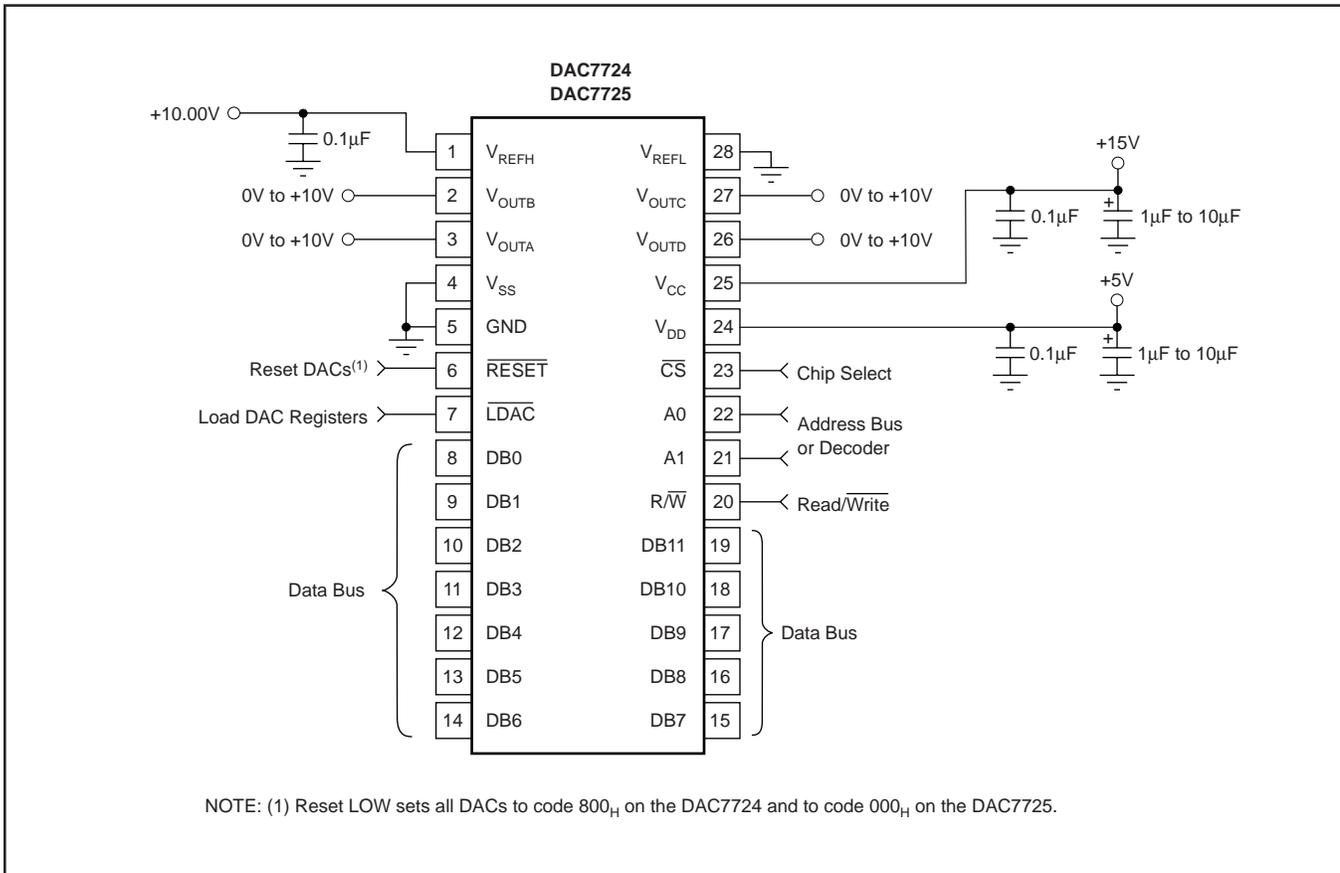


FIGURE 2. Basic Single-Supply Operation of the DAC7724/25.

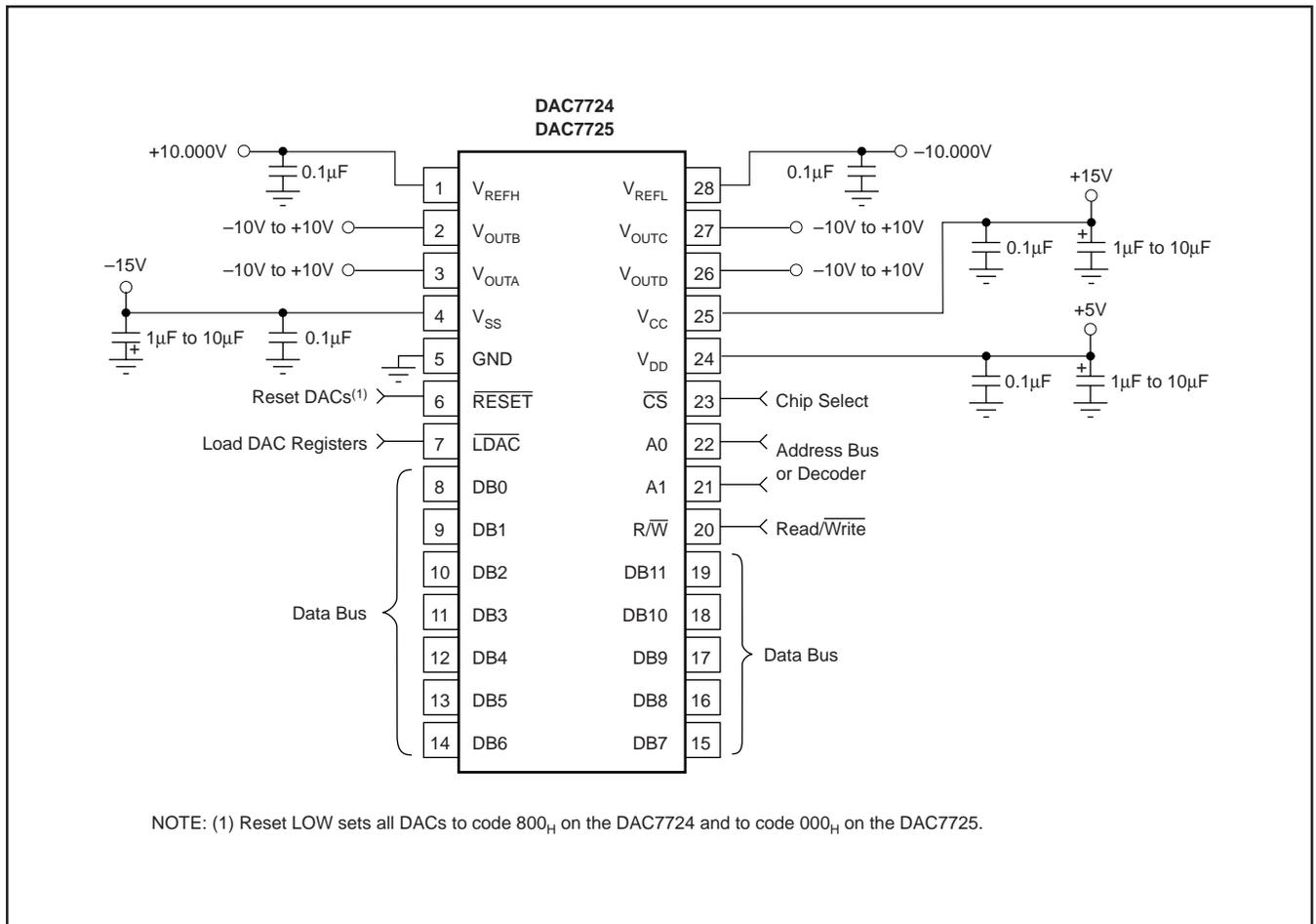


FIGURE 3. Basic Dual-Supply Operation of the DAC7724/25.

ANALOG OUTPUTS

When $V_{SS} = -15V$ (dual supply operation), the output amplifier can swing to within 4V of the supply rails, guaranteed over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. With $V_{SS} = 0V$ (single-supply operation) and R_{LOAD} connected to ground, the output can swing to ground. Note that the settling time of the output op-amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) if the output amplifier has a negative offset. At the negative offset limit of -4 LSB ($-9.76mV$), for the single-supply case, the first specified output starts at code 004_H.

REFERENCE INPUTS

For dual-supply operation, the reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 4V$ and $V_{CC} - 4V$ provided that V_{REFH} is at least 1.25V greater than V_{REFL} . For single-supply operation ($V_{SS} = 0V$), V_{REFL} value can be above 0V, with the same provision that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essen-

tially, the offset of the output op-amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of $-14.25V$ to $-15.75V$. The voltage on V_{SS} sets several bias points within the converter, if V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages and can vary from a few microamps to approximately 0.3mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. See "Reference Current vs Code" in the Typical Performance Curves.

The analog supplies (or the analog supplies and the reference power supplies) have to come up first. If the power supplies for the references come up first, then the V_{CC} and V_{SS} supplies will be "powered from the reference via the ESD protection diodes" (see page 4).

Bypassing the reference voltage or voltages with at least a 0.1 μ F capacitor placed as close to the DAC7724/25 package is strongly recommended.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7724/25. Note that each internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the register becomes transparent. When this signal is returned HIGH, the digital word currently in the register is latched. The first set of registers (the Input Registers) are triggered via the A0, A1, $\overline{R/W}$, and \overline{CS} inputs. Only one of these registers is transparent at any given time. The second set of registers (the DAC Registers) are all transparent when \overline{LDAC} input is pulled LOW.

Each DAC can be updated independently by writing to the appropriate Input Register and then updating the DAC Register. Alternatively, the entire DAC Register set can be configured as always transparent by keeping \overline{LDAC} LOW—the DAC update will occur when the Input Register is written.

The double buffered architecture is mainly designed so that each DAC Input Register can be written at any time and then all DAC output voltages updated simultaneously by pulling \overline{LDAC} LOW. It also allows a DAC Input Register to be written to at any point and the DAC voltage to be synchronously changed via a trigger signal connected to \overline{LDAC} .

DIGITAL TIMING

Figure 4 and Table II provide detailed timing for the digital interface of the DAC7724 and DAC7725.

DIGITAL INPUT CODING

The DAC7724 and DAC7725 input data is in straight binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \cdot N}{4096}$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) errors.

A1	A0	$\overline{R/W}$	\overline{CS}	\overline{RESET}	\overline{LDAC}	SELECTED INPUT REGISTER	STATE OF SELECTED INPUT REGISTER	STATE OF ALL DAC REGISTERS
L ⁽¹⁾	L	L	L	H ⁽²⁾	L	A	Transparent	Transparent
L	H	L	L	H	L	B	Transparent	Transparent
H	L	L	L	H	L	C	Transparent	Transparent
H	H	L	L	H	L	D	Transparent	Transparent
L	L	L	L	H	H	A	Transparent	Latched
L	H	L	L	H	H	B	Transparent	Latched
H	L	L	L	H	H	C	Transparent	Latched
H	H	L	L	H	H	D	Transparent	Latched
L	L	H	L	H	H	A	Readback	Latched
L	H	H	L	H	H	B	Readback	Latched
H	L	H	L	H	H	C	Readback	Latched
H	H	H	L	H	H	D	Readback	Latched
X ⁽³⁾	X	X	H	H	L	NONE	(All Latched)	Transparent
X	X	X	H	H	H	NONE	(All Latched)	Latched
X	X	X	X	L	X	ALL	Reset ⁽⁴⁾	Reset ⁽⁴⁾

NOTES: (1) L = Logic LOW. (2) H= Logic HIGH. (3) X = Don't Care. (4) DAC7724 resets to 800_H, DAC7725 resets to 000_H. When \overline{RESET} rises, all registers that are in their latched state retain the reset value.

TABLE I. DAC7724 and DAC7725 Control Logic Truth Table.

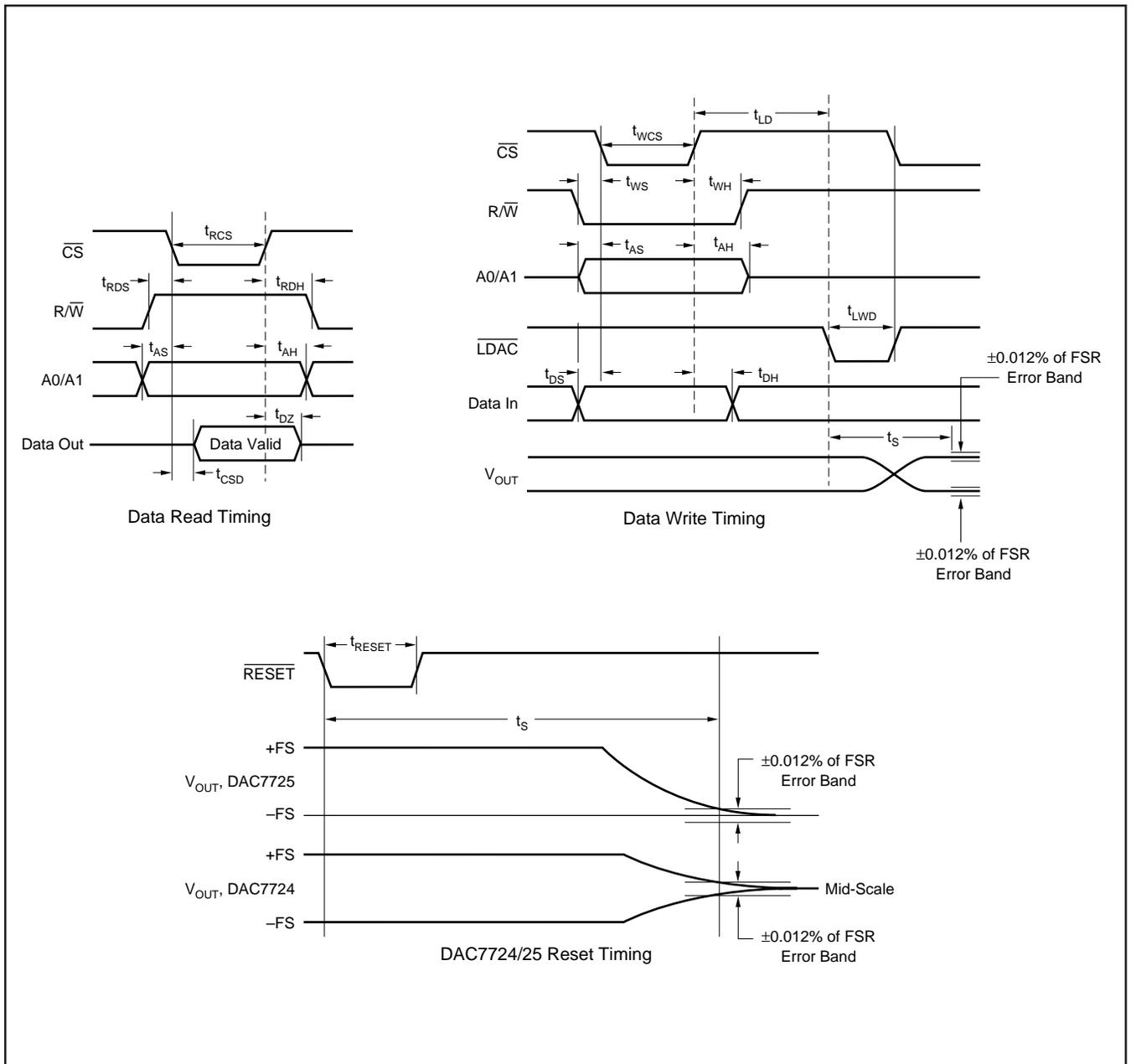


FIGURE 4. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	\overline{CS} LOW for Read	200			ns
t_{RDS}	R/W HIGH to \overline{CS} LOW	10			ns
t_{RDH}	R/W HIGH after \overline{CS} HIGH	10			ns
t_{DZ}	\overline{CS} HIGH to Data Bus in High Impedance		100		ns
t_{CSD}	\overline{CS} LOW to Data Bus Valid		100	160	ns
t_{WCS}	\overline{CS} LOW for Write	50			ns
t_{WS}	R/W LOW to \overline{CS} LOW	0			ns
t_{WH}	R/W LOW after \overline{CS} HIGH	0			ns
t_{AS}	Address Valid to \overline{CS} LOW	0			ns
t_{AH}	Address Valid after \overline{CS} HIGH	0			ns
t_{LD}	LDAC Delay from \overline{CS} HIGH	10			ns
t_{DS}	Data Valid to \overline{CS} LOW	0			ns
t_{DH}	Data Valid after \overline{CS} HIGH	0			ns
t_{LWD}	LDAC LOW	50			ns
t_{RESET}	RESET LOW Time	50			ns
t_s	Settling Time			10	μ s

TABLE II. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7724N	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N	Samples
DAC7724N/750	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N	Samples
DAC7724NB	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N B	Samples
DAC7724NB/750	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N B	Samples
DAC7724NB/750G4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N B	Samples
DAC7724NBG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7724N B	Samples
DAC7724U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7724U/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7724UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7724UB/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7724UBG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7724UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7724U B	Samples
DAC7725N	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7725N	Samples
DAC7725NB	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7725N B	Samples
DAC7725NB/750	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7725N B	Samples
DAC7725NB/750G4	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7725N B	Samples
DAC7725NBG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-245C-168 HR	-40 to 85	DAC7725N B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7725U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples
DAC7725UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples
DAC7725UB/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples
DAC7725UB/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples
DAC7725UBG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples
DAC7725UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7725U B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

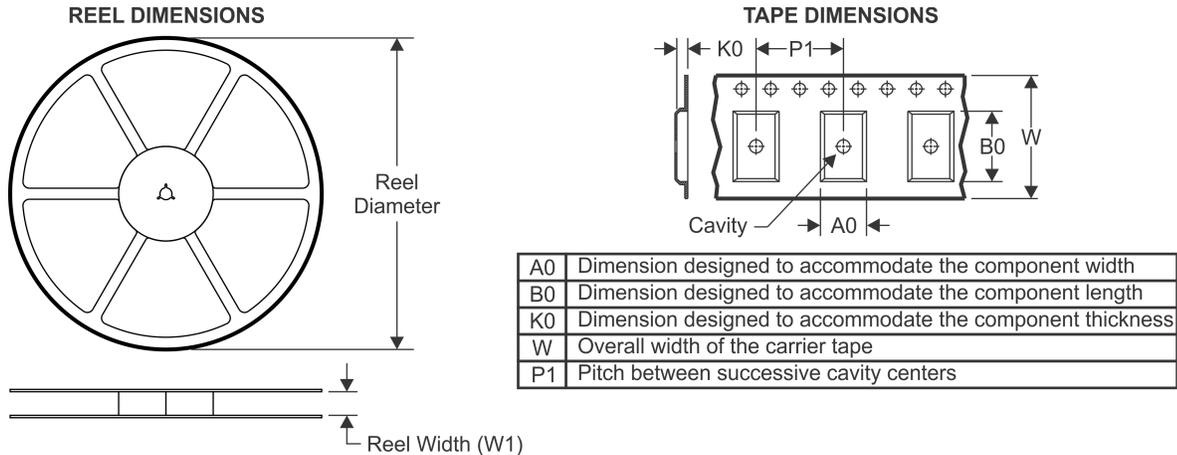
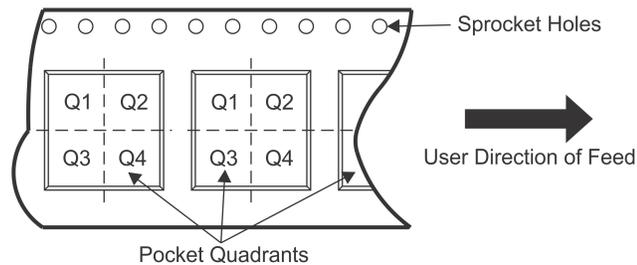
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

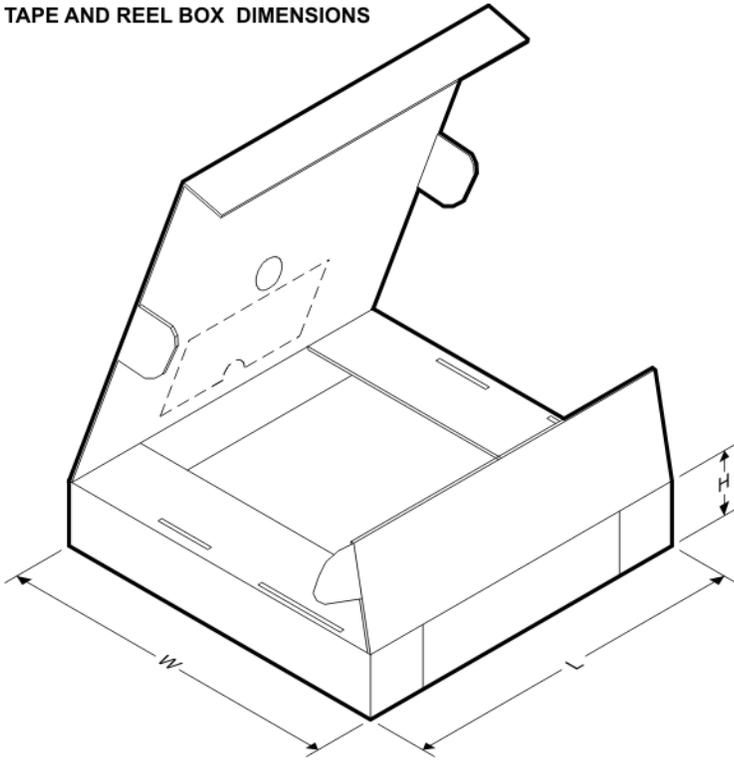
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7724U/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DAC7724UB/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DAC7725UB/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7724U/1K	SOIC	DW	28	1000	367.0	367.0	55.0
DAC7724UB/1K	SOIC	DW	28	1000	367.0	367.0	55.0
DAC7725UB/1K	SOIC	DW	28	1000	367.0	367.0	55.0

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.