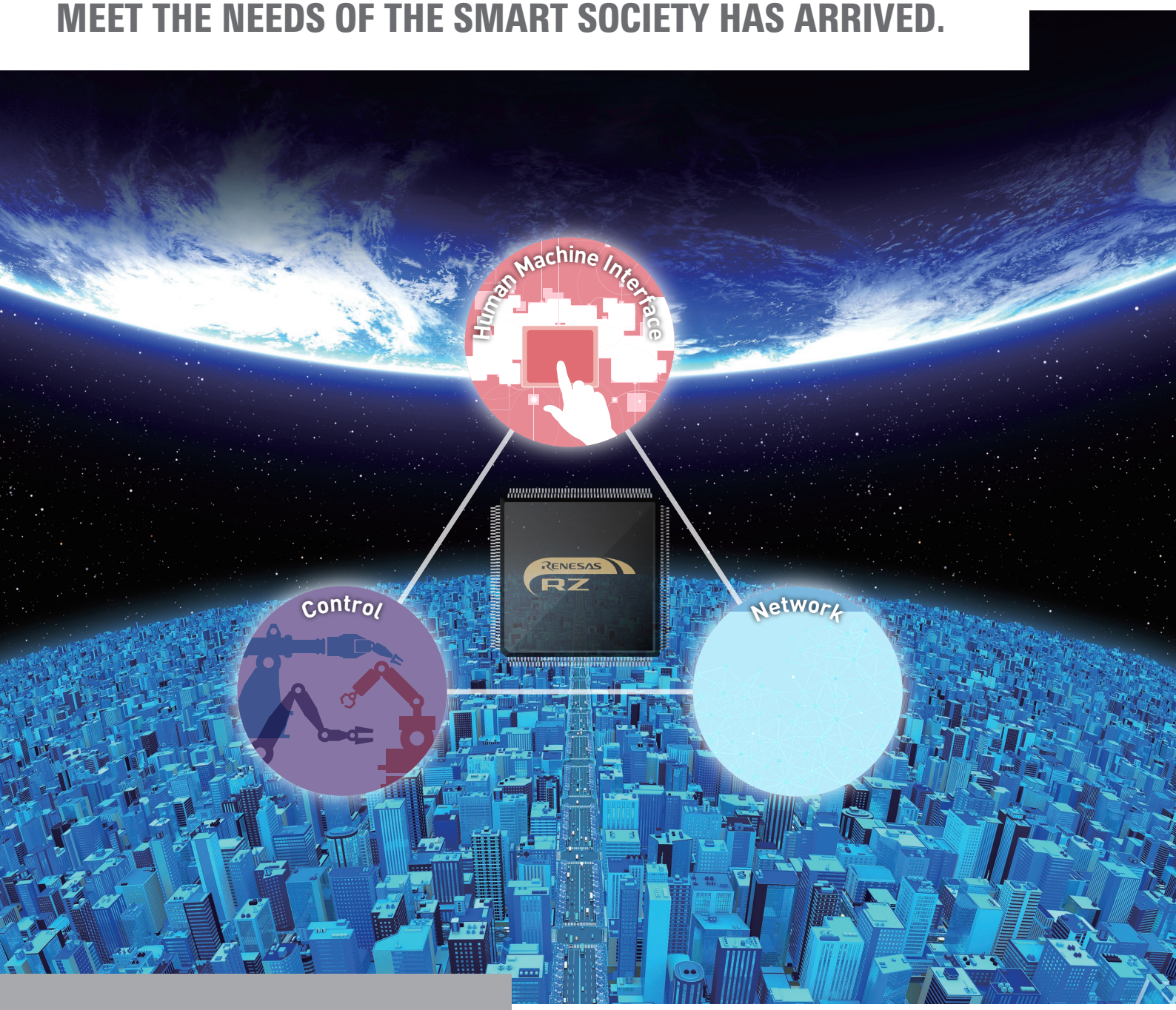
RZ FAMILY MICROPROCESSORS

64-Bit & 32-Bit High-performance MPUs

2023.04

THE NEXT-GENERATION PROCESSOR TO MEET THE NEEDS OF THE SMART SOCIETY HAS ARRIVED.



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The utilization of intelligent technology is advancing in all aspects of our lives, including electric household appliances, industrial equipment, building management, power grids, and transportation. The cloud-connected “smart society” is coming ever closer to realization. Microcontrollers are now expected to provide powerful capabilities not available previously, such as high-performance and energy-efficient control combined with interoperation with IT networks, support for human-machine interfaces, and more. To meet the demands of this new age, Renesas has drawn on its unmatched expertise in microcontrollers to create the RZ family of embedded processors. The lineup of these “next-generation processors that are as easy to use as conventional microcontrollers” to meet different customer requirements.

The Zenith of the Renesas micro

As embedded processors to help build the next generation of advanced products, the RZ family offers features not available elsewhere and brings new value to customer applications.

RZ/V Series

64-bit Cortex®-A CPU, Up to 1.2GHz
Low-power Embedded AI
for Vision-AI Application

RZ/G Series

32/64-bit Cortex®-A CPU, Up to 1.5Hz
64-bit RISC-V CPU, Up to 1.0GHz
for HMI and IoT Application

RZ/A Series

32/64-bit Cortex®-A CPU, Up to 1GHz
- DDR3L/4 (RZ/A3UL)
- Up to 10MB Embedded RAM for HMI Application

RZ/T Series

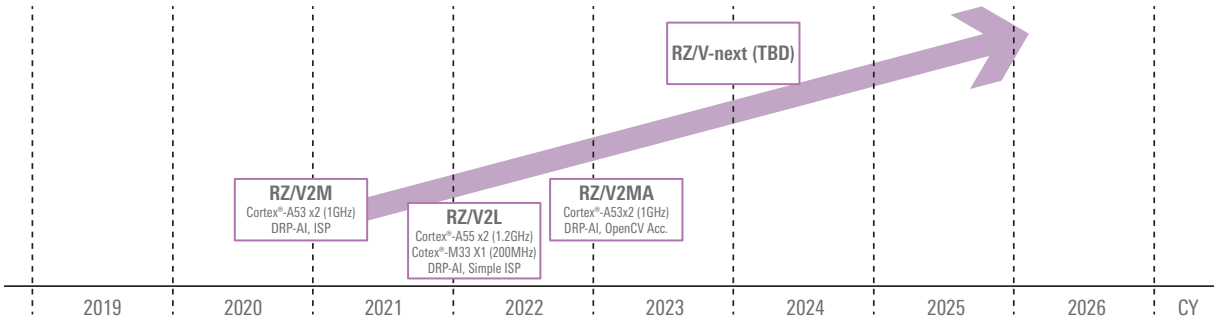
32-bit Cortex®-R CPU, Up to 800MHz
Real-time Control
Multi-protocol Encoder I/F
for AC servo, Actuator, Inverter

RZ/N Series

32-bit Cortex®-A/M/R CPU, Up to 500MHz
Multi-protocol Industrial Network
for PLC, Remote IO, Gateway

RZ/V Series

RZ/V Series Roadmap



RZ/V Series Features

- AI Accelerator "DRP-AI" achieves high-speed AI inference and low power consumption
- 4K (2160p30) video codec and high-performance image signal processor (ISP) (RZ/V2M)
- Provides Vision Processing Accelerator (OpenCV) and Image Signal Processor (Simple ISP) function as DRP library
- Equipped with a 3D Graphics Engine for fast image rendering (RZ/V2L)
- Adopts Civil Infrastructure Platform (CIP) Linux kernel that can be supported for more than 10 years

* DRP: Dynamically Reconfigurable Processor

Founded in CY2016

CIVIL INFRASTRUCTURE PLATFORM

RZ/V Series Application

IP Camera

Surveillance camera

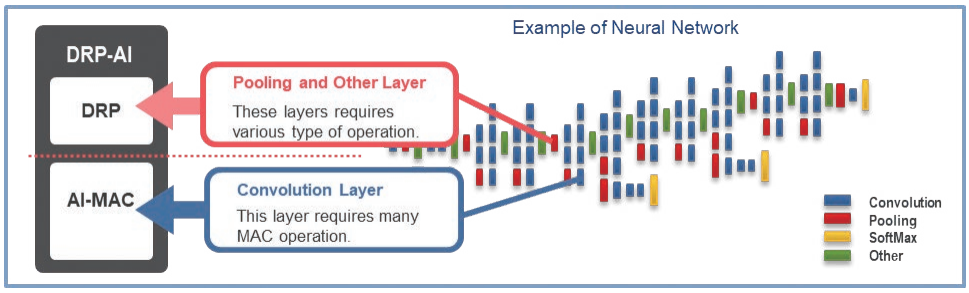
Retail

Logistics

Image inspection

Features of DRP-AI

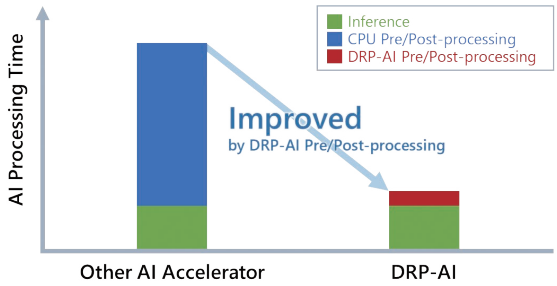
DRP-AI consists of AI-MAC (multiply-accumulate processor) and DRP (reconfigurable processor). AI processing can be executed at high speed by assigning AI-MAC for operations on the convolution layer and fully connected layer, and DRP for other complex processing such as preprocessing and pooling layer.



For more detailed technical information on DRP-AI, please refer to the following white paper.
White Paper: Embedded AI-Accelerator DRP-AI

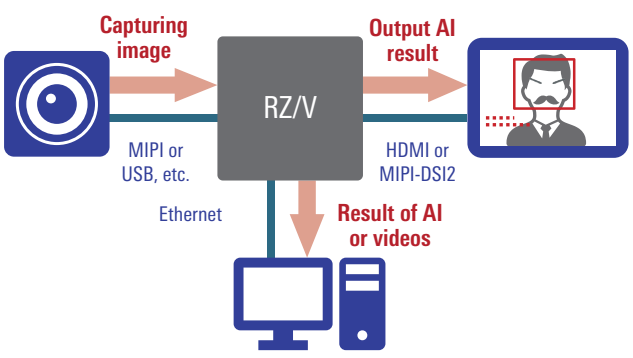
While most AI accelerators specialize only in AI inference and rely on the CPU for pre- and post-processing, DRP-AI integrates pre- and post-processing and AI inference into a single DRP-AI hardware to achieve superior AI processing performance.

	Other AI Accelerator	DRP-AI
Pre-processing	CPU	DRP-AI
Inference	AI Accelerator	DRP-AI
Post-processing	CPU	DRP-AI

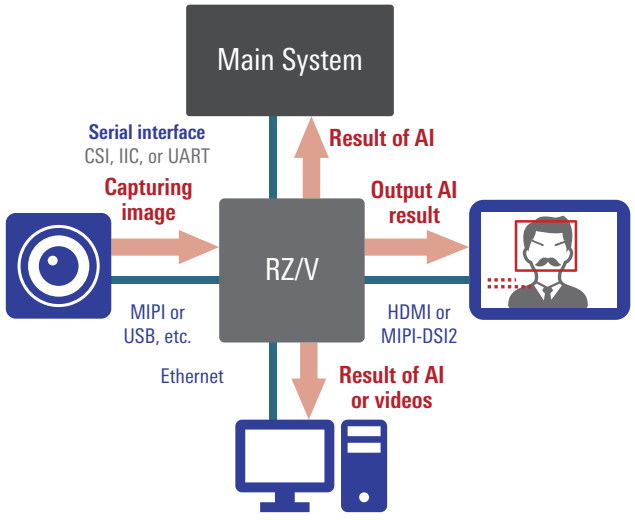


Use Case

Standalone system



Add-on the AI inference on your system



RZ/V2M Group

CPU
- 2× Cortex-A53 (up to 1.0GHz)

Vision and AI
- AI Accelerator; DRP-AI at 1.0 TOPS/W class
- Image Signal Processor (ISP) of multi-stream available
- Camera Interface; 2× MIPI CSI-2
- Face and Human Detection Engine

Video and Graphics
- H.265/H.264 Multi Codec
- JPEG Codec Engine
- 2D Graphics Engine

Display Interface
- MIPI-DSI (4-lane)
- HDMI 1.4a

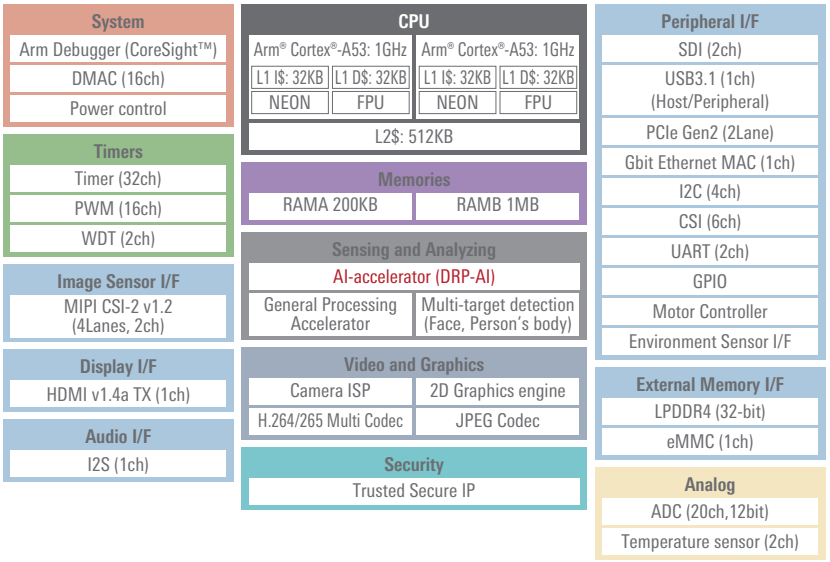
Audio Interface
- Serial Sound Interface × 1ch

Communication Interface
- SD Host × 2ch
- PCI-Express 2.0 (2-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I^2C Bus × 4ch
- SCI × 6ch
- UART × 2ch

Memory Interface
- NAND Flash Interface ONFI1.0 × 1ch
- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch

Security
- Hardware Security Engine

RZ/V2M block diagram



RZ/V2L Group

CPU
- 2× Cortex-A55 or 1× Cortex-A55 (up to 1.2GHz)
- 1× Cortex-M33 (up to 200MHz)

Vision and AI
- AI Accelerator; DRP-AI
  * Image Signal Processor (Simple ISP) Function is provided as DRP Library
- Camera Interface; 1× MIPI CSI-2 / 1× Digital Parallel

Video and Graphics
- H.264 Codec
- 3D Graphics Engine

Display Interface
- MIPI-DSI (4-lane)
- Digital Parallel

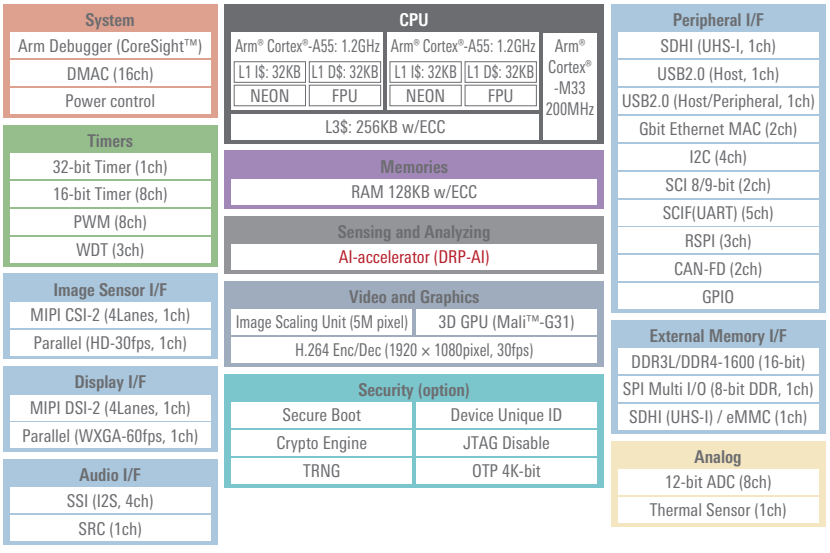
Audio Interface
- Serial Sound Interface × 4ch

Communication Interface
- Gigabit Ethernet × 2ch
- USB2.0 Host × 1ch
- USB2.0 Host/Function × 1ch
- I^2C Bus × 4ch
- SCI × 2ch
- UART × 5ch

Memory Interface
- SPI Multi I/O (8bit DDR) × 1ch
- SDHI (UHS-I) / eMMC × 1ch
- 16-bit DDR3L-1333/DDR4-1600 × 1ch

Security
- Hardware Security Engine (Option)

RZ/V2L block diagram



RZ/V2MA Group

CPU
- 2× Cortex-A53 (up to 1.0GHz)

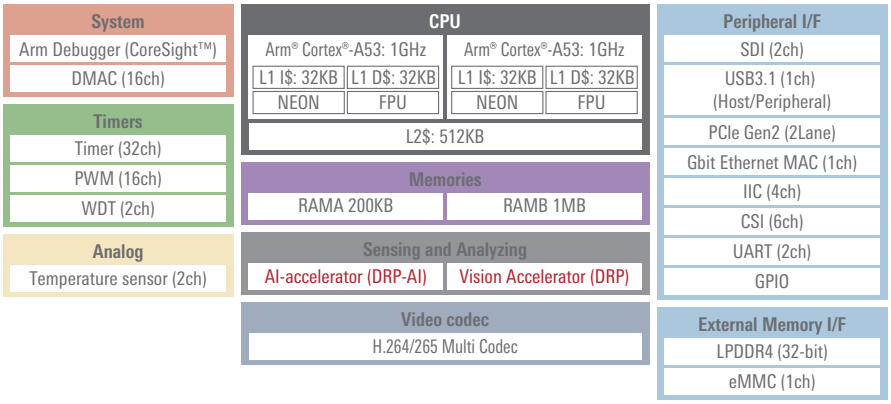
Vision and AI
- AI Accelerator; DRP-AI at 1.0 TOPS/W class
- OpenCV Accelerator (DRP)

Video and Graphics
- H.265/H.264 Multi Codec

Communication Interface
- SD Host × 2ch
- PCI-Express 2.0 (2-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I^2C Bus × 4ch
- SCI × 6ch
- UART × 2ch

Memory Interface
- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch

RZ/V2MA block diagram



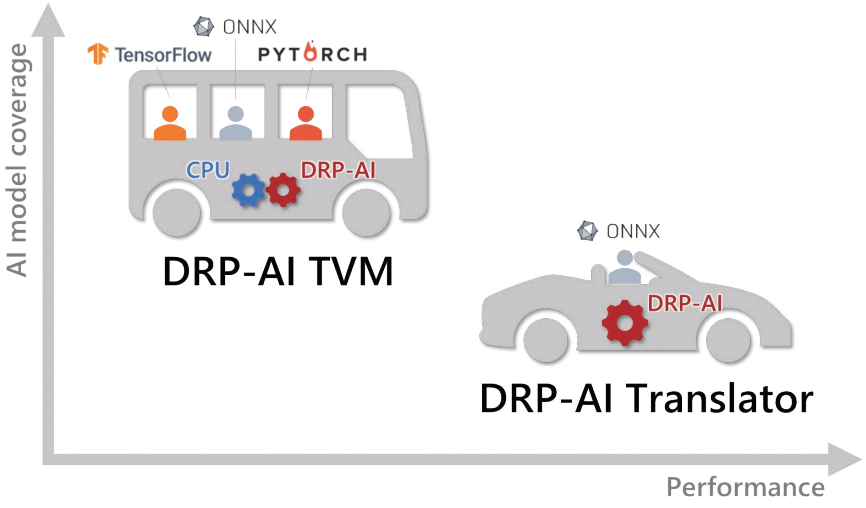
Development Environment for AI

Renesas offers two development environments: DRP-AI Translator, designed to extract the full performance potential of DRP-AI, and DRP-AI TVM,** which extends the coverage of the AI model to both DRP-AI and the CPU.

- DRP-AI Translator
  A translator that converts trained AI models in ONNX* format into object code for DRP-AI.

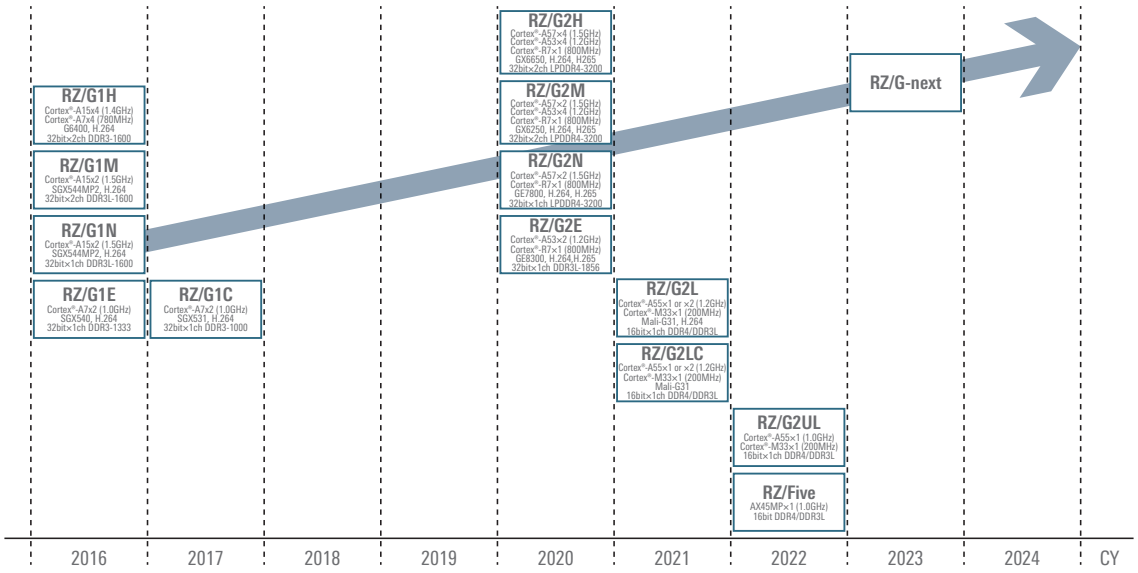
- DRP-AI TVM**
  This AI development environment brings the power of the Apache TVM open-source deep learning compiler to DRP-AI Translator and supports AI models utilizing Arm processors as well as DRP-AI.

* ONNX: Open Neural Network Exchange
** DRP-AI TVM is powered by EdgeCortix MERA™ Compiler Framework



RZ/G Series

RZ/G Series Roadmap



RZ/G2 Highlights

- High Performance
  64-bit Arm Cortex-A cores, plus powerful 3D graphics engine and video engine capable of supporting up to 4K UHD, to offer the highest performance
- Wide Coverage
  Entry-level RZ/G2L Group 3 products equipped with Cortex-A55 with improved processing performance have been newly added to the RZ/G2 lineup
- High Reliability
  Built-in Error Correction Code (ECC) for internal and external memory, which is essential for high-reliability mission critical systems
- Super Long Term Support (SLTS)
  Applying Civil Infrastructure Platform (CIP) Linux, the Linux kernel will be provided with over 10 years of maintenance
- Verified Linux Package
  Renesas verifies and provides a Linux package that combines CIP and Linux basic software. Minimize your Linux maintenance resources

RZ/G2 Specification 1

Items	RZ/G2H	RZ/G2M	RZ/G2N	RZ/G2E
CPU (Arm® Cortex®-A)	4× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz 4× Cortex®-A53@1.2GHz L1,L2 Parity/ECC	2× Cortex®-A57@1.5GHz L1,L2 Parity/ECC	2× Cortex®-A53@1.2GHz L1,L2 Parity/ECC
CPU (Arm® Cortex®-R)	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC	1× Cortex®-R7@800MHz L1,TCM w/ECC
DRAM I/F	32-bit ×2ch LPDDR4(3200) w/ECC	32-bit ×2ch LPDDR4(3200) w/ECC	32-bit ×1ch LPDDR4(3200) w/ECC	32-bit ×1ch DDR3L(1856) w/ECC
Video in	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	2×MIPI-CSI2, 2×Digital (RGB/YCbCr) up to 8 input image can be captured	1×MIPI-CSI2, 1×Digital(RGB/YCbCr) up to 2 input image can be captured
Video Codec	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264	Support up to FHD resolutions Decoding: H.265, Encoding and Decoding: H.264
3D GFX	PowerVR GX6650@600MHz	PowerVR GX6250@600MHz	PowerVR GE7800@600MHz	PowerVR GE8300@600MHz
Display out	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	1×HDMI, 1×LVDS, 1×Digital RGB	2×LVDS or 1×LVDS, 1×Digital RGB
USB	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×2ch (1H, 1H/F/OTG) USB3.0/2.0×1ch (DRD)	USB2.0×1ch (H/F) USB3.0/2.0×1ch (DRD)
Gbit Ether	1ch	1ch	1ch	1ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
PCIe	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	2ch (Rev2.0 1Lane)	2ch (Rev2.0 1Lane) one of the 2ch is shared with SATA	1ch (Rev2.0 1Lane)
SATA	1ch (Pin Shared)	No	1ch (Pin Shared)	No
Package	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	1022pin FCBGA, 29mm×29mm 0.8mm ball pitch	552pin FCBGA, 21mm×21mm 0.8mm ball pitch

Pin Compatible

RZ/G2 Specification 2

Items	RZ/G2L	RZ/G2LC	RZ/G2UL (Type2) Pin compatible with RZ/G2LC	RZ/G2UL (Type1) Full function
CPU (Arm® Cortex®-A)	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× or 2× Cortex®-A55@1.2GHz L1,L3 Parity/ECC	1× Cortex®-A55@1.0GHz L1,L3 Parity/ECC	1× Cortex®-A55@1.0GHz L1,L3 Parity/ECC
CPU (Arm® Cortex®-M)	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz	1× Cortex®-M33@200MHz
DRAM I/F	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC	16-bit ×1ch DDR4-1600/DDR3L-1333 w/ECC
Video in	1×MIPI CSI-2 or 1×Digital Parallel input	1×MIPI CSI-2	1×MIPI CSI-2	1×MIPI CSI-2
Video Codec	Support up to Full HD @30fps resolutions Encoding and Decoding: H.264	–	–	–
3D GFX	Arm Mali-G31 GPU @500MHz	Arm Mali-G31 GPU @500MHz	–	–
Display out	1×MIPI DSI or 1×Digital Parallel output	1×MIPI DSI	–	1×Digital Parallel output
USB	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)	USB2.0×2ch (1Host, 1Host/Function/OTG)
Gbit Ether	2ch	1ch	1ch	2ch
CAN	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)	2ch (support CAN-FD)
12-bit ADC	8ch	–	–	2ch
Package	551pin LFBGA, 21mm×21mm 0.8mm ball pitch 456pin LFBGA, 15mm×15mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch	361pin LFBGA, 13mm×13mm 0.5mm ball pitch

Pin Compatible

RZ/Five (RISC-V) Features and Specification

The RZ/Five is an entry-class general-purpose Linux MPU with a 64-bit RISC-V architecture.

- General-purpose MPU adopting an Open Instruction Set Architecture RISC-V
- Provide development environment to easy mutual migration between ARM and RISC-V
- General-purpose MPU specialized for IoT Edge

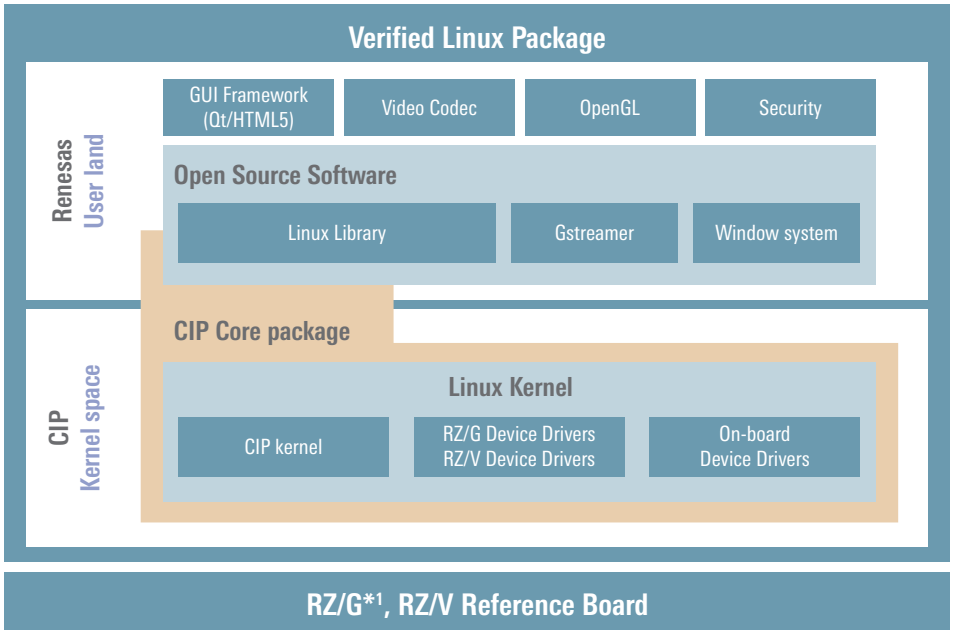
Items	RZ/Five
CPU	64bit RISC-V CPU Core AndesCore™ AX45MP Single core 1.0 GHz
DRAMI/F	16-bit × 1ch DDR4-1600/DDR3L-1333 w/ECC
USB	USB2.0 × 2ch (1Host, 1Host/Function/OTG)
Gbit Ether	2ch : 13mm × 13mm Package 1ch : 11mm × 11mm Package
CAN	2ch (support CAN-FD)
12-bit ADC	2ch
Package	361pin, LFBGA, 13mm × 13mm, 0.5mm pitch 266pin, LFBGA, 11mm × 11mm, 0.5mm pitch

Super Long Term Software Support

Renesas RZ/G and RZ/V microprocessors are the only embedded MPUs that meet the long-term support demands for industrial and infrastructure equipment manufacturers through the 10+ year support offered by the Super Long Term Support (SLTS) kernel maintained by the Civil Infrastructure Platform (CIP). The CIP SLTS Linux kernel supports countermeasures against vulnerability to security attacks with a long-term maintenance period of 10 years or more. This reduces Linux maintenance costs and simplifies adoption of reliable industrial-grade Linux.

Verified Linux Package(VLP) Reduces Cost and Simplifies Design

The "Verified Linux Package (VLP)" for the RZ/G and RZ/V series is a combination of the Civil Infrastructure Platform (CIP) Core Package and the basic software (Linux BSP, multimedia, graphics, security, etc.) for IoT devices. This packaged software is verified by Renesas and is available from the Renesas RZ Linux platform site. With VLPs, you can start developing applications quickly while minimizing Linux maintenance resources.



GUI Framework
- Qt application framework
- HTML5 application framework

Multimedia
- H.264 Codec
- H.265 Decoder
- 3D graphics

Secure Middle Ware
- Encrypted kernel boot
- Security communication
- Secure storage

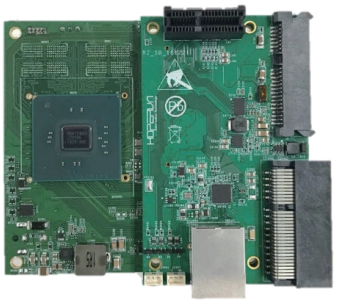
CIP SLTS Kernel
- Civil Infrastructure Platform project
- 10+ years super long term support Reliability/Security/Real-time

*1: RZ/G Reference Board is used for Kernel development as a software development platform for CIP projects.

Flexible Development Kits

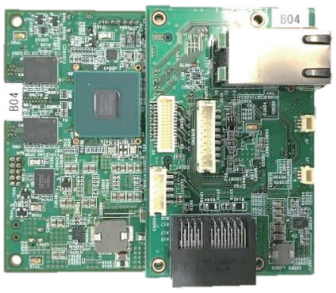
RZ/G2 development kits support the industry standard 96Boards specification and SMARC specification to enable evaluation and speed development with wide variety of mezzanine boards and existing carrier boards. Renesas provides circuit schematics, component BOMs, and board layout data to make it easy to spin your own custom hardware.

RZ/G2H,G2M,G2N Development Kit (96Boards format compatible)



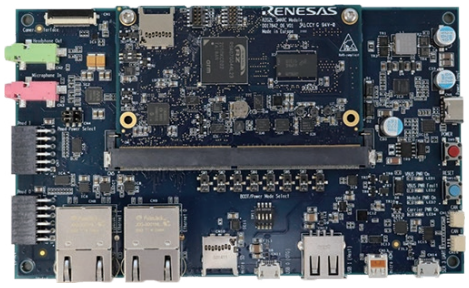
- Main Memory: 4 GB DDR4
- QSPI NOR FLASH 64 MByte
- I²C EEPROM 512 Byte
- External Storage: micro SD × 1
- Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT

RZ/G2E Development Kit (96Boards format compatible)

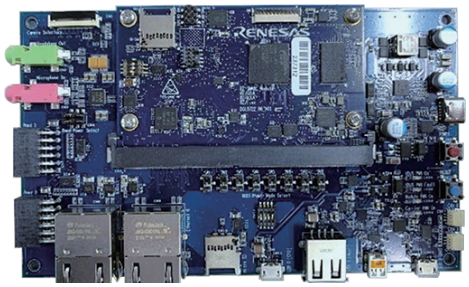


- Main Memory: 2 GB DDR3L
- QSPI NOR FLASH 64 MByte
- I²C EEPROM 512 Byte
- External Storage: micro SD × 1
- Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
- HDMI out / LVDS out or MIPI DSI out
- Wi-Fi + BT

RZ SMARC v2.1 Module + Carrier Board



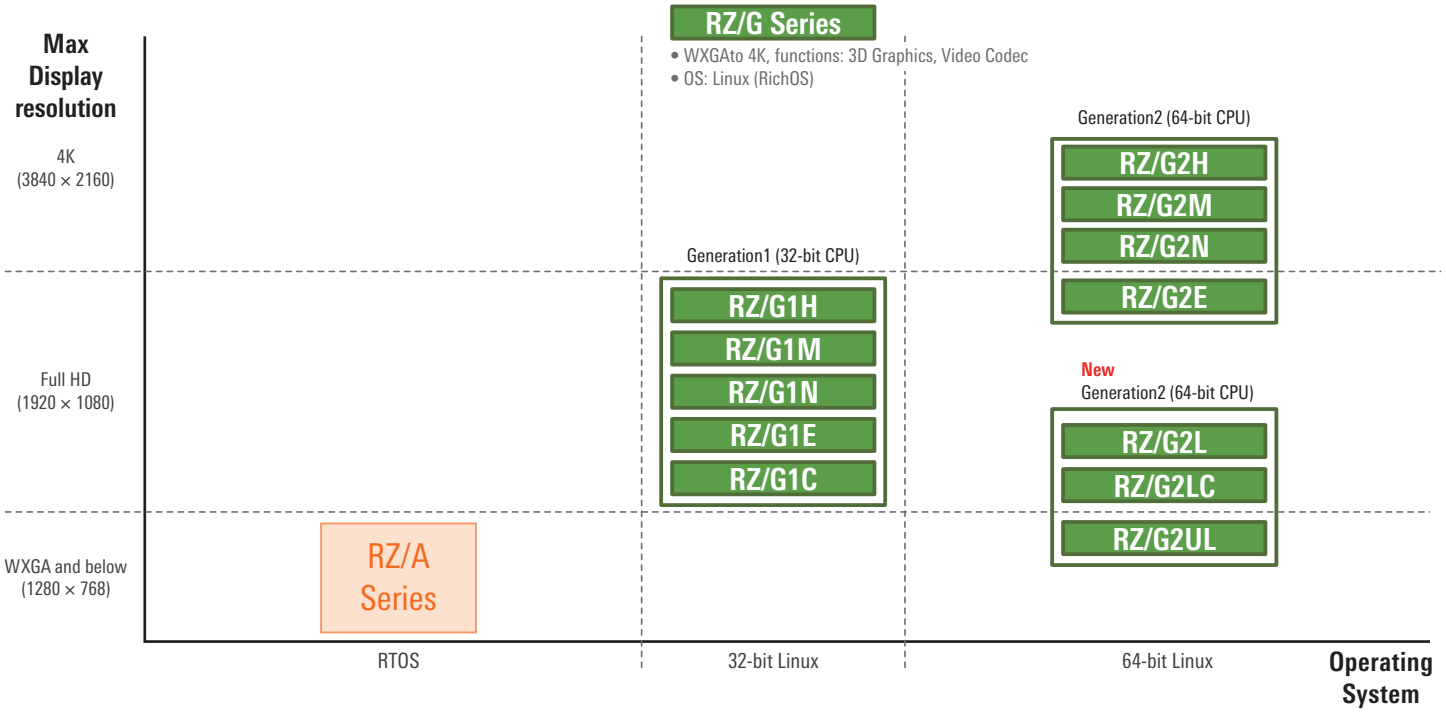
- RZ/G2L, RZ/G2LC, RZ/G2UL SMARC Module
  - Size: 82mm × 50mm
  - Processor: RZ/G2L, RZ/G2LC, RZ/G2UL (Type-1)
  - Main Memory: 2GB DDR4 (1GB × 2) *G2UL: 1GB (1GB × 1)
  - QSPI NOR FLASH: 16MB
  - eMMC Memory: 64GB
  - External Storage: micro SD × 1
  - A/D Converter Interface × 2
  - JTAG connector



- RZ/Five SMARC Module
  - Size: 82mm × 50mm
  - Processor: RZ/Five
  - Main Memory: 1GB DDR4 (1GB × 1)
  - QSPI NOR FLASH: 16MB
  - eMMC Memory: 64GB
  - External Storage: micro SD × 1
  - A/D Converter Interface × 2
  - JTAG connector

- Carrier Board
  - Size: 160mm × 100mm
  - Gigabit Ethernet × 2
  - USB2.0 × 2ch (OTG × 1ch, Host × 1ch)
  - MIPI CSI-2 Camera connector (can connect to Google Coral Camera)
  - Micro HDMI (output) connector
  - CAN-FD × 2
  - External Storage: micro SD × 1
  - Audio Line In × 1
  - Audio Line Out × 1
  - PMOD × 2
  - USB-Type C for Power Input

HMI Solutions



RZ/G2H (R8A774Ex)

CPU core
- Arm® Cortex®-A57, quad-core
  Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core
  Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core
  Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels

External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)

3D graphics
- PowerVR™ GX6650

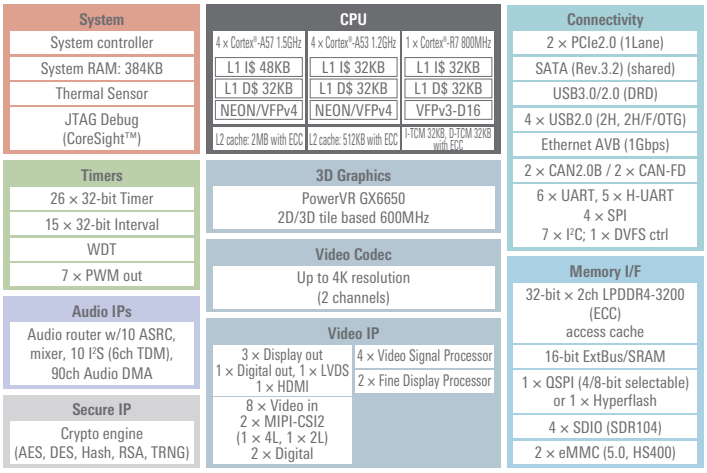
Video functions
- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/reduction, filtering)

Audio functions
- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels

Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel

Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2H (R8A774Ex) block diagram



FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

RZ/G2M (R8A774Ax)

CPU core
- Arm® Cortex®-A57, quad-core
  Max. operating frequency: 1.5GHz
- Arm® Cortex®-A53, quad-core
  Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core
  Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-A53)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 512KB

Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 2 channels

External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)

3D graphics
- PowerVR™ GX6250

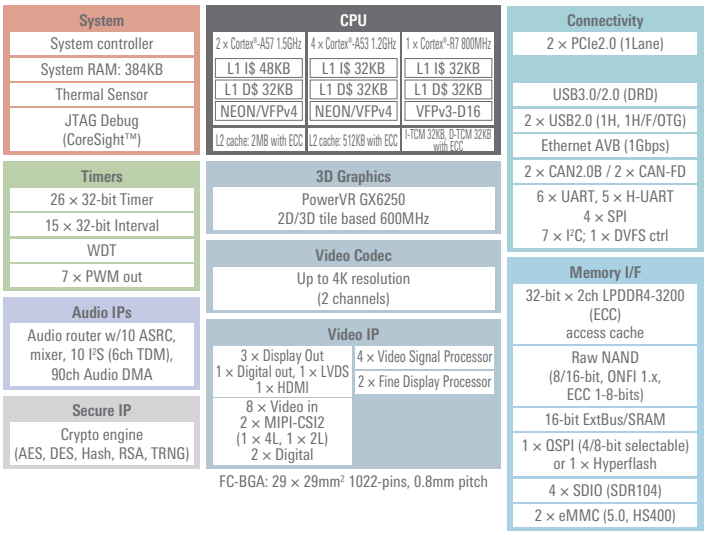
Video functions
- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions
- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels

Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels

Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722, GMII/MII interface, PHY device connection support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2M (R8A774Ax) block diagram



FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

RZ/G2N (R8A774Bx)

CPU core
- Arm® Cortex®-A57, quad-core
  Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core
  Max. operating frequency: 800MHz

Cache memory (Cortex®-A57)
- L1 instruction cache: 48KB
- L1 data cache: 32KB
- L2 cache: 2MB

Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory
- Ability to connect LPDDR4-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1 channel

External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 2 channels (one of PHY is shared with Serial ATA)

3D graphics
- PowerVR™ GE7800

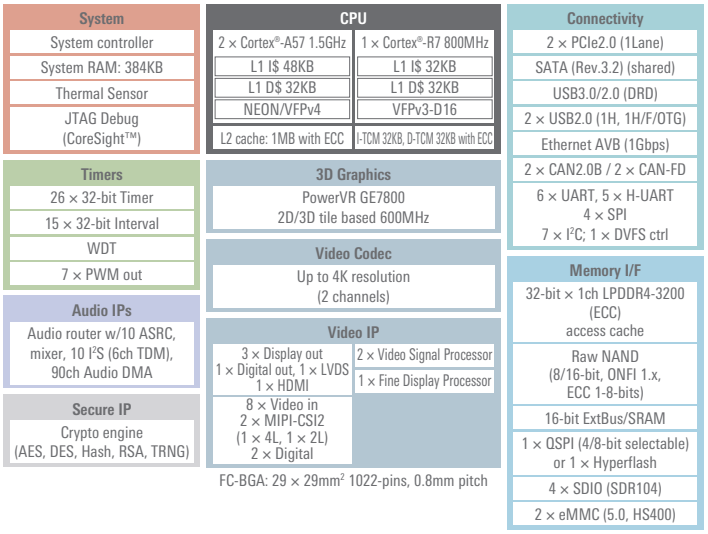
Video functions
- Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions
- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels

Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel

Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface × 7 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2N (R8A774Bx) block diagram



FC-BGA: 29 × 29mm² 1022-pins, 0.8mm pitch

RZ/G2E (R8A774C0)

CPU core
- Arm® Cortex®-A53, quad-core
  Max. operating frequency: 1.2GHz
- Arm® Cortex®-R7, single-core
  Max. operating frequency: 800MHz

Cache memory (Cortex®-A53)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 256KB

Cache memory (Cortex®-R7)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- I-TCM: 32KB
- D-TCM: 32KB

External memory
- Ability to connect DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 32 bits × 1channel

External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 8/16 bits
- PCI Express 2.0 : 1 Lane × 1 channel

3D graphics
- PowerVR™ GE8300

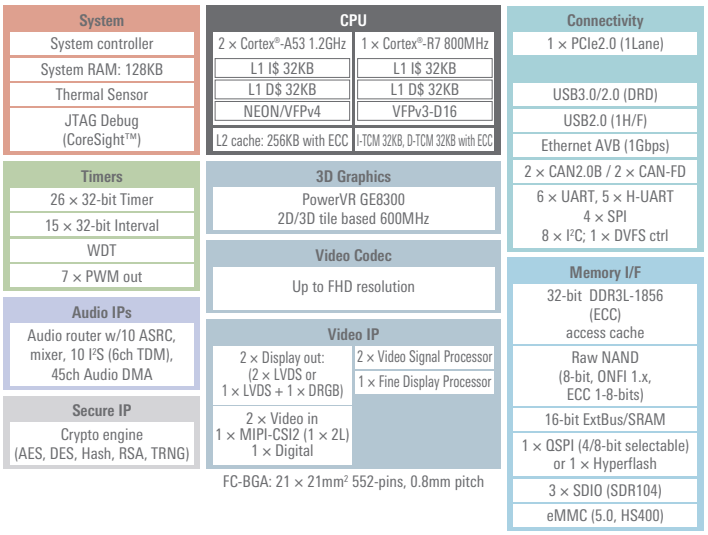
Video functions
- Video display interface × 2 channels (2 channels: LVDS, 1 channel: RGB888)
- Video input interface × 3 channels (1 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video codec module: VCP4 × 1 channel
- IP converter module
- Video image processing functions (color conversion, image enlargement/ reduction, filtering)

Audio functions
- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels

Storage interfaces
- USB 3.0 DRD × 1 channel
- USB 2.0 × 1 channel (Host-Function 1channel)
- SD host interface × 3 channels
- Multimedia card interface × 1 channel

Other peripheral functions
- 32-bit timer × 15 channels
- PWM timer × 7 channels
- I^2C bus interface × 8 channels
- Serial communication interface (SCIF) × 6 channels
- Quad serial peripheral interface (QSPI) × 2 channels (boot support)
- Clock-synchronous serial interface (MSIOF) × 4 channels (SPI/IIS support)
- Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
- Controller area network (CAN) interface × 2 channels
- Interrupt controller (INTC)
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2E (R8A774C0) block diagram



FC-BGA: 21 × 21mm² 552-pins, 0.8mm pitch

RZ/G2L(R9A07G044Lxx)

CPU core
- Arm® Cortex®-A55, dual-core or single-core
  Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core
  Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel

3D graphics
- Arm Mali™-G31 GPU

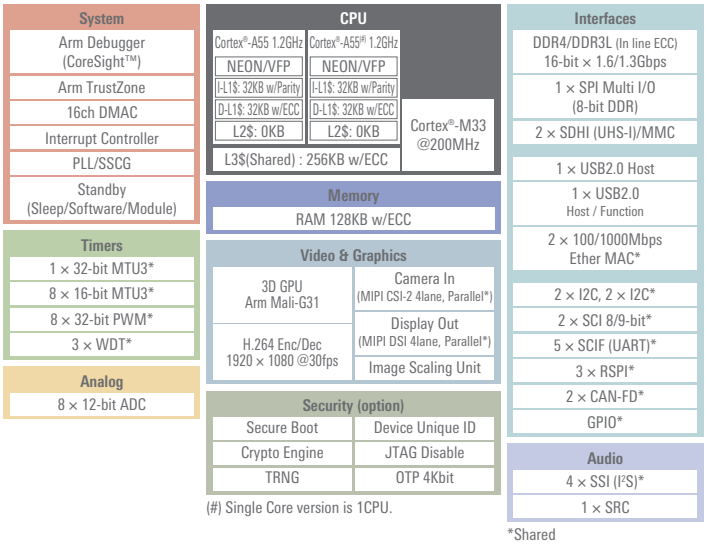
Video functions
- Video display interface: MIPI DSI × 1 channel or Digital parallel output × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel or Digital parallel input × 1 channel
- Video codec module: VCPL4 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions
- Sampling rate converter × 1 channel
- Serial sound interface × 4 channels

Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions
- 32-bit timer × 1 channel
- 16-bit timer × 8 channels
- PWM timer × 8 channels
- I^2C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (8bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 8 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2L(R9A07G044Lxx) block diagram



(#) Single Core version is 1CPU.

*Shared

RZ/G2LC(R9A07G044Cxx)

CPU core
- Arm® Cortex®-A55, dual-core or single-core
  Max. operating frequency: 1.2GHz
- Arm® Cortex®-M33, single-core
  Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel

3D graphics
- Arm Mali™-G31 GPU

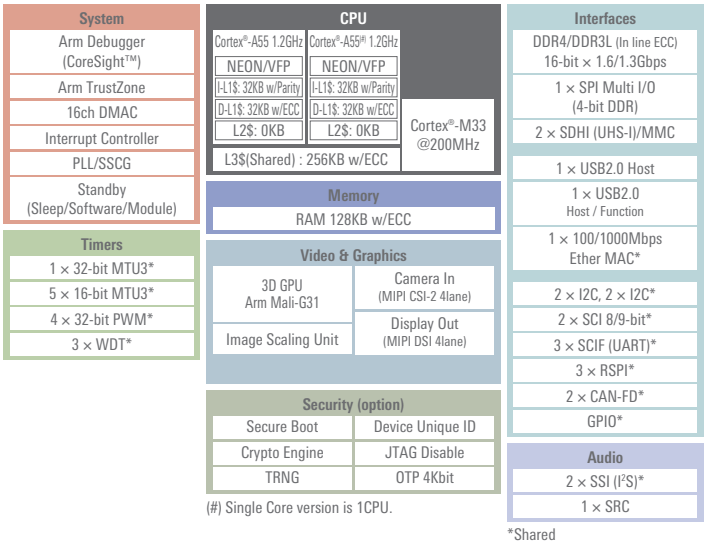
Video functions
- Video display interface:
  MIPI DSI × 1 channel
- Video input interface:
  MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions
- Sampling rate converter × 1 channel
- Serial sound interface × 2 channels

Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions
- 32-bit timer × 1 channel
- 16-bit timer × 5 channels
- PWM timer × 4 channels
- I^2C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 3 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 1 channel
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2LC(R9A07G044Cxx) block diagram



(#) Single Core version is 1CPU.

*Shared

RZ/G2UL(R9A07G043Uxx)

CPU core
- Arm® Cortex®-A55, single-core
  Max. operating frequency: 1.0GHz
- Arm® Cortex®-M33, single-core
  Max. operating frequency: 200MHz

Cache memory (Cortex®-A55)
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L3 cache: 256KB

External memory
- Ability to connect DDR4-SDRAM / DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel

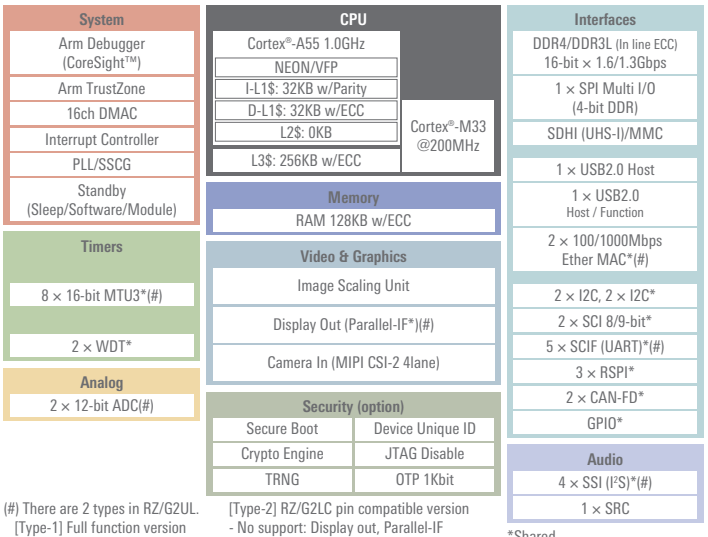
Video functions
- Video display interface:
  Digital parallel output × 1 channel
- Video input interface:
  MIPI CSI-2 × 1 channel
- Video image processing functions (Resizer and Color Space / Color Format Conversion)

Audio functions
- Sampling rate converter × 1 channel
- Serial sound interface × 4 channels

Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions
- 16-bit timer × 8 channels
- I^2C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller× 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) × 3channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/G2UL(R9A07G043Uxx) block diagram



(#) There are 2 types in RZ/G2UL.
[Type-1] Full function version
- This block diagram is Type-1.

[Type-2] RZ/G2LC pin compatible version
- No support: Display out, Parallel-IF
- 1×Ether MAC, 3×SCIF, 3×SSI

*Shared

RZ/Five [RISC-V] (R9A07G043Fxx)

CPU core
- 64bit RISC-V CPU Core AndesCore™ AX45MP Single core 1.0 GHz

Cache memory
- L1 Instruction Cache: 32K Byte
- L1 Data Cache: 32K Byte
- L2 Cache: 256K Byte

External memory
- Ability to connect DDR4-SDRAM /
- DDR3L-SDRAM via DDR dedicated bus
- Data bus width: 16 bits × 1 channel

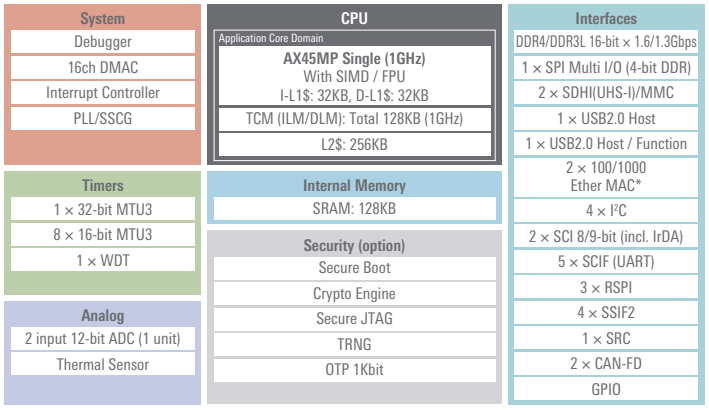
Audio functions
- Sampling rate converter × 1 channel
- Serial sound interface × 4 channels

Storage interfaces

Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface × 1 channel (Shared with SDHI)

Other peripheral functions
- 16-bit timer × 8 channels
- I^2C bus interface × 4 channels
- Serial communication interface with FIFO (SCIF) × 5 channels
- Serial communication interface (SCI) × 2 channels
- SPI Multi I/O Bus Controller × 1 channel (4bit Double data rate)
- Serial Peripheral Interface (RSPI) ×3 channels
- Gigabit Ethernet controller × 2 channels
- Controller area network (CAN) interface × 2 channels (support CAN FD)
- 12-bit A/D converter × 2 channels
- Interrupt controller
- Clock generator (CPG): on-chip PLL
- On-chip debug function

RZ/Five [RISC-V] (R9A07G043Fxx) block diagram



*: The 266-pin package has one channel of Gigabit Ethernet.

Package Information: 361-pin, 13 × 13mm PBGA (0.5mm pitch)
266-pin, 11 × 11mm PBGA (0.5mm pitch)

RZ/G Series Application

[HMI Application] The HMI can be made more expressive by making full use of the 3D graphics and video capabilities.


KIOSK/POS Terminal


Measuring Equipment


Inspection Device


Medical Display


Nurse Call System


CNC Equipment


Doorbell System


Multifunction Printer


Building Automation Control Panel


Digital Signage


Industrial Display


Surveillance Camera

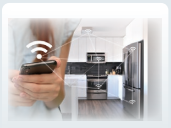

Handy Terminal


Home Security


Business Purpose Equipment

[IoT Application] Optimized for IoT devices by taking advantage of CPU performance, various interface functions, and security functions


Solar Inverter


Secure Home Gateway


EV Charger


Industrial Gateway


Infra Sensing Gateway

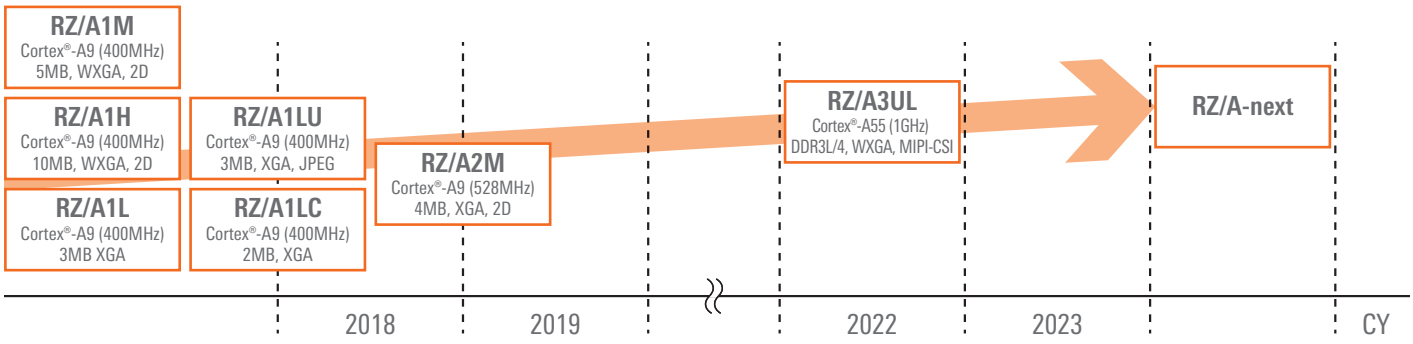

Smart Agriculture Gateway

RZ Partner Ecosystem Solutions

Visit the webpage below for the latest information on RZ partner ecosystem.
https://www.renesas.com/products/microcontrollers-microprocessors/rz-mpus/rz-partner-solutions

RZ/A Series

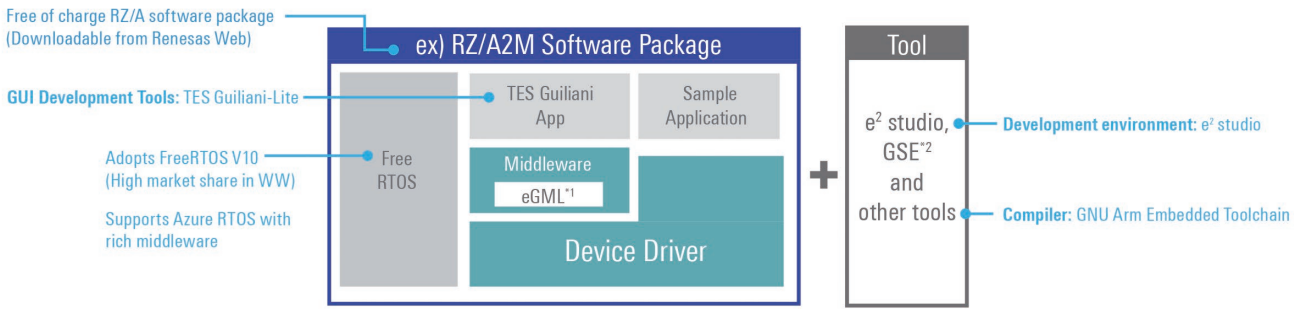
RZ/A Series Roadmap



RZ/A Series Application

Benefits of RZ/A Series — Develop like MCUs

RZ/A series MPUs retain the ease-of-use of Renesas MCUs due to rich integrated development environments, and deliver higher performance than MCUs.



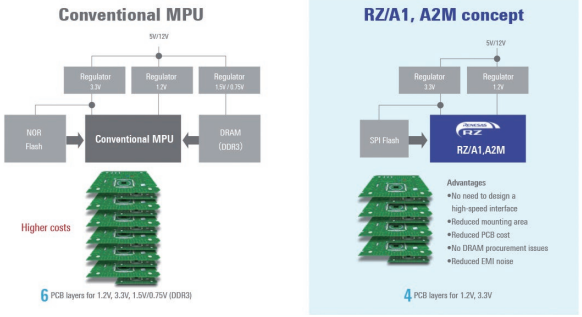
This is an example using Free RTOS.
*1: embedded Graphics Multiplatform Library
*2: Guiliani Streaming Editor

Benefits of RZ/A3UL

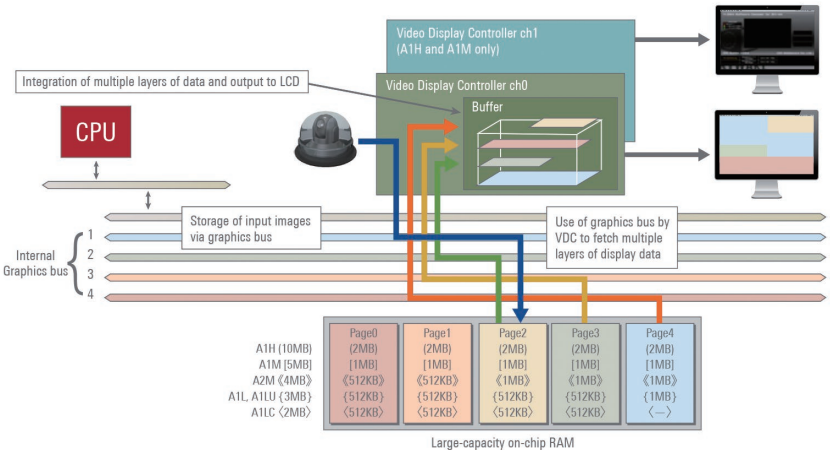
- 64bit CPU@1GHz RTOS MPU
- Choice of two memory I/Fs for different applications
  – Octal-SPI Flash/Octal-SPI RAM: For simple and low cost PCB design
  – DDR3L/DDR4: For high resolution HMI and camera use cases
- Pin-compatible RZ/A3UL (RTOS) and RZ/G2UL (Linux) for easy migration
  – The 361-pin package is pin-compatible between RZ/A3UL and RZ/G2UL

Benefits of RZ/A1 Group, and RZ/A2M MPUs

- Eliminate the need to design a high-speed interface
- Reduced mounting area
- Reduced PCB cost
- No DRAM procurement issues
- Reduced EMI noise



- Include on-chip graphics display and camera input capabilities



DRP Library

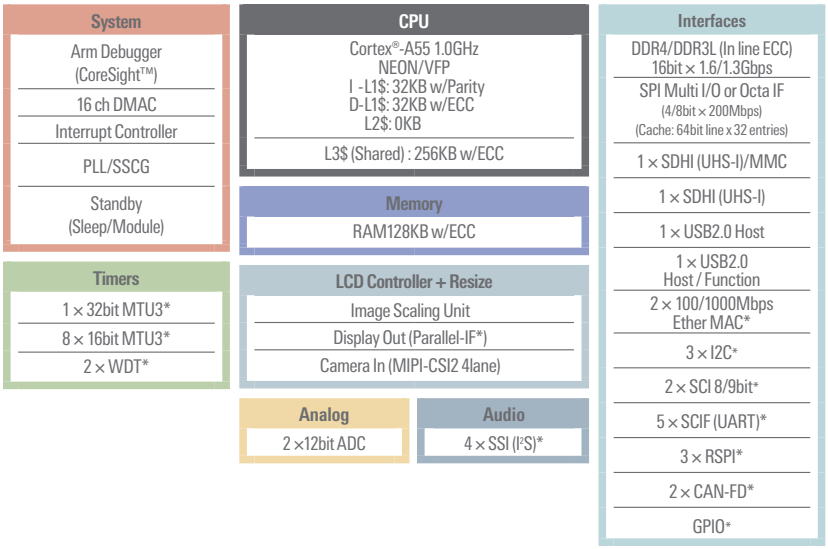
- RZ/A2M MPUs with DRP improve image processing performance by 10X over RZ/A1 MPUs
  – Dynamically Reconfigurable Processor (DRP) technology accelerates image processing
  – Enables hybrid e-AI solutions with DRP for image processing + CPU for inference

The RZ/A2M is designed around e-AI for smart appliances, network cameras, service robots, scanner products, and industrial equipment requiring high-speed image processing. The RZ/A2M combines a general-purpose MPU with Renesas' proprietary DRP technology for unique hybrid processing for image recognition and machine vision (MV), and AI processing works in conjunction with the Cortex®-A9, which pre-processes image data at high speed and extracts features for recognition target.

RZ/A3UL Group

- 64-bit Arm® Cortex®-A55 (1 GHz, single core)
- 16bit DDR3L/DDR4-1600 (in line ECC)
- Octal-SPI Flash/RAM IF
- Camera IF; MIPI-CSI2 (4 lanes)
- Display IF; Parallel RGB888/RGB666
- 2x Gigabit Ethernet
- 2x CAN (CAN-FD)
- 2x USB2.0 (Host, Host/Peripheral)
- 2x SDHI (UHS-I, UHS-I/MMC)

RZ/A3UL block diagram



* Shared

RZ/A2M Group

CPU (Arm® Cortex®-A9)
- Operating frequency: 528MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- 4MB

Main graphics and camera input functions
- Video display controller (VDC6): 1 channel
  LCD output: Max. WXGA
  Screen superimposition: 3 layers
  Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- MIPI-CSI2 interface: 1 channel
- Distortion compensation unit (IMR): 1 channel
- 2D graphics engine: 1 channel
- Sprite engine: 1 channel
- JPEG coding engine: 1 channel

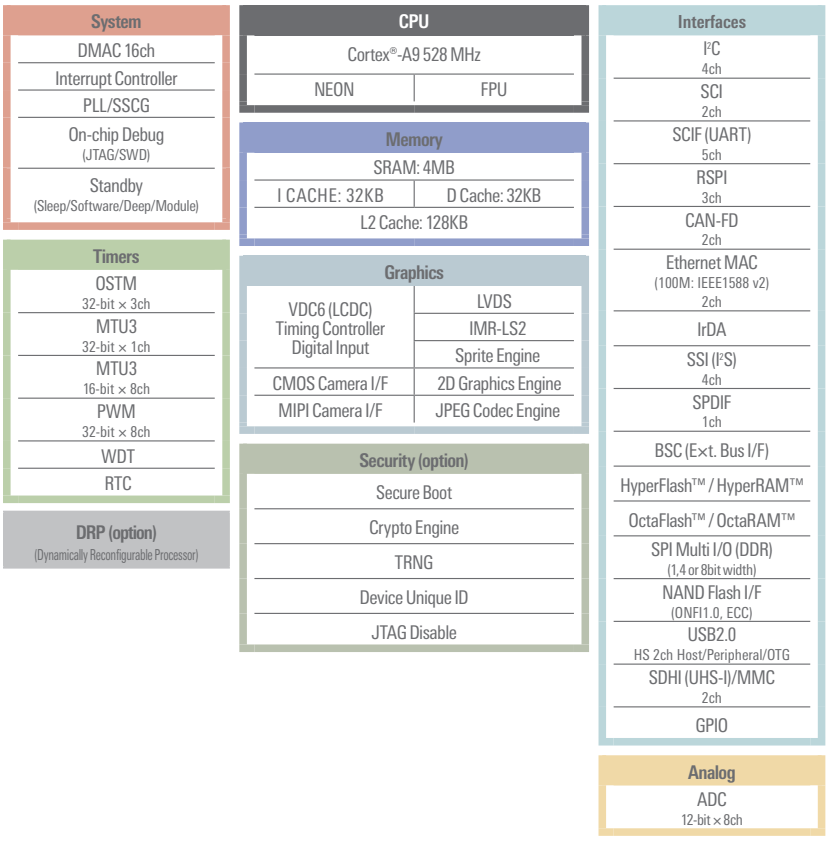
Main memory interface functions
- NOR flash, SDRAM, NAND flash
- Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)
- SD/MMC host interface: 2 channels

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I^2C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels

Optional functions
- DRP (Dynamically Reconfigurable Processor)

Package
- 176-LFBGA (13mm×13mm, 0.8mm pitch)
- 256-LFBGA (11mm×11mm, 0.5mm pitch)
- 272-FBGA (17mm×17mm, 0.8mm pitch)
- 324-FBGA (19mm×19mm, 0.8mm pitch)

RZ/A2M block diagram



RZ/A1H Group and RZ/A1M Group (Pin Compatible)

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- RZ/A1H: 10MB
- RZ/A1M: 5MB

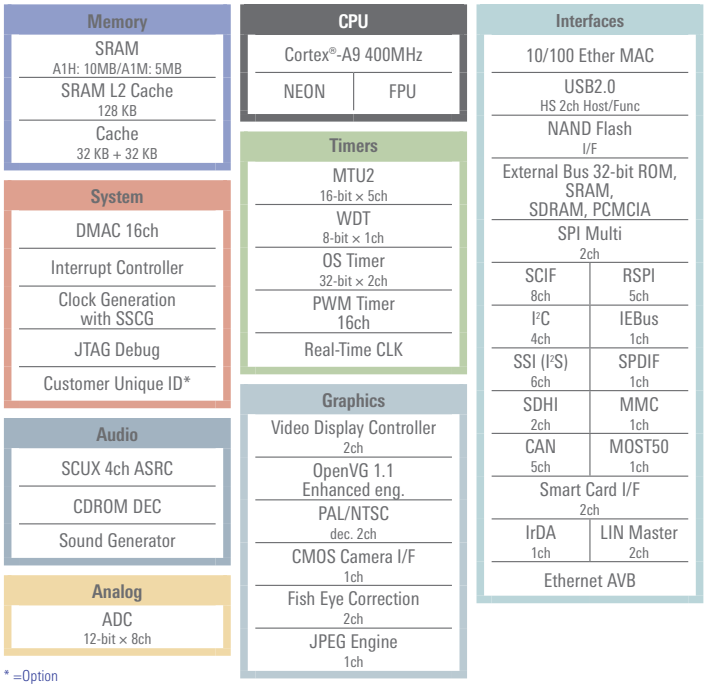
Main graphics and camera input functions
- Video display controller (VDC5): 2 channels
  LCD output: Max. WXGA
  Screen superimposition: 4 layers
  Video input: Max. XGA (CVBS analog input supported)
- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions
- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 2 channels (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 8 channels
- I^2C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

Package
- 256-LFBGA (11mm × 11mm,0.5mm pitch)
- 256-LFQFP (28mm × 28mm,0.4mm pitch)
- 324-FBGA (19mm × 19mm,0.8mm pitch)

RZ/A1H,and RZ/A1M block diagram



* =Option

RZ/A1LU Group

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- 3MB

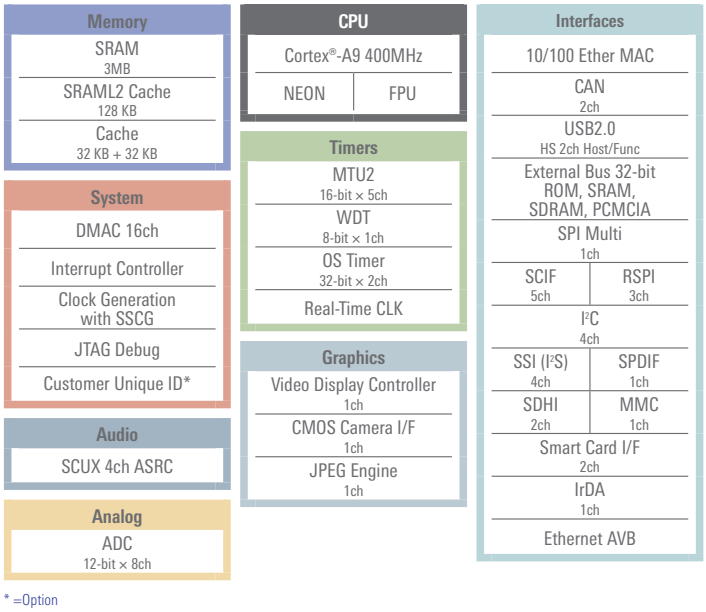
Main graphics and camera input functions
- LCD controller (VDC5): 1 channel
  LCD output: Max. WXGA
  Screen superimposition: 3 layers
  Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions
- NOR flash, SDRAM
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 5 channels
- I^2C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- Ethernet AVB: 1 channel
- CAN: 2 channels

Package
- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)

RZ/A1LU block diagram



* =Option

RZ/A1L, RZ/A1LC Group

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- RZ/A1L: 3MB
- RZ/A1LC: 2MB

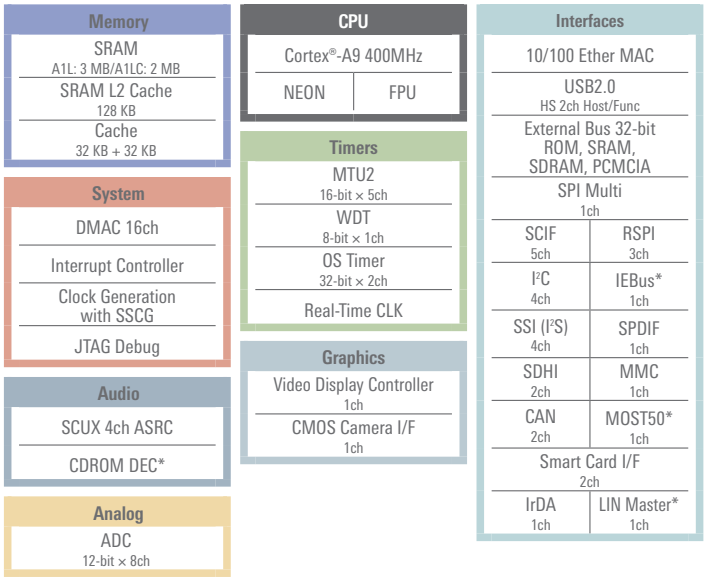
Main graphics and camera input functions
- LCD controller (VDC5): 1 channel
  LCD output: Max. WXGA
  Screen superimposition: 3 layers
  Video input: Max. XGA
- CMOS camera input (CEU): 1 channel

Main memory interface functions
- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I^2C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels

Package
- 176-LFBGA (8mm × 8mm,0.5mm pitch)
- 176-LFQFP (24mm × 24mm,0.5mm pitch)
- 208-LFQFP (28mm × 28mm,0.5mm pitch)
- 233-FBGA (15mm × 15mm, 0.8mm pitch)

RZ/A1L, RZ/A1LC block diagram



* RZ/A1L Group specification only.

RZ/A Series: Development Environments (Integrated Development Environments)

	RENESAS	arm	iar
Development environments	• e² studio*1 	• Arm® DS 	• IAR Embedded Workbench® for Arm® 
Compilers	• GNU Arm Embedded Toolchain	• Arm Compiler	• IAR C/C++ compiler*3
ICEs	• J-Link LITE from Segger • J-Link series from Segger*2 	• DSTREAM™ • ULINKpro™ • ULINKproD™ • ULINK2™ 	• I-jet™/I-jet Trace™ for Arm® Cortex®-A/R/M • JTAGjet-Trace 

*1: Eclipse-based development environment from Renesas (https://www.renesas.com/e2studio)
*2: Renesas does not handle ICEs from Segger. Contact a sales agent for details.
*3: A free evaluation license is available provided the 14-day time-limited evaluation or the code size-limited evaluation.

RZ/A Series: Development Tools (Debuggers, ICEs)

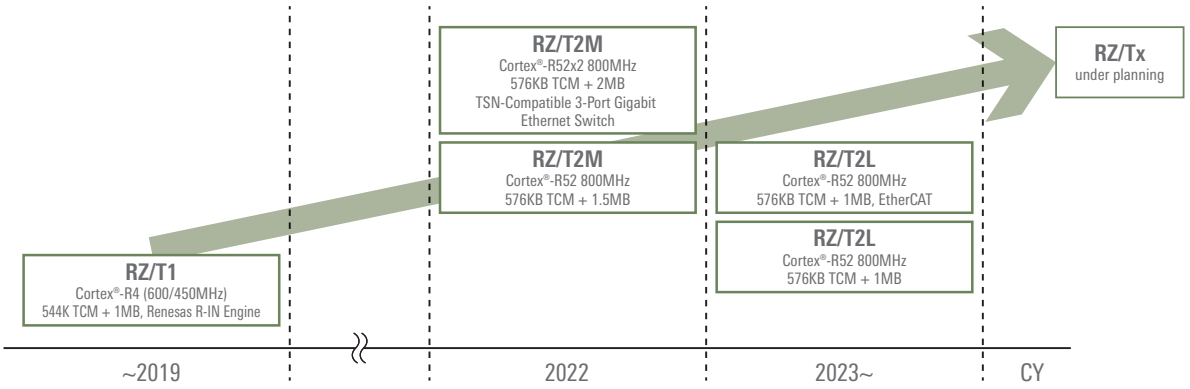
	KUC Kyoto Microcomputer Co., Ltd.	SEGGER	LAUTERBACH DEVELOPMENT TOOLS
Debuggers	• PARTNER-Jet2 	• Ozone • e² studio	• PowerView 
ICEs		• J-Link Series 	• PowerDebug 
Supported compilers	• exeGCC from Kyoto Microcomputer • GNU Arm Embedded Toolchain • Arm compiler • IAR C/C++ compiler, etc.	• GNU Arm Embedded Toolchain • Arm compiler • IAR C/C++ compiler, etc.	• GNU Arm Embedded Toolchain • Arm compiler • IAR C/C++ compiler, etc.

RZ/A Series: Solutions from Partner Companies

Visit the webpage below for the latest information on RZ/A Series development tools, including solutions from partner companies.
https://www.renesas.com/products/microcontrollers-microprocessors/rz-mpus/rz-partner-solutions

RZ/T Series

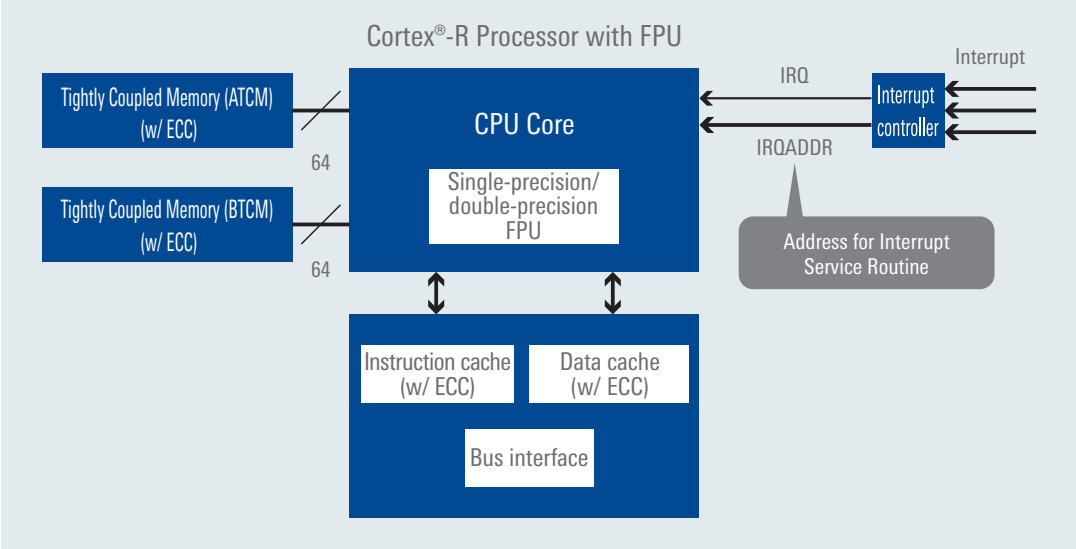
RZ/T Series Roadmap



RZ/T Series Features

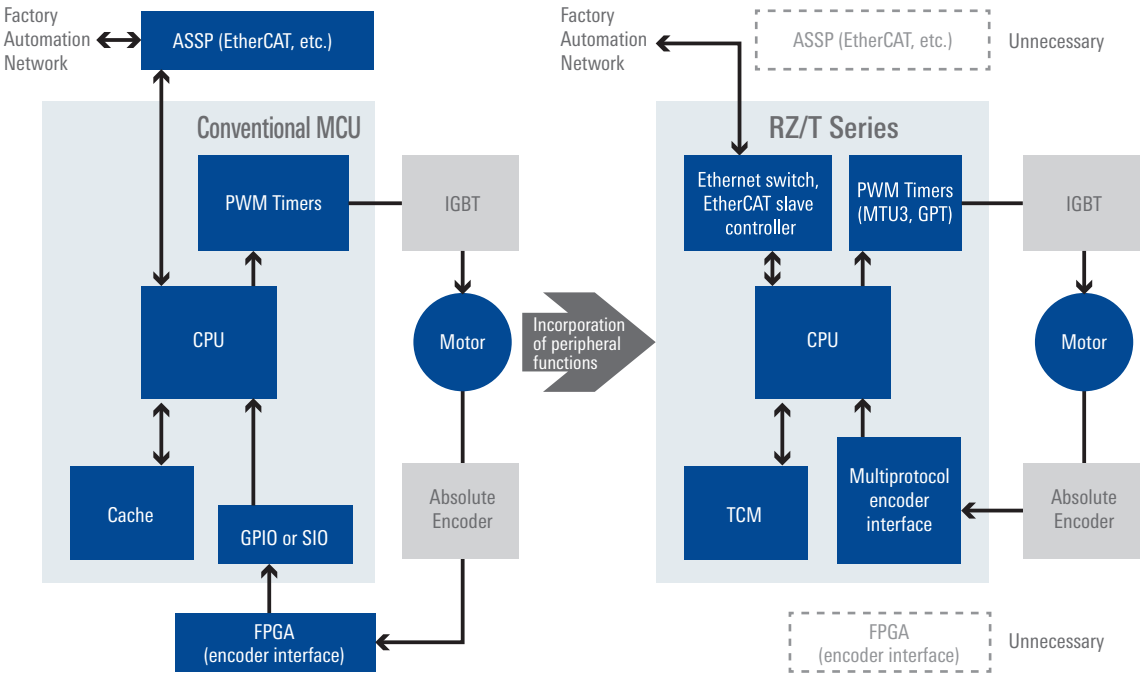
- High-performance, high-speed real-time control
- Integrated peripheral functions

High-performance, high-speed real-time control



- High-speed RAM directly coupled to the CPU allows fast processing and bypassing of the cache for reliable real-time responsiveness.
- ECC for enhanced reliability
- Assures responsive interrupt handling suitable for embedded control applications.

Integrated peripheral functions



- Integrates communication ASSP that would previously have been implemented as an external device.
- Integrates encoder interface that would previously have been implemented by an FPGA or ASIC.

	EnDat 2.2	BiSS-C	NIKON A-format	FA-CODER	HIPERFACE DSL
Related specifications	Heidenhein Corp http://www.heidenhain.de	iC-Haus GmbH http://www.biss-interface.com	NIKON Corporation http://www.nikon.co.jp	TAMAGAWA SEIKI CO.,LTD. http://www.tamagawa-seiki.co.jp	SICK STEGMANN GmbH http://www.sick.com
Communication system	Clock synchronous	Clock synchronous	Asynchronous	Asynchronous	Asynchronous
Transmission link	RS-485	RS-422	RS-485	RS-485	RS-485
Supported frequencies/data transfer rates	100kHz to 16.7MHz	62.5kHz to 10MHz	2.5Mbps, 4Mbps, 6.67Mbps, 8Mbps, 16Mbps	2.5Mbps	9.375Mbps
I/O pin count/ signal level	4/3.3V TTL level	2 / 3.3V TTL level	3 / 3.3V TTL level	3 / 3.3V TTL level	3 / 3.3V TTL level
Compatible functions on T series	- Propagation delay function - Not supported for incremental signals	- Delay compensation function - Supported in C mode (not supported in B mode) - Not supported for incremental signals - Supported on 1-to-1 connections (not supported on bus connections)	- Supported on 1-to-1 connections and bus connections	- Baseband NRZ code support - Not supported for incremental signals or synchronous Manchester code	- External synchronous communication (sync mode) - Asynchronous communication (free running mode) - Estimator function (position estimation when error occurs) - RSSI, quality monitoring

RZ/T Series Application

A fast CPU operating at 300MHz to 800MHz and large-capacity tightly-coupled memory provide the high performance and advanced functionality required by industrial applications such as industrial motors or AC servo drives. The RZ/T series is powerful enough to handle Industrial Ethernet processing of various types while still maintaining real-time performance.


Industrial motors


Industrial controllers


Robots


Actuators

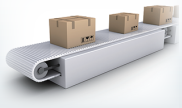

AC servo drivers


Medical Equipment


Elevator


Wind Turbine


Robot Gripper


Conveyor

RZ/T2M Group

CPU core
- Arm® Cortex®-R52 × 2
- Operating frequency: 800MHz/400MHz/200MHz
- Single-precision/double-precision floating-point unit

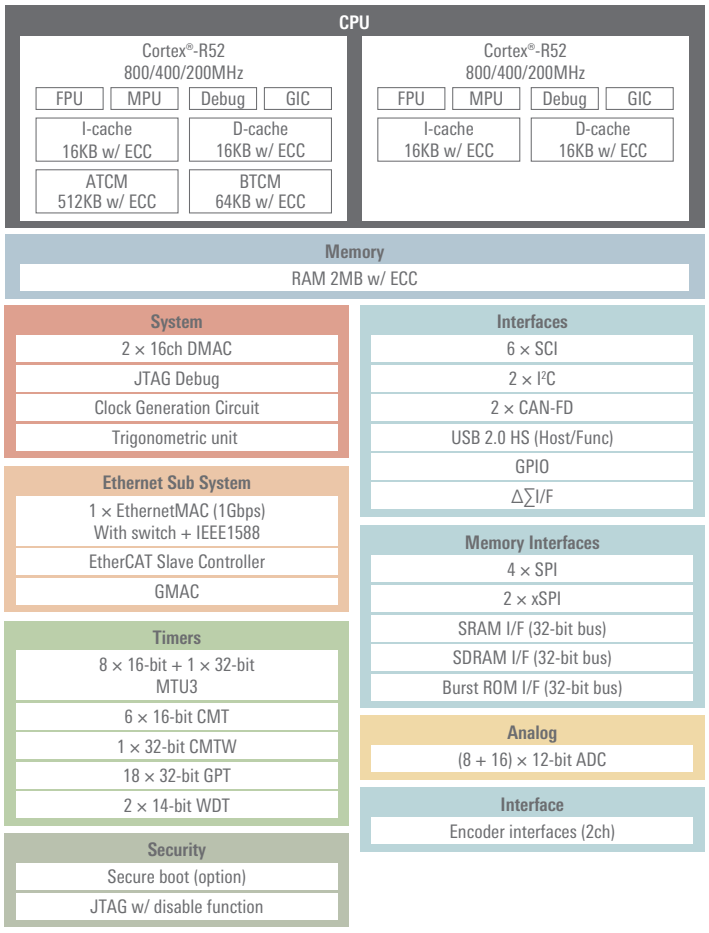
On-chip memory
- Tightly Coupled Memory: 512KB (W/ ECC) + 64KB (W/ ECC)
- 2MB on-chip RAM (with ECC)

Features
- Low latency peripheral port (LLPP) bus
- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT slave controller
- Encoder interface
- PWM timer
- ΔΣ interface
- ADC
- Trigonometric function unit
- xSPI
- CAN-FD
- USB2.0
- SPI, SCI, I^2C

Safety functions
- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Packages
- 320-pin FBGA (17mm × 17mm, 0.8mm pitch)
- 225-pin FBGA (13mm × 13mm, 0.8mm pitch)
- 176-pin LQFP (24mm × 24mm, 0.5mm pitch)
- 128-pin LQFP (14mm × 20mm, 0.5mm pitch)
- Tj = −45°C to +125°C

RZ/T2M Group block diagram



RZ/T2M Product Lineup

Security	R9A07G075M28GBG	R9A07G075M26GBG	R9A07G075M28GBA	R9A07G075M26GBA	R9A07G075M27GBA	—	R9A07G075M05GFP	R9A07G075M05GFA
Non-Security	R9A07G075M24GBG	R9A07G075M22GBG	R9A07G075M24GBA	R9A07G075M22GBA	—	R9A07G075M21GBA	R9A07G075M01GFP	R9A07G075M01GFA
CPU	Dual Cortex®-R52 (800+800MHz)						Single Cortex®-R52 (800MHz)	
System RAM	2.0MB wECC						1.5MB wECC	
TCM Memory	CPU0 : ATCM: 512KB wECC, BTCM: 64KB wECC CPU1 : ATCM: none, BTCM: none						CPU0 : ATCM: 512KB wECC, BTCM: 64KB wECC	
∑Δ interface	3ch × 2 units							
Encoder I/F Protocol	A-format™, BiSS-C, EnDat2.2, FA-CODER®, HIPERFACE DSL®							
Motor Control Peripherals	PWM Timer (MTU3, GPT), ∑Δ Interface, 12bit ADC, Encoder Interface, Trigonometric Accelerator							
Ethernet Port	3ports (100/1000Mbps)				None			
EtherCAT Port	Max 3ports (Exclusive with Ethernet)				None			
Industrial Ethernet Protocol	EtherCAT®, PROFINET RT/IRT, EtherNet/IP™, CC-Link IE Basic, TSN (IEC/IEEE 60802 Industrial Profile), OPC UA over TSN				None			
CAN	CAN FD ×2ch	Classic CAN ×2ch	CAN FD ×2ch	Classic CAN ×2ch	CAN FD ×2ch	Classic CAN ×2ch	Classic CAN ×2ch	Classic CAN ×2ch
Package	BGA320 (17mm×17mm, 0.8mm pitch)		BGA225 (13mm×13mm, 0.8mm pitch)				QFP176 (24mm×24mm, 0.5mm pitch)	QFP128 (14mm×20mm, 0.5mm pitch)
Power Supply	1.1V, 1.8V, 3.3V							
Operating Temperature	Tj = -40 to +125°C							

* More protocols will be supported in the future

RZ/T2L Group

CPU core
- Arm® Cortex®-R52
- Operating frequency: 800MHz/400MHz/200MHz
- Single-precision/double-precision floating-point unit

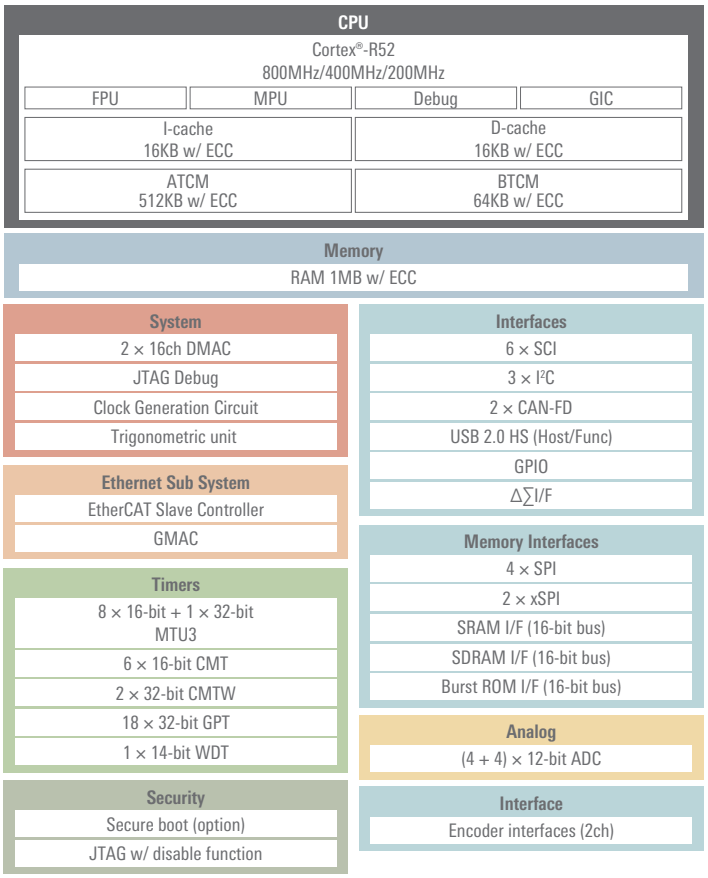
On-chip memory
- Tightly Coupled Memory: 512KB (W/ ECC) + 64KB (W/ ECC)
- 1MB on-chip RAM (with ECC)

Features
- Low latency peripheral port (LLPP) bus
- EtherCAT slave controller
- Gigabit Ether MAC
- Encoder interface
- PWM timer
- ΔΣ interface
- ADC
- Trigonometric function unit
- Serial host interface
- xSPI
- CAN-FD
- USB2.0
- SPI, SCI, I^2C

Safety functions
- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Packages
- FBGA 196pin (12mm × 12mm, 0.8mm pitch)
- Tj = −45°C to +125°C

RZ/T2L Group block diagram



RZ/T2L Product Lineup

Part Number	R9A07G074M08GBG	R9A07G074M05GBG	R9A07G074M04GBG	R9A07G074M01GBG
CPU	Cortex®-R52 (Max 800MHz)			
System RAM	1.0MB (w/ECC)			
TCM Memory	ATCM 512KB (w/ECC) / BTCM 64KB (w/ECC)			
External bus	8, 16 bit			
Peripheral functions for motor control	PWM Timer (MTU3, GPT), ADC, ⊿Σ interface, Trigonometric function unit			
GMAC	1 ch			
Ethernet Port	3 ports			
EtherCAT	Supported	Not Supported	Supported	Not Supported
CAN	CAN-FD	CAN	CAN-FD	CAN
Security	Supported	Supported	Not Supported	Not Supported
Package	BGA196 (12mm × 12mm, 0.8mm pitch)			
Power Supply	1.1V, s1.8V, 3.3V			
Operating Temperature	Tj = -40 to +125℃			

RZ/T1 Group

CPU core
- Arm® Cortex®-R4
- Operating frequency: 600MHz/400MHz/300Hz
- High-performance, high-speed real-time control
- Single-precision/double-precision floating-point unit

Renesas R-IN engine (“R-IN engine”)
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- R-IN engine instruction memory: 512KB (w/ ECC) + data memory: 512KB (w/ ECC)

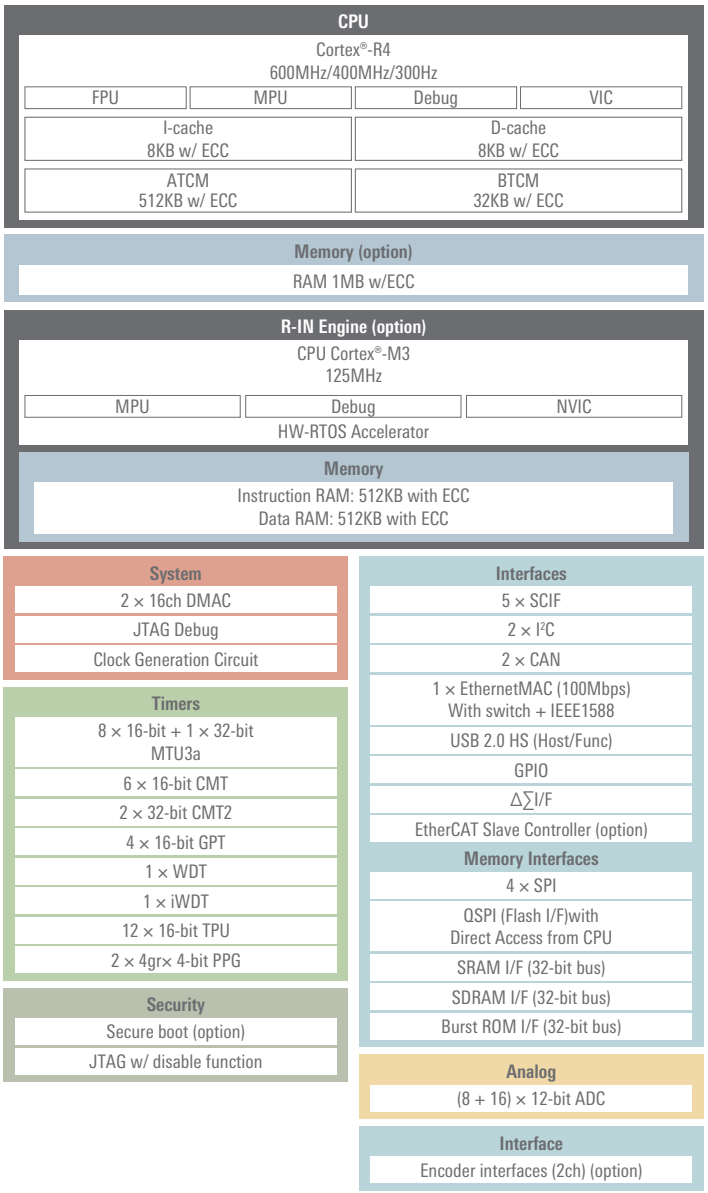
On-chip memory
- Tightly Coupled Memory: 512KB (w/ ECC) + 32KB (w/ ECC)
- Extended RAM instruction memory 512KB (w/ ECC) + data memory: 512KB (w/ ECC)

Features
- Industrial Ethernet communication accelerator with multi-protocol support (R-IN engine)
- EtherCAT slave controller
- PWM timer: MTU3a, GPT
- Encoder interface (Nikon A-format™/BiSS-C/EnDat2.2/HIPERFACE DSL®/ FA-CODER®)

Note: 2ch encoder support depends on the combination of the selected protocol.
- High Speed USB
- Secure boot (option)
- Safety functions
  – ECC memory
  – CRC (32-bit)
  – Independent WDT: Operating on dedicated on-chip oscillator
- ΔΣ interface
- 100Mbps EtherMAC (with Ethernet switch)
- Ethernet accelerator
- Power supply voltage: 1.2V, 3.3V

Package
- FBGA 320pin (17mm × 17mm, 0.8mm pitch)
- QFP 176pin (20mm × 20mm, 0.4mm pitch)
- Tj = –45°C to +125°C

RZ/T1 Group block diagram



RZ/T1 Product Lineup

CPU	Tightly coupled memory	Extended RAM							
600 MHz + R-IN Engine (150MHz)	512KB +32KB	– (1MB for R-IN)						R7S910017	R7S910018
450 MHz + R-IN Engine (150MHz)	512KB +32KB	– (1MB for R-IN)						R7S910015	R7S910016
600 MHz	512KB +32KB	1MB		R7S910007	R7S910013	R7S910027	R7S910028		
450 MHz	512KB +32KB	1MB		R7S910006		R7S910025	R7S910026		
		–	R7S910001	R7S910002	R7S910011				
300 MHz	512KB +32KB	–				R7S910035	R7S910036		
Package			176 QFP	320 BGA	320 BGA	320 BGA	320 BGA	320 BGA	320 BGA
Encoder I/F			–		Yes	–	Yes	–	Yes
Industrial Ethernet			– (Standard Ethernet)			EtherCAT		Multi-protocol support	

Utilizing the Arm® Ecosystem

■ Utilizing Renesas' Experience and the Arm® Ecosystem

Customers can benefit from solutions combining Renesas' accumulated experience in the microcontroller industry and the global ecosystem of Arm® partners. Products such as development environments, OS, and middleware are available from partner companies supporting the RZ/T series.

RZ/T Series: Development Environments (Integrated Development Environments)

	iar	RENESAS
Development environments	• IAR Embedded Workbench® for Arm® 	• e² studio*1 
Compilers	• IAR C/C++ compiler*2	• GNU tool*4
Other tools	• AP4 and FSP Smart Configurator code generation tools from Renesas can be used.	• Code generation function available as a plug-in.
ICEs	• I-jet™/I-jet Trace™ for Arm Cortex®-A/R/M • JTAGjet-Trace 	• J-Link LITE from Segger • J-Link series from Segger*5 

*1. Eclipse-based development environment from Renesas (http://renesas.com/e2studio)
*2. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)
*3. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*4. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
*5. Renesas does not handle ICEs from Segger. Contact a sales agent for details.

RZ/T Series: Development Tools (Debuggers, ICEs)

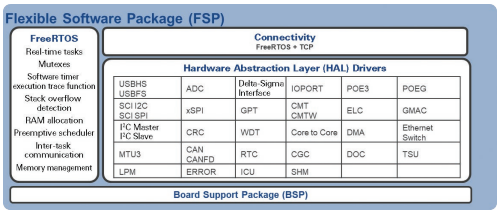
	KUC Kyoto Microcomputer Co., Ltd.	DTS INSIGHT Our insight, your value	LAUTERBACH DEVELOPMENT TOOLS	Computex
Debuggers	• PARTNER-Jet2 	• microVIEW-PLUS 	• TRACE32 PowerView 	• CSIDE version 7 
ICEs		• adviceLUNA II 	• TRACE32 PowerDebug & PowerTrace 	• PALMiCE4  JTAG model Large capacity trace model
Supported compilers	• exeGCC from Kyoto Microcomputer • GNU tool*1 • Arm CC*2 • IAR C/C++ compiler,*3 etc.	• Arm CC*2 • GNU tool,*1 etc.	• Arm CC*2 • GNU tool*1 • IAR C/C++ compiler*3 etc.	• Arm CC*2 • IAR C/C++ compiler*3 • GNU tool,*1 etc.
Supported product	RZ/T1, RZ/T2M		RZ/T1, RZ/T2M, RZ/T2L	RZ/T1

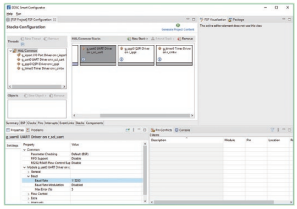
*1. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
*2. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*3. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)

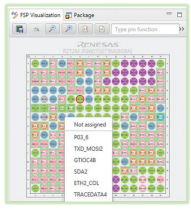
Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

(Supported product: RZ/T2M, RZ/T2L)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.
Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as IAR Embedded Workbench® for Arm from IAR Systems and e² studio.



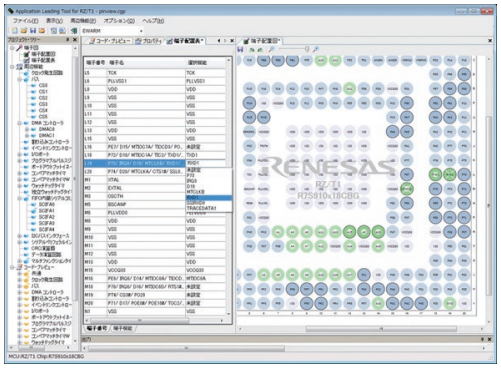


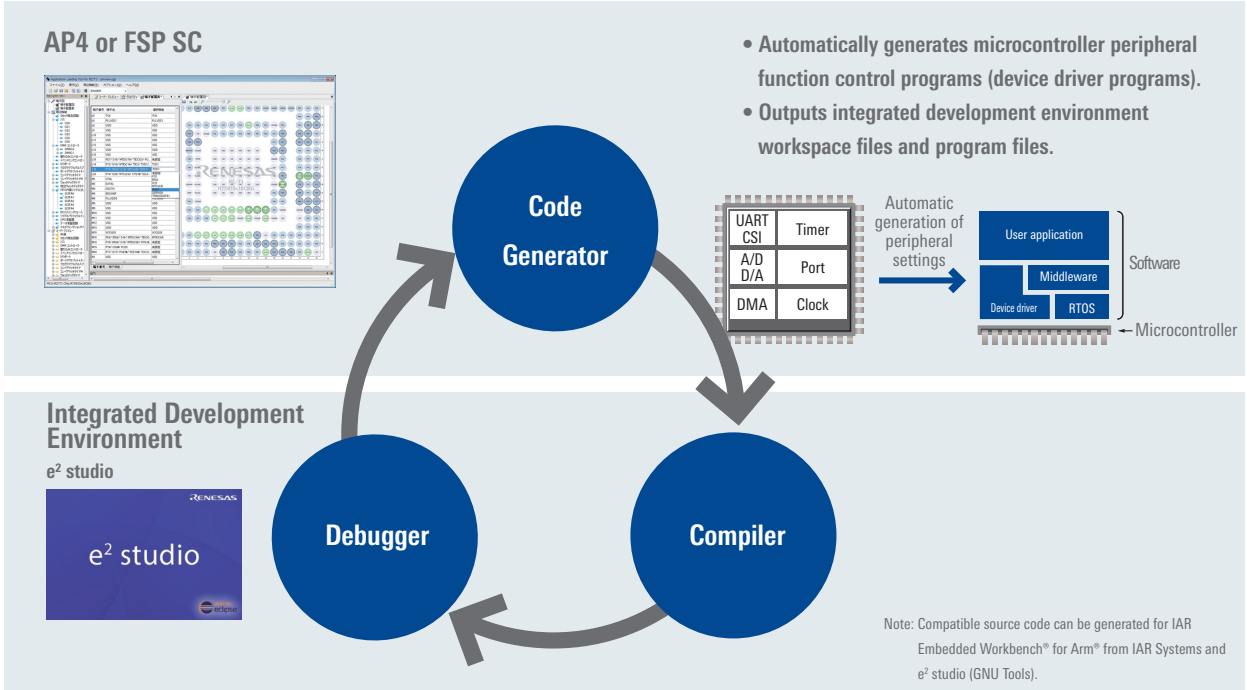


Code Generation Support Tool: AP4

(Supported product: RZ/T1)

AP4 is a standalone tool that automatically generates peripheral function control programs (device driver programs) based on settings entered by the user. The build tool (compiler) is selectable. This makes it possible to generate peripheral function control program code to match a specific build tool and enables interoperation with integrated development environments. (https://www.renesas.com/ap4)
The version of AP4 that is compatible with the RZ/T1 group can generate compatible source code for IAR Embedded Workbench® for Arm® from IAR Systems, Development Studio (DS-5™) from Arm®, and e² studio (GNU Tools).





RZ Ecosystem Solutions from Partner Companies

Visit the webpage below for the information on RZ/T series solutions from partner companies.
https://www.renesas.com/products/microcontrollers-microprocessors/rz-mpus/rz-partner-solutions

Renesas Starter Kit+ for RZ/T2M

https://www.renesas.com/rskrzt2m

- The board is mounted with a dual-core RZ/T2M with a 320BGA package and can be used to evaluate almost all of the device's functions.
- Emulator circuit is mounted, can start program debugging by simply connecting USB cable to PC.
- Ordering number: RTK9RZT2M0S00000BE

- 320-pin RZ/T2M MPU (R9A07G075M24GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod™, Grove®, QWIIC®, and mikroBUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.

Renesas Starter Kit+ for RZ/T2L

www.renesas.com/rskrzt2l

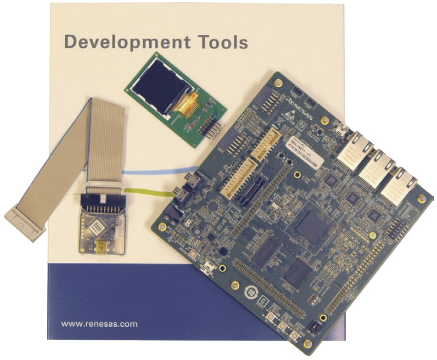
- Emulator circuit is mounted, can start program debugging by simply connecting USB cable to PC.
- Ordering number: RTK9RZT2L0S00000BJ

- 196-pin RZ/T2L MPU (R9A07G074M04GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod™, Grove®, QWIIC®, and mikroBUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.

RZ/T1-Starter-Kit-Plus

https://www.renesas.com/RZT1-Starter-Kit-Plus

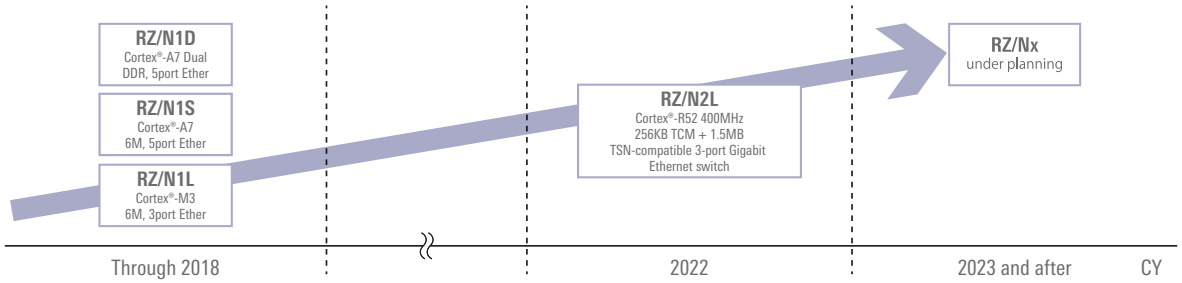
- The Renesas Starter Kit+ for RZ/T1 is the perfect starter kit for developers who are new to the RZ/T1.
- The kit includes an LCD display module, J-Link LITE debugging emulator, and e^2 studio integrated development environment so you can start evaluating the RZ/T1 immediately after opening the box.
- Ordering number: RTK7910018S01000BE



- RZ/T1 (R7S910018)
- QSPI FlashROM 64Mbyte
- SDRAM 64Mbyte × 2
- NOR Flash 64Mbyte × 2
- Rich interface
- Serial, USB, CAN
- Digilent Pmod I/F (PMOD connector)
- ΔΣ I/F (DSMI connector)
- Ethernet (10/100Base, EtherCAT) I/F etc.
- Audio codec
- Includes SEGGER's simple debug probe "J-Link LITE"
- Includes LCD for debugging

RZ/N Series

RZ/N Series Roadmap



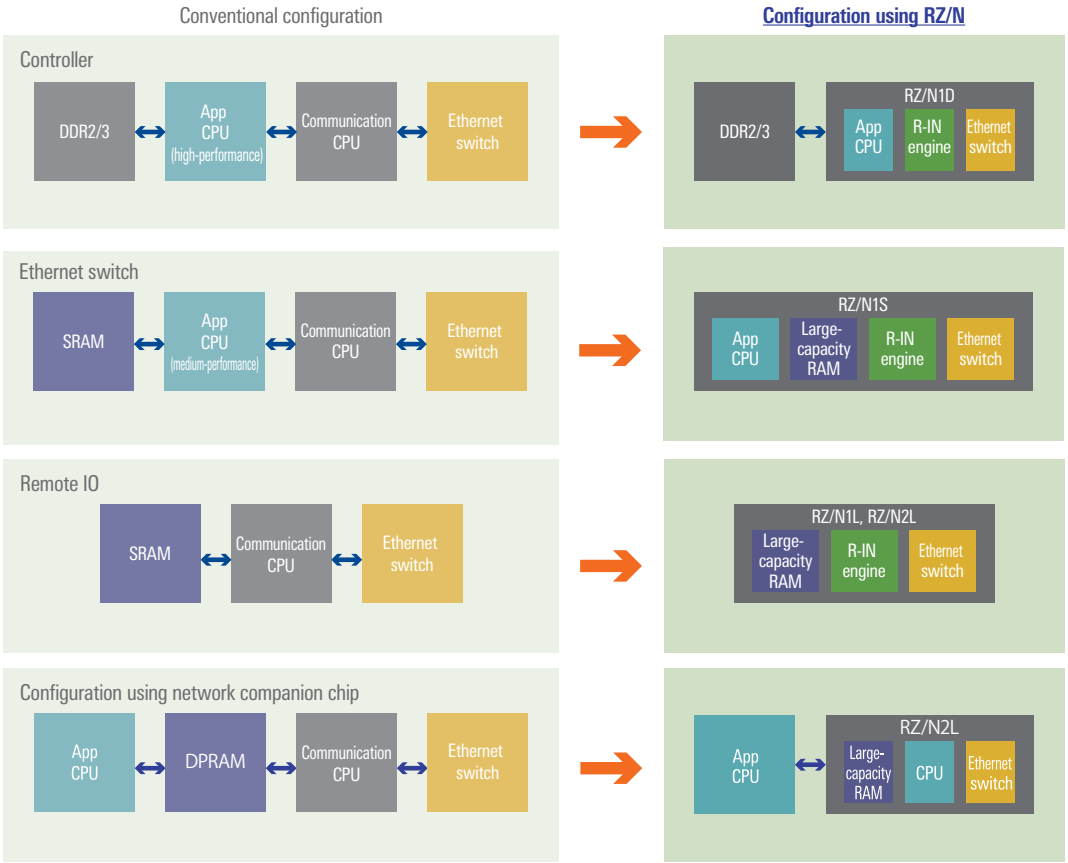
RZ/N Series Features

1. Provides optimized microcontrollers for a variety of industrial network applications
2. Integrated Ethernet switch and EtherCAT slave controller alongside support for major Industrial Ethernet protocols and TSN
3. Redundant network configuration reduces network downtime to zero

1. Provides optimized microcontrollers for a variety of industrial network applications

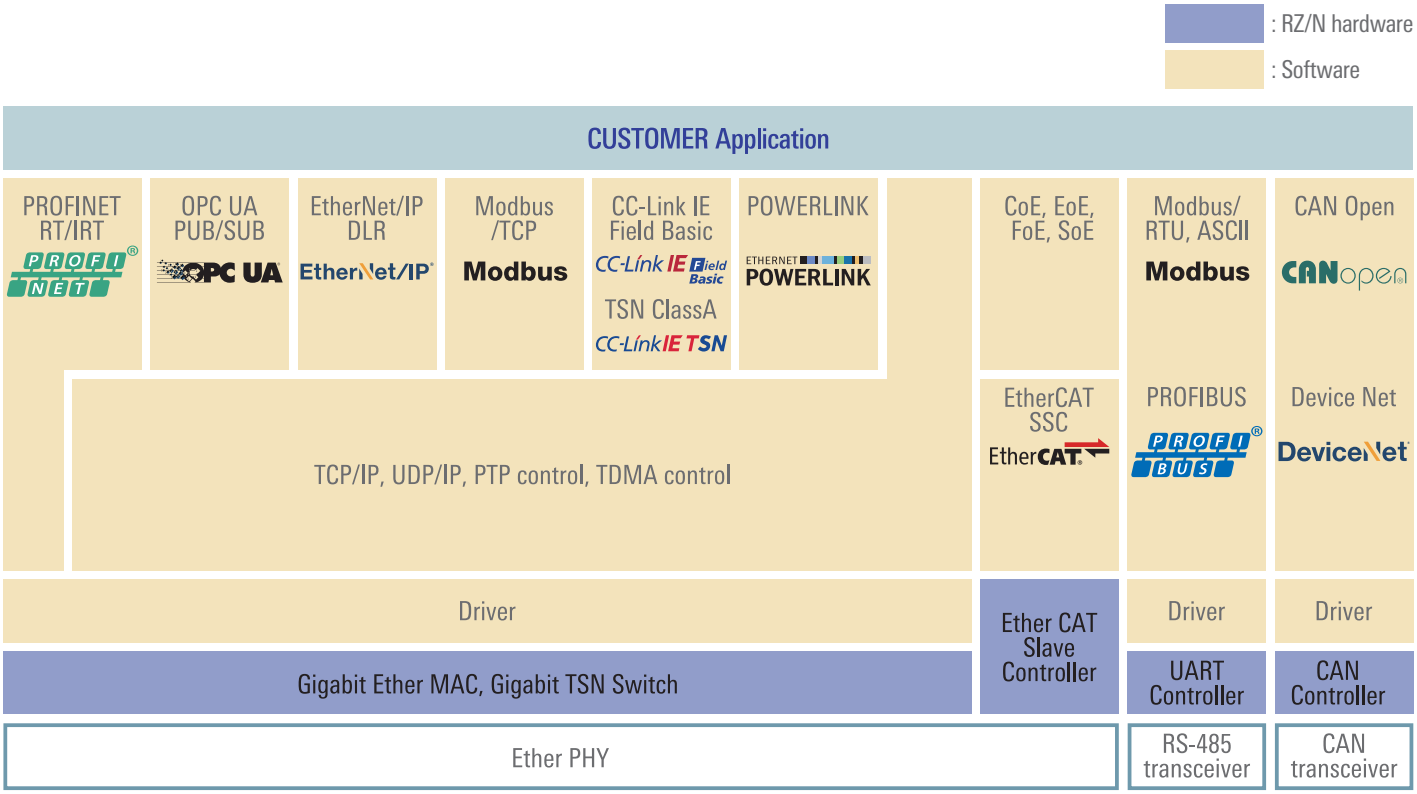
The RZ/N1 series lineup provides a choice of three CPU options and features the Renesas R-IN engine ("R-IN engine") and an on-chip 5-port Gigabit Ethernet switch, making it ideal for a variety of industrial network applications. Integrating the functionality of a communication CPU and key peripheral components helps reduce the BOM cost.

The RZ/N2L is optimized for the role of dedicated network companion chip, simplifying the task of adding network functionality to industrial equipment. Since it handles network-related processing independently of the external CPU, Industrial Ethernet support can be implemented without the need to make major changes to the existing application software.



2. Integrated Ethernet switch and EtherCAT slave controller alongside support for major Industrial Ethernet protocols and TSN

A wide range of Industrial Ethernet protocols are supported. Separating application processing and network processing allows for more efficient application control.



3. Redundant network configuration reduces network downtime to zero

Advanced redundant network configuration support helps eliminate network downtime.

— Redundant network connections: Parallel Redundancy Protocol (PRP)

— Looped network connections: HSR (High-availability Seamless Redundancy), DLR (Device Level Ring), RSTP (Rapid Spawning Trees)

RZ/N Series Application

PLC industrial controllers

Industrial switches

Sensor hubs

Gateways

Communication modules

Remote I/O

RZ/N2L Group

CPU core
- Arm® Cortex®-R52
- Operating frequency: 400MHz/200MHz
- Single-precision/double-precision floating-point unit

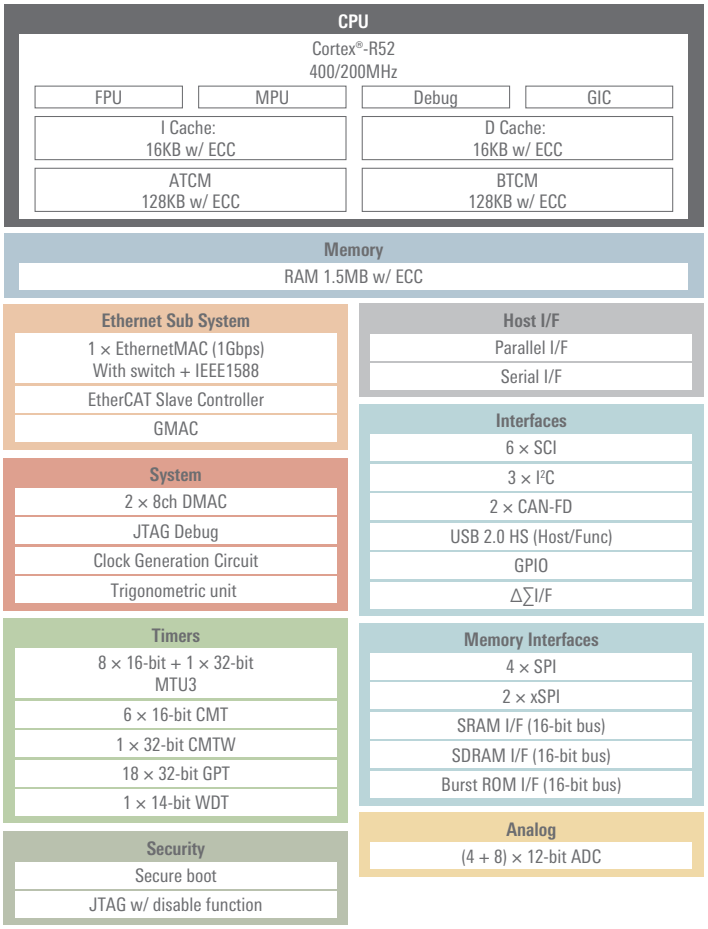
On-chip memory
- Tightly Coupled Memory: 128KB (w/ ECC) + 128KB (w/ ECC)
- 1.5MB on-chip RAM (with ECC)

Features
- TSN support
- 3-port Gigabit Ethernet switch
- EtherCAT slave controller
- Parallel host/serial host interface
- PWM timer
- ΔΣ interface
- ADC
- Trigonometric function unit
- CAN-FD
- USB2.0
- SPI, SCI, I²C
- xSPI

Safety functions
- Register write protection, input clock oscillation stop detection, and CRC
- Isolated peripheral function access via MPU

Packages
- 225-pin FBGA (13mm × 13mm, 0.8mm pitch)
- 121-pin FBGA (10mm × 10mm, 0.8mm pitch)
- Tj = −45°C to +125°C

RZ/N2L Group block diagram



RZ/N2L Product Lineup

Part Number		R9A07G084M08GBG	R9A07G084M04GBG	R9A07G084M08GBA	R9A07G084M04GBA
CPU		Cortex®-R52 (Max 400MHz)			
Tightly Coupled Memory		ATCM 128KB (w/ECC) / BTCM 128KB (w/ECC)			
RAM		1.5MB (w/ECC)			
External bus		8, 16bit		Not Supported	
Host I/F	Serial Host	OSPI/QSPI		QSPI	
	Parallel Host	8, 16bit		Not Supported	
Industrial Ethernet Protocol		EtherCAT®, PROFINET RT/IRT, EtherNet/IP™, TSN (IEC/IEEE 60802 Industrial Profile), CC-Link IE Field Basic, OPC UA over TSN			
Ether Port		3 ports		2 ports	
Motor Control Peripherals		PWM Timer (MTU3, GPT), ADC*, ΣΔ Interface, Trigonometric function unit			
Security		Supported	Not Supported	Supported	Not Supported
Power		1.1V, 1.8V, 3.3V			
Operating Temperature		Tj = -40 to +125°C			
Package		FBGA		FBGA	
Pin Count		225pin		121pin	
Package Information		13mm × 13mm, 0.8mm pitch		10mm × 10mm, 0.8mm pitch	

* 225pin only

RZ/N1D Group

CPU core
- Arm® Cortex®-A7 dual-core processor
- Operating frequency: 500MHz

Cache memory
- L1 I-cache: 16KB × 2, D-cache: 16KB × 2
- L2: 256KB

Internal memory
- 2MB (ECC)

External memory
- DDR2/DDR3 controller
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions
- EtherCAT slave controller
- Sercos® III slave controller
- HSR switch (400-pin)
- 5-port Ethernet switch

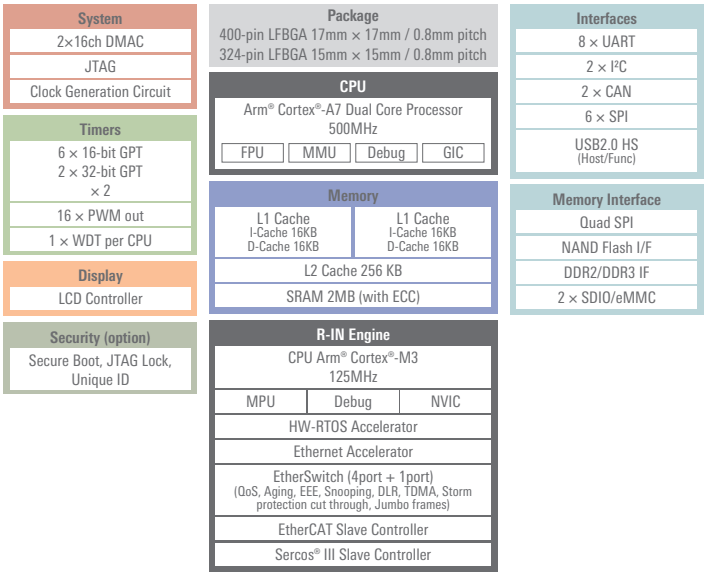
Other communication functions
- UART × 8 channels
- I^2C × 2 channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN

Other functions
- LCD controller
- ADC: 12-bit × 8 channels × 2 units (400-pin)
- ADC: 12-bit × 8 channels × 1 unit (324-pin)
- PWM timer, GPT

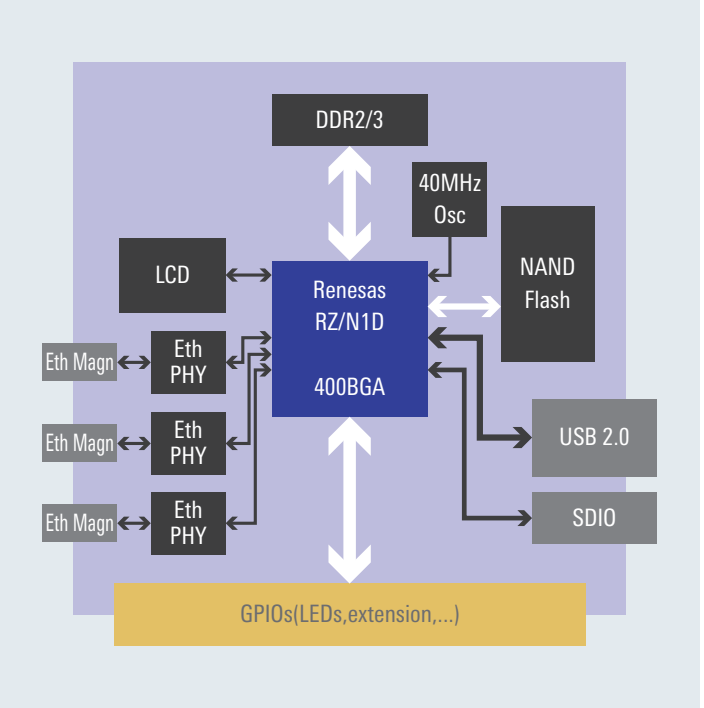
Package
- 400-pin: LFBGA, 17 × 17mm, 0.8mm pin pitch
- 324-pin: LFBGA, 15 × 15mm, 0.8mm pin pitch

Operating temperature
- Tj = −40°C to +110°C

RZ/N1D Group block diagram



Application example: Programmable logic controller block diagram



RZ/N1S Group

CPU core
- Arm® Cortex®-A7 single-core processor
- Operating frequency: 500MHz

Cache memory
- L1 I-cache: 16KB, D-cache: 16KB
- L2: 128KB

Internal memory
- 6MB (ECC)

External memory
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

R-IN engine
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Main Ethernet communication functions
- EtherCAT slave controller
- Sercos® III slave controller
- 5-port Ethernet switch

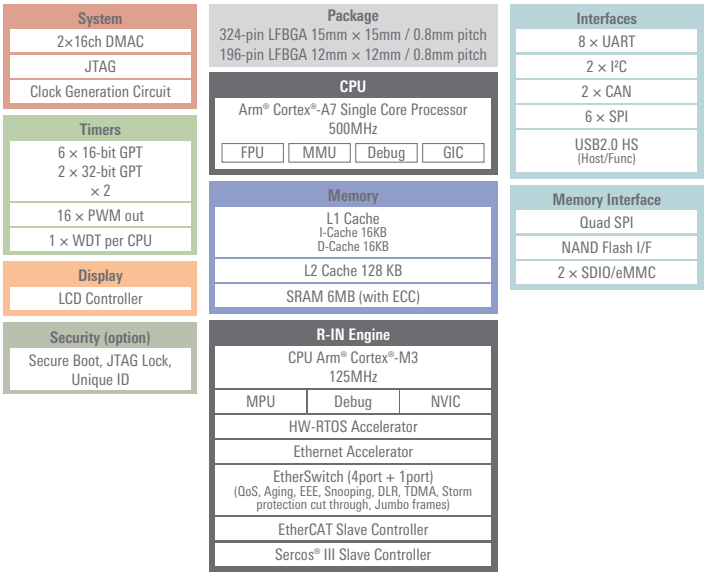
Other communication functions
- UART × 8 channels
- I^2C × 2 channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN

Other functions
- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

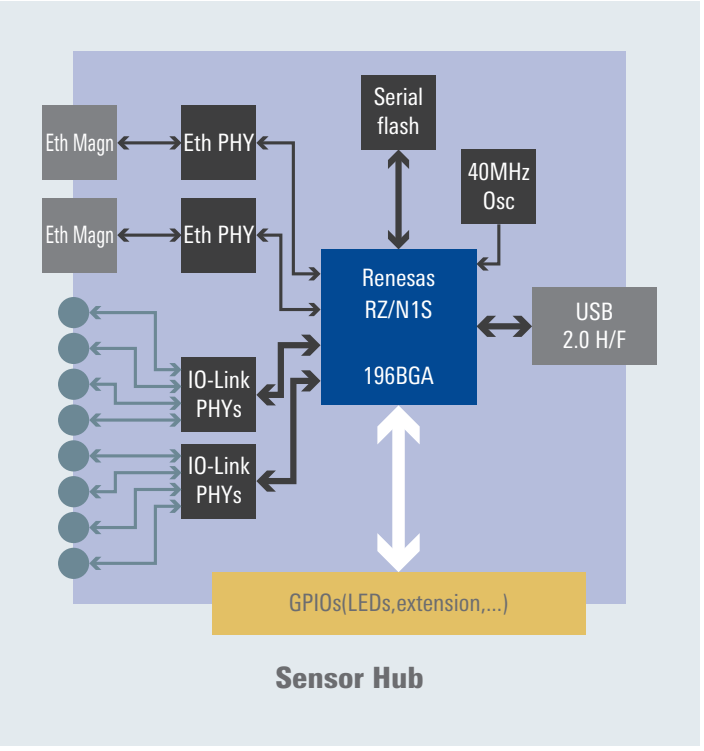
Package
- 324-pin: LFBGA, 15 × 15mm, 0.8mm pin pitch
- 196-pin: LFBGA, 12 × 12mm, 0.8mm pin pitch

Operating temperature
- Tj = −40°C to +110°C

RZ/N1S Group block diagram



Application example: Sensor Hub block diagram



RZ/N1L Group

R-IN engine
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

Internal memory
- 6MB (ECC)

External memory
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

Main Ethernet communication functions
- EtherCAT slave controller
- Sercos® III slave controller
- GbE Ethernet switch

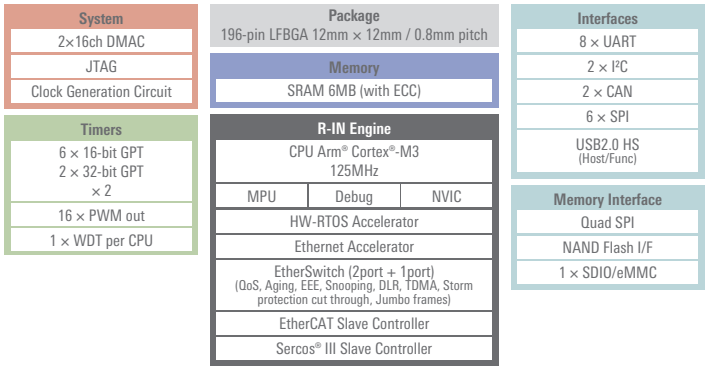
Other communication functions
- UART × 8 channels
- I^2C × 2 channels
- USB Host/Function × 1 channel, Host 1 channel
- SPI × 6 channels (master × 4 channels, slave × 2 channels)
- CAN × 2 channels

Other functions
- LCD controller
- ADC: 12-bit × 8 channels × 1 unit
- PWM timer, GPT

Package
- 196-pin: LFBGA, 12 × 12mm, 0.8mm pin pitch

Operating temperature
- Tj = −40°C to +110°C

RZ/N1L Group block diagram



RZ/N2L: Development Environments (Integrated Development Environments)

	IAR	RENESAS
Development environments	• IAR Embedded Workbench® for Arm® 	• e² studio*1 
Compilers	• IAR C/C++ compiler*2	• GNU tool*4
Other tools	• AP4 and FSP Smart Configurator code generation tools from Renesas can be used.	• Code generation function available as a plug-in.
ICEs	• I-jet™/I-jet Trace™ for Arm Cortex®-A/R/M • JTAGjet-Trace 	• J-Link LITE from Segger • J-Link series from Segger*5 

*1. Eclipse-based development environment from Renesas (http://renesas.com/e2studio)
*2. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)
*3. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*4. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
*5. Renesas does not handle ICEs from Segger. Contact a sales agent for details.

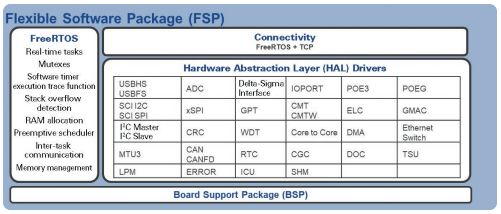
RZ/N2L: Development Tools (Debuggers, ICEs)

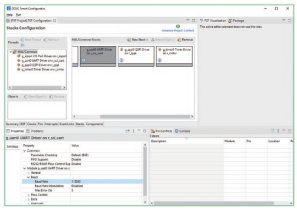
	Kyoto Microcomputer Co., Ltd.	DTS INSIGHT Our insight, your value	LAUTERBACH DEVELOPMENT TOOLS
Debuggers	• PARTNER-Jet2 	• microVIEW-PLUS 	• TRACE32 PowerView 
ICEs		• adviceLUNA II 	• TRACE32 PowerDebug & PowerTrace 
Supported compilers	• exeGCC from Kyoto Microcomputer • GNU tool*1 • Arm CC*2 • IAR C/C++ compiler,*3 etc.	• Arm CC*2 • GNU tool,*1 etc.	• Arm CC*2 • GNU tool*1 • IAR C/C++ compiler*3 etc.

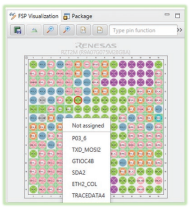
*1. GNU TOOLS & SUPPORT Website (https://llvm-gcc-renesas.com/)
*2. Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*3. Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (https://www.iar.com/EWARM)

Code Generation Support: Flexible Software Package (FSP) + Smart Configurator (SC)

The FSP includes everything you'll need to start developing software: board-dependent programs, peripheral function drivers, middleware, and documentation on how to use them.
Smart Configurator is a utility based on the concept of "combining software components freely." The intuitive GUI makes it easy to configure pins and FSP driver settings and to generate source code customized for your use case. It works together with integrated development environments such as IAR Embedded Workbench® for Arm from IAR Systems and e² studio.







Renesas Starter Kit+ for RZ/N2L

https://www.renesas.com/rskrzn2l

- The board is mounted with a RZ/N2L with a 225BGA package and can be used to evaluate almost all of the device's functions.
- Emulator circuit is mounted, can start program debugging by simply connecting USB cable to PC.
- Ordering number: RTK9RZN2L0S00000BE

- 225-pin RZ/N2L MPU (R9A07G084M04GBG)
- Gigabit Ethernet PHY
- Octal flash memory
- Pmod™, Grove®, QWIIC®, and mikroBUS™ connectors
- Pin header for external expansion
- Includes a USB power cable that can also be used to connect an emulator.

CONNECT IT! ETHERNET RZ/N

https://www.renesas.com/RZN-YConnect-It

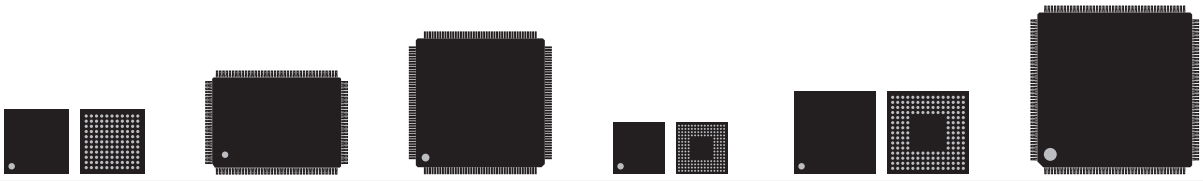
- CONNECT IT! ETHERNET RZ/N is the perfect solution kit for developers new to developing with the RZ/N1.
- The kit comes with not only an evaluation board, but also a JTAG emulator and various sample software.
- It is possible to evaluate master communication / slave communication of industrial networks.

- JTAG emulator
  - IAR I-jet Lite (20-pin flat ribbon/USB cable)
- 2 USB cables
- Startup manuals
- Pin setting tool
- RZ/N Solution Kit DVD
  - User's manual
  - OS (Linux, ThreadX®(Evaluation version), HW-RTOS)
  - Software PLC Codesys
  - Protocol stacks

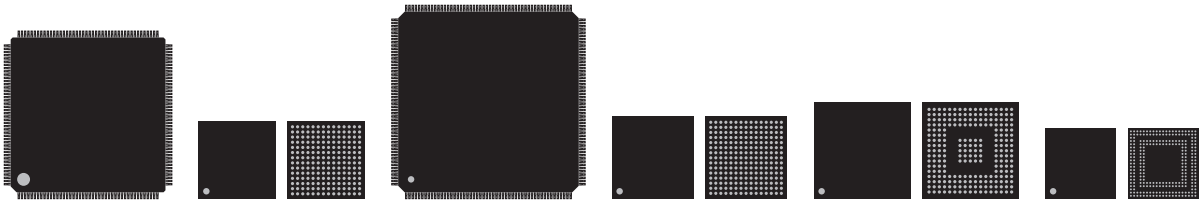
RZ Ecosystem Solutions from Partner Companies

Visit the webpage below for the information on RZ/N series solutions from partner companies.
https://www.renesas.com/products/microcontrollers-microprocessors/rz-mpus/rz-partner-solutions

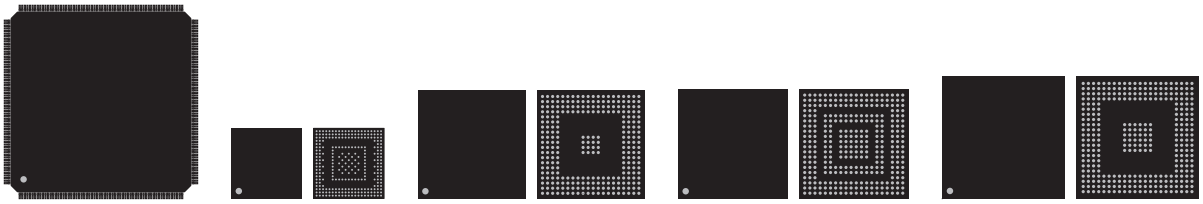
RZ Family Package Lineup



Pin-type:	121-LFBGA	128-LFQFP	176-HLQFP	176-LFBGA	176-LFBGA	176-LFQFP
Size:	10 x 10 mm	14 x 20 mm	20 x 20 mm	8 x 8 mm	13 x 13 mm	24 x 24 mm
Pitch:	0.80 mm	0.50 mm	0.40 mm	0.50 mm	0.80 mm	0.50 mm
Thickness:	1.40 mm	1.60 mm	1.70 mm	1.40 mm	1.40 mm	1.60 mm
Group:	RZ/N2L	RZ/T2M	RZ/T1	RZ/A1L, A1LC, A1LU	RZ/A2M	RZ/T2M

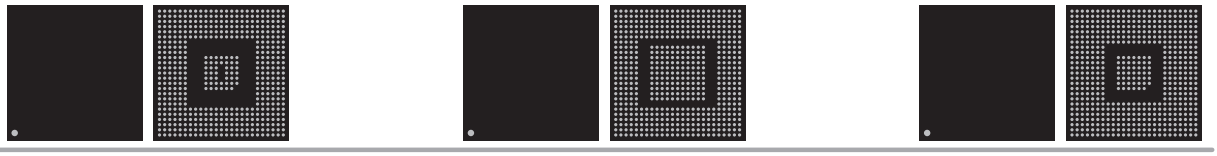


Pin-type:	176-LFQFP	196-LFBGA	208-LFQFP	225-LFBGA	233-FBGA	256-LFBGA
Size:	24 x 24 mm	12 x 12 mm	28 x 28 mm	13 x 13 mm	15 x 15 mm	11 x 11 mm
Pitch:	0.50 mm	0.80 mm	0.50 mm	0.80 mm	0.80 mm	0.50 mm
Thickness:	1.70 mm	1.70 mm	1.70 mm	1.40 mm	1.9 mm	1.40 mm
Group:	RZ/A1L, A1LU	RZ/N1L, N1S, RZ/T2L	RZ/A1L, A1LU	RZ/T2M, RZ/N2L	RZ/A1LU	RZ/A2M, A1H, A1M

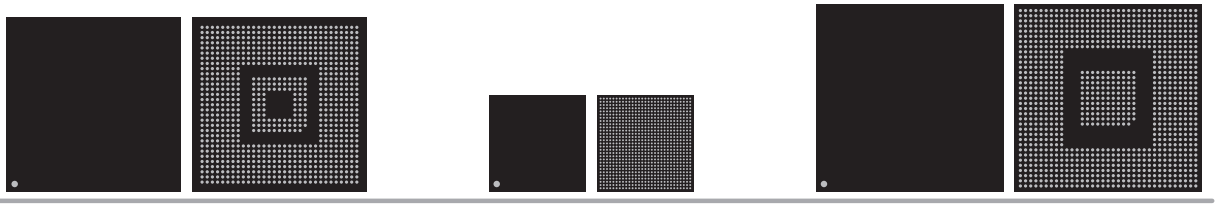


Pin-type:	256-LFQFP	266-LFBGA	272-FBGA	320-FBGA		324-FBGA
Size:	28 x 28 mm	11 x 11 mm	17 x 17 mm	17 x 17 mm		19 x 19 mm
Pitch:	0.40 mm	0.50 mm	0.8 mm	0.80 mm		0.80 mm
Thickness:	1.70 mm	1.40 mm	1.90 mm	2.30 mm	1.40 mm	2.10 mm
Group:	RZ/A1H, A1M	RZ/Five	RZ/A2M	RZ/T1	RZ/T2M	RZ/A2M, A1H, A1M

Pin-type:	324-LFBGA	361-LFBGA	400-LFBGA	456-LFBGA
Size:	15 x 15 mm	13 x 13 mm	17 x 17 mm	15 x 15 mm
Pitch:	0.80 mm	0.50 mm	0.80 mm	0.50 mm
Thickness:	1.70 mm	1.40 mm	1.70 mm	1.40 mm
Group:	RZ/N1D, N1S	RZ/G2LC, G2UL, RZ/Five	RZ/N1D	RZ/G2L, V2L



Pin-type:	501-FBGA	551-LFBGA	552-FBGA
Size:	21 x 21 mm	21 x 21 mm	21 x 21 mm
Pitch:	0.80 mm	0.80 mm	0.80 mm
Thickness:	2.40 mm	1.40 mm	2.45 mm
Group:	RZ/G1E, G1C	RZ/G2L, V2L	RZ/G2E



Pin-type:	831-FBGA	841-FCBGA	1022-FBGA	
Size:	27 x 27 mm	15 x 15 mm	29 x 29 mm	
Pitch:	0.80 mm	0.50 mm	0.80 mm	
Thickness:	2.40 mm	1.90 mm ± 0.2 mm	2.5 mm	3.15 mm
Group:	RZ/G1H, G1M, G1N	RZ/V2M, RZ/V2MA	RZ/G2M, G2N	RZ/G2H

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(Rev.5.0-1 October 2020)

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Document No. R01CP0031EJ0900