TPS7B82-Q1 300-mA High-Voltage Ultralow-I_Q Low-Dropout Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C ≤ T_A ≤ 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Extended Junction Temperature Range: –40°C ≤ T_J ≤ 150°C
- Low Quiescent Current I_Q:
  - 300-nA Shutdown I_Q
  - 2.7 µA Typical at Light Loads
  - 5 µA Maximum at Light Loads
- 3-V to 40-V Wide V_{IN} Input Voltage Range With up to 45-V Transient
- Maximum Output Current: 300 mA
- 2% Output-Voltage Accuracy
- Maximum Dropout Voltage: 700 mV at 200-mA Load Current for Fixed 5-V Output Version
- Stable With Low-ESR (0.001-Ω to 5-Ω) Ceramic Output-Stability Capacitor (1 µF to 200 µF)
- Fixed 5-V and 3.3-V Output Voltage
- Thermal Resistance ($R_{\theta JA}$): 63.9°C/W
- Packages:
  - 8-Pin HVSSOP, $R_{\theta JA}$ = 63.9°C/W
  - 6-Pin WSON, $R_{\theta JA}$ = 72.8°C/W
  - 5-Pin TO-252, $R_{\theta JA}$ = 38.8°C/W

2 Applications

- Automotive Head Unit
- Powering MCUs and CAN/LIN Transceivers
- Telematics Control Unit
- Body Control Modules
- Always-ON Battery-Connected Applications
  - Gateway Applications
  - Remote Keyless Entry Systems

3 Description

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. It is especially necessary to have ultralow I_Q for always-on systems.

The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 40 V (45-V load dump protection). Operation down to 3 V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7-µA typical quiescent current at light load, this device is an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to 125°C and with junction temperatures from –40°C to 150°C. Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is well suited as a power supply for various automotive applications.

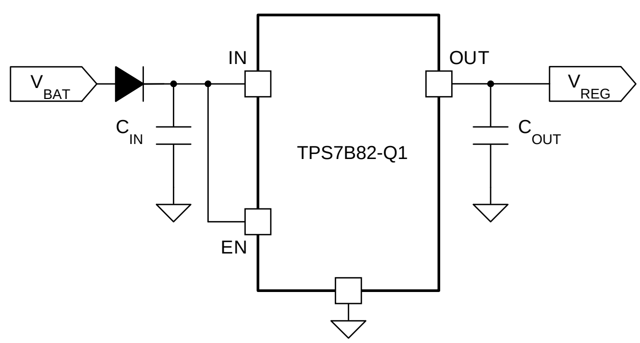
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B82-Q1	HVSSOP (8)	3.00 mm × 3.00 mm
	WSON (6)	2.00 mm × 2.00 mm
	TO-252 (5)(2)	6.10 mm × 6.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

Typical Application Schematic



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4 Revision History

Changes from Revision D (October 2018) to Revision E	Page
• Added KVU package to document as Preview device	1
• Changed DRV status from Preview to Production Data	1
• Added TO-252 sub-bullet and added $R_{\theta JA}$ values for HVSSOP and WSON sub-bullets in *Packages* bullet	1
• Added KVU to *Pin Configuration and Functions* section	4
• Changed *Electrical Characteristics* table	6
• Added second column in *Test Conditions* to call out device package differences	6

Changes from Revision C (February 2018) to Revision D	Page
• Added DRV package to document	1
• Changed *–40°C to 125°C* to *–40°C ≤ T_A ≤ 125°C* in first *AEC-Q100 Qualified* sub-bullet in *Features* section	1
• Changed *Extended Junction Temperature Range* bullet of *Features* section	1
• Changed first *Low Quiescent Current I_Q* sub-bullet in *Features* section	1
• Deleted *Integrated Fault Protection* bullet from *Features* section	1
• Added WSON to *Packages* bullet in *Features* section	1
• Changed MSOP to HVSSOP throughout document	1
• Changed first bullet in *Applications* section	1
• Added *Telematics Control Unit* bullet to *Applications* section	1
• Changed second paragraph of *Description* section	1
• Added DRV package to *Pin Configuration and Functions* section	4
• Changed maximum specification of second $I_{(Q)}$ parameter row from *5 µA* to *6.5 µA*	6
• Added first row and last three rows to $V_{(Dropout)}$ parameter	6
• Changed *Input Capacitor* section	12

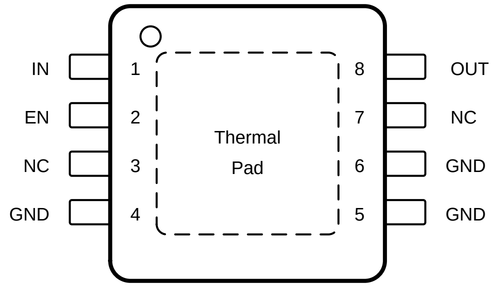
Changes from Revision B (February 2018) to Revision C	Page
• Added *Feature*: Device Junction Temperature Range: –40°C to 150°C	1
• Changed *Feature* From: Fixed 5-V Output Voltage To: Fixed 5-V and 3.3-V Output Voltage	1
• Added *Feature*: "Thermal Resistance ($R_{\theta JA}$): 63.9°C/W"	1
• Added "Powering MCUs and CAN/LIN Transceivers" to the *Applications* list	1
• Changed the *Description* section	1
• Changed the *Device Information* table	1
• Added PowerPAD to the DGN package description	4
• Changed pins 5 and 6 From: NC To: GND in the *Pin Configuration and Functions*	4
• Deleted Note 3 from V_{OUT} in the *Absolute Maximum Ratings*	5
• Changed the VALUE column for Output voltage From: 5 V To: 5 V or 3.3 V in Table 1	12

Changes from Revision A (November 2017) to Revision B	Page
• Deleted values from capacitors C_{IN} and C_{OUT} in the *Typical Application Schematic*	1
• Deleted values from capacitors C_{IN} and C_{OUT} in Figure 15	12

Changes from Original (September 2017) to Revision A	Page
• Deleted 2.5-V and 3.3-V device options from the *Features* list	1
• Changed V_{EN} to Enable input in the *Absolute Maximum Ratings*	5
• Deleted the blank NOM column from the *Recommended Operating Conditions* table	5
• Deleted requirements for 3.3-V and 2.5-V device versions from the *Electrical Characteristics* table	6
• Changed conditions for Figure 9	8
• Deleted 3.3-V and 2.5- output voltages from the *Design Requirements* table	12

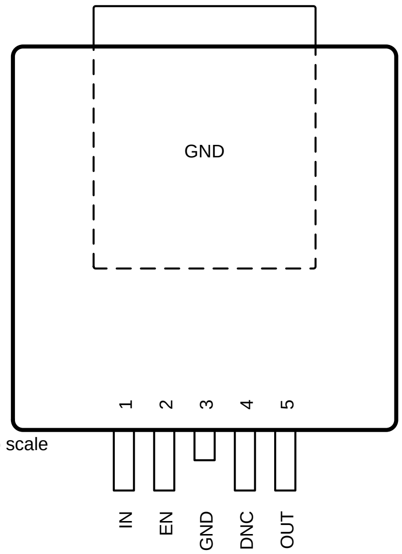
5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD™
Top View



Not to scale

KVU Package (Preview)
5-Pin TO-252
Top View



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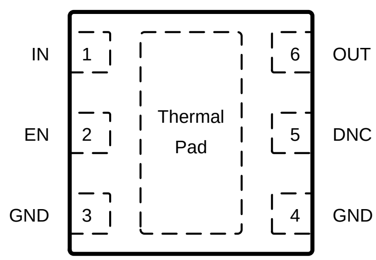
DRV Package
6-Pin WSON PowerPAD™
Top View



Not to scale

NC – No internal connection

Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	DGN	DRV	KVU		
DNC	—	5	4	—	Do not connect to a biased voltage. Tie this pin to ground or leave floating.
EN	2	2	2	I	Enable input pin
GND	4, 5, 6	3,4	3, TAB	—	Ground reference
IN	1	1	1	I	Input power-supply pin
NC	3, 7	—	—	—	Not internally connected
OUT	8	6	5	O	Regulated output voltage pin
Thermal pad				—	Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Unregulated input(3)	–0.3	45	V
V_{EN}	Enable input(3)	–0.3	V_{IN}	V
V_{OUT}	Regulated output	–0.3	7	V
T_J	Junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 45 V for 200 ms.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	3	40	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{OUT}	Output capacitor requirements(1)	1	200	µF
ESR	Output capacitor ESR requirements(2)	0.001	5	Ω
T_A	Ambient temperature range	–40	125	°C
T_J	Junction temperature range	–40	150	°C

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant ESR value at f = 10 kHz.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7B82-Q1			UNIT
		DGN (HVSSOP)	DRV (WSON)	KVU (TO-252)(2)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.9	72.8	38.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	85.8	46.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	37.4	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	2.7	10.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.3	37.3	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.1	13.8	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Preview package.

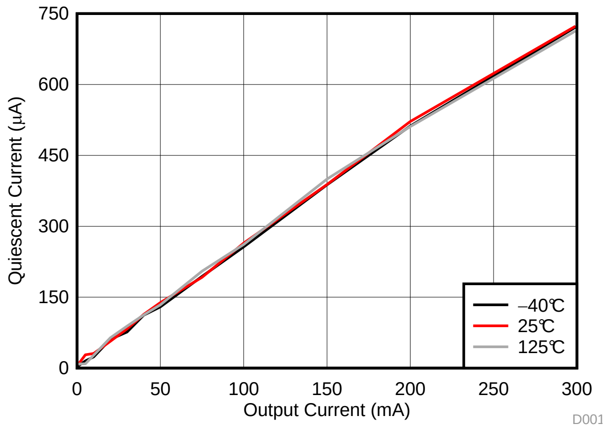
6.5 Electrical Characteristics

V_{IN} = 14-V, 10-µF ceramic output capacitor, T_J = –40°C to 150°C, over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)								
V_{IN}	Input voltage				$V_{OUT(NOM)}$ + $V_{(Dropout)}$		40	V
$I_{(SD)}$	Shutdown current	EN = 0 V				0.3	1	µA
$I_{(Q)}$	Quiescent current	V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0 mA		DRV and KVU packages		1.9	3.5	
				DGN package		1.9	5	µA
		V_{IN} = 6 V to 40 V, EN ≥ 2 V, I_{OUT} = 0.2 mA		DRV and KVU packages		2.7	4.5	
				DGN package		2.7	6.5	
$V_{(IN, UVLO)}$	V_{IN} undervoltage detection	Ramp V_{IN} down until the output turns OFF					2.7	V
		Hysteresis				200		mV
ENABLE INPUT (EN)								
V_{IL}	Logic-input low level						0.7	V
V_{IH}	Logic-input high level				2			V
REGULATED OUTPUT (OUT)								
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + $V_{(Dropout)}$ to 40 V, I_{OUT} = 1 mA to 300 mA		DRV and KVU packages	–1.5%		1.5%	
				DGN package	–2%		2%	
$V_{(Line-Reg)}$	Line regulation	V_{IN} = 6 V to 40 V, I_{OUT} = 10 mA					10	mV
$V_{(Load-Reg)}$	Load regulation	V_{IN} = 14 V, I_{OUT} = 1 mA to 300 mA		DRV and KVU packages			10	mV
				DGN package			20	
$V_{(Dropout)}$	Dropout voltage	$V_{OUT(NOM)}$ = 5 V	I_{OUT} = 300 mA	DRV and KVU packages		630	1170	mV
				DGN package			1000	
			I_{OUT} = 200 mA	DRV and KVU packages		420	780	
				DGN package		400	700	
			I_{OUT} = 100 mA	DRV and KVU packages		210	390	
				DGN package		200	350	
		V_{OUT} = 3.3 V	I_{OUT} = 300 mA	DRV and KVU packages		730	1350	
				DGN package			1250	
			I_{OUT} = 200 mA	DRV and KVU packages		475	900	
				DGN package			850	
			I_{OUT} = 100 mA				450	
I_{OUT}	Output current	V_{OUT} in regulation			0		300	mA
$I_{(CL)}$	Output current limit	V_{OUT} short to 90% × V_{OUT}			310	510	690	mA
PSRR	Power-supply ripple rejection	$V_{(Ripple)}$ = 0.5 V_{PP}, I_{OUT} = 10 mA, frequency = 100 Hz, C_{OUT} = 2.2 µF				60		dB
OPERATING TEMPERATURE RANGE								
$T_{(SD)}$	Junction shutdown temperature					175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown					20		°C

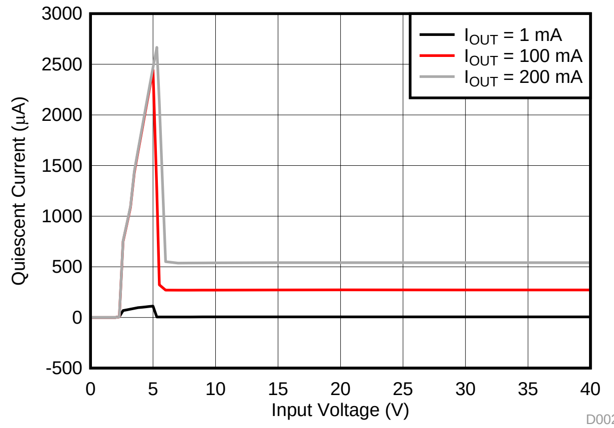
6.6 Typical Characteristics

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



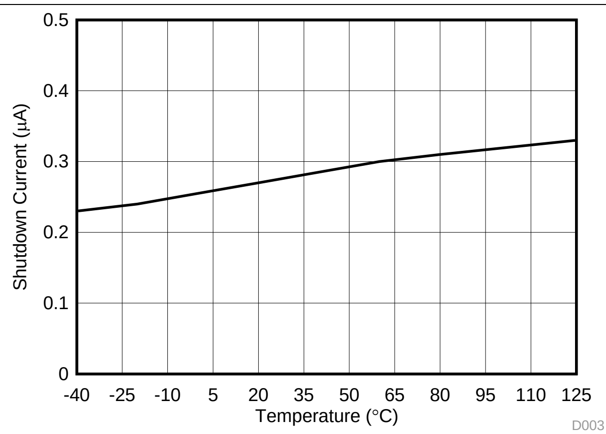
V_{OUT} = 5 V

Figure 1. Quiescent Current vs Output Current



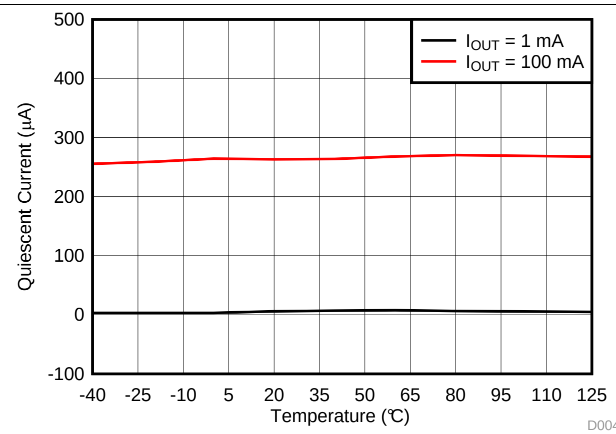
V_{OUT} = 5 V

Figure 2. Quiescent Current vs Input Voltage



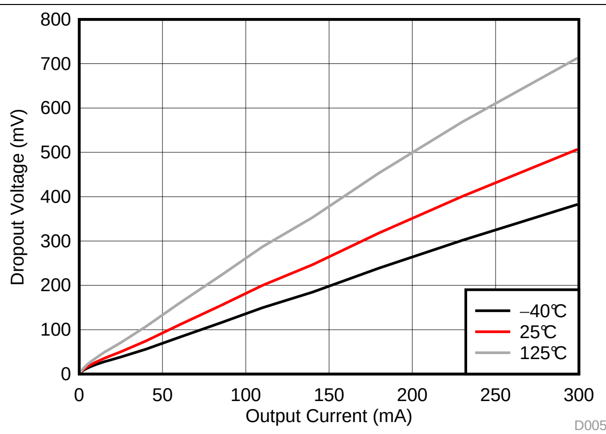
V_{EN} = 0 V

Figure 3. Shutdown Current vs Ambient Temperature



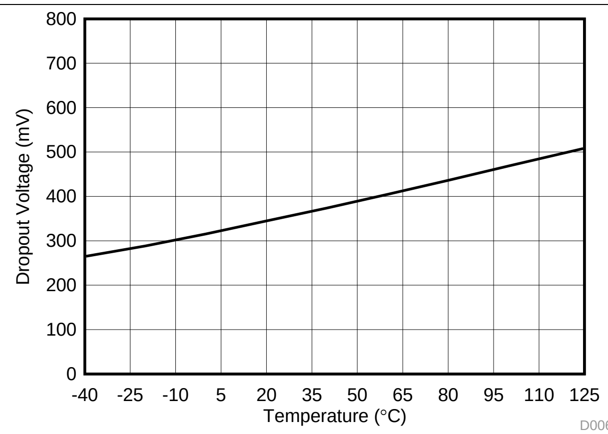
V_{OUT} = 5 V

Figure 4. Quiescent Current vs Ambient Temperature



V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

Figure 5. Dropout Voltage vs Output Current

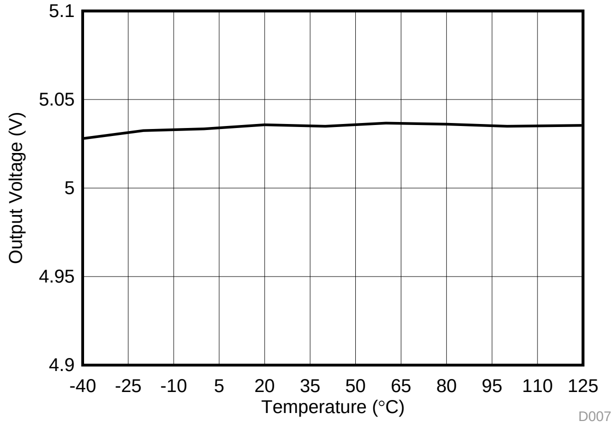


V_{IN} = 5 V, 5-V fixed output, $V_{(Dropout)} = V_{IN} – V_{OUT}$

Figure 6. Dropout Voltage vs Ambient Temperature

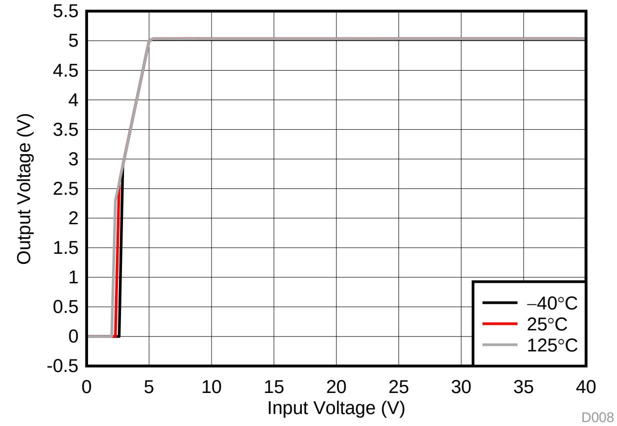
Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



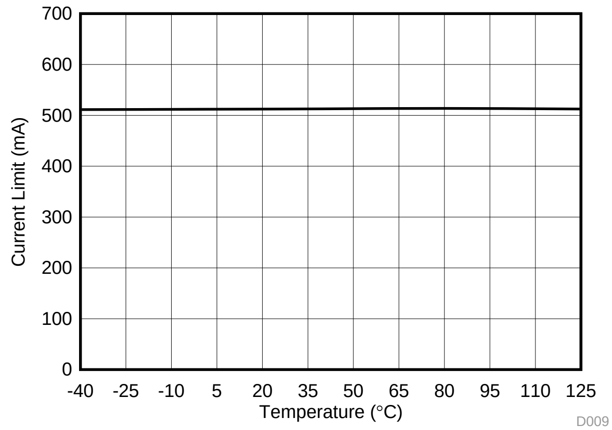
V_{OUT} = 5 V

Figure 7. Output Voltage vs Ambient Temperature



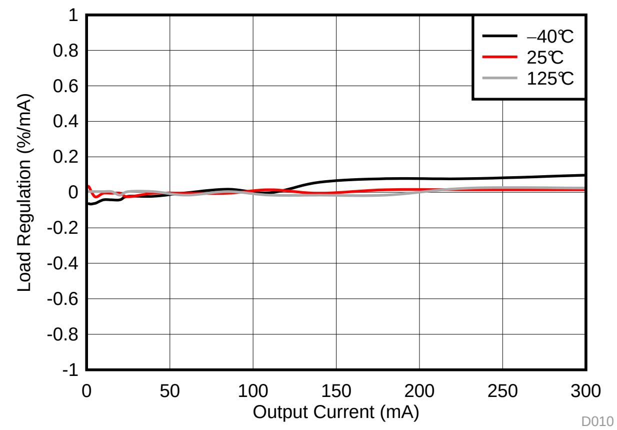
V_{OUT} = 5 V, I_{OUT} = 1 mA

Figure 8. Output Voltage vs Input Voltage



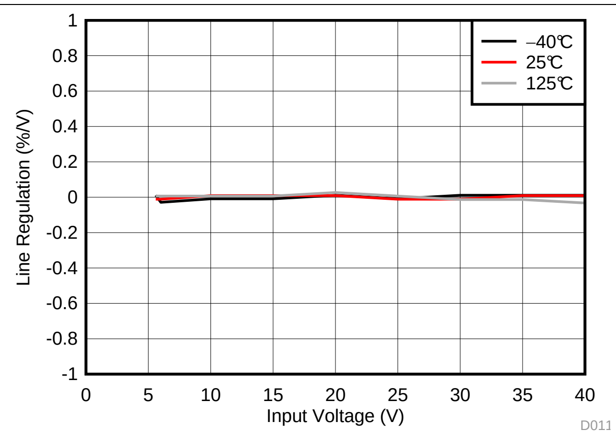
V_{IN} = 14 V, V_{OUT} is shorted to 90% × V_{OUT}

Figure 9. Output Current Limit vs Ambient Temperature



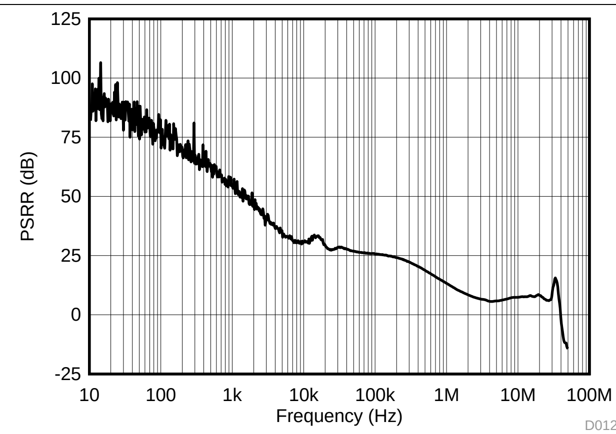
V_{OUT} = 5 V

Figure 10. Load Regulation



V_{OUT} = 5 V, I_{OUT} = 10 mA

Figure 11. Line Regulation

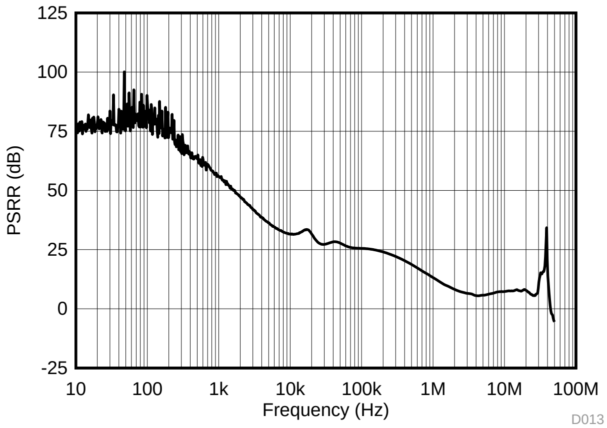


I_{OUT} = 10 mA

Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

V_{IN} = 14 V, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC (unless otherwise noted)



I_{OUT} = 100 mA

Figure 13. PSRR vs Frequency

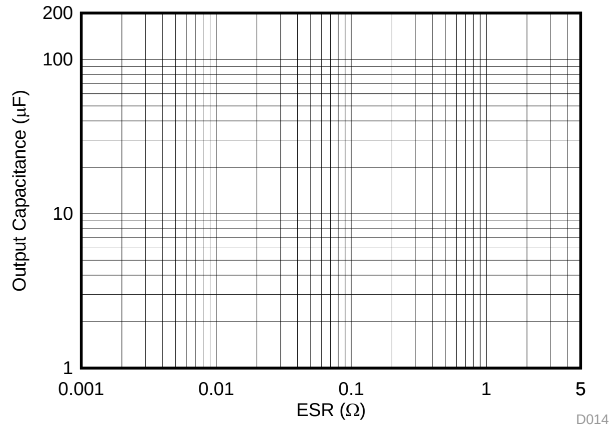


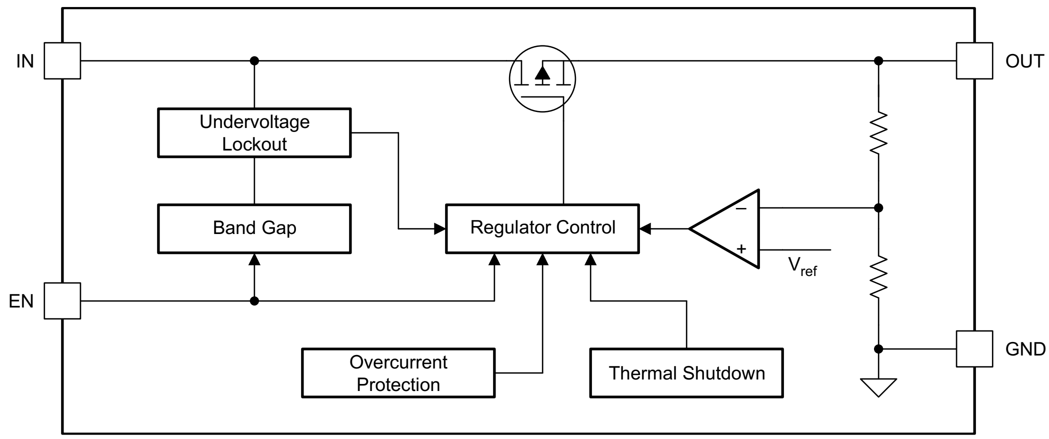
Figure 14. Output Capacitance vs ESR Stability

7 Detailed Description

7.1 Overview

The TPS7B82-Q1 is a 40-V 300-mA low-dropout linear regulator with ultralow quiescent current. This voltage regulator consumes only 3 µA of quiescent current at light load, and is quite suitable for the automotive always-on application.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation ON. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

7.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internal UVLO threshold ($V_{(UVLO)}$). This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required level.

7.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the TSD trip point minus thermal shutdown hysteresis, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} Lower Than 3 V

The device normally operates with input voltages above 3 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With V_{IN} Larger Than 3 V

When V_{IN} is greater than 3 V, if V_{IN} is also higher than the output set value plus the device dropout voltage, V_{OUT} is equal to the set value. Otherwise, V_{OUT} is equal to V_{IN} minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B82-Q1 is a 300-mA 40-V low-dropout linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

Figure 15 shows a typical application circuit for the TPS7B82-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

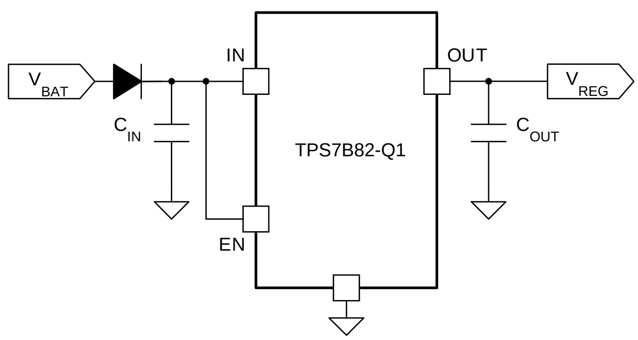


Figure 15. TPS7B82-Q1 Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Requirements Parameters

PARAMETER	VALUE
Input voltage range	3 V to 40 V
Output voltage	5 V or 3.3 V
Output current	300 mA maximum

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

8.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10-µF to 22-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

To ensure the stability of the TPS7B82-Q1, the device requires an output capacitor with a value in the range from 1 μF to 200 μF and with an ESR range between 0.001 Ω and 5 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.3 Application Curve

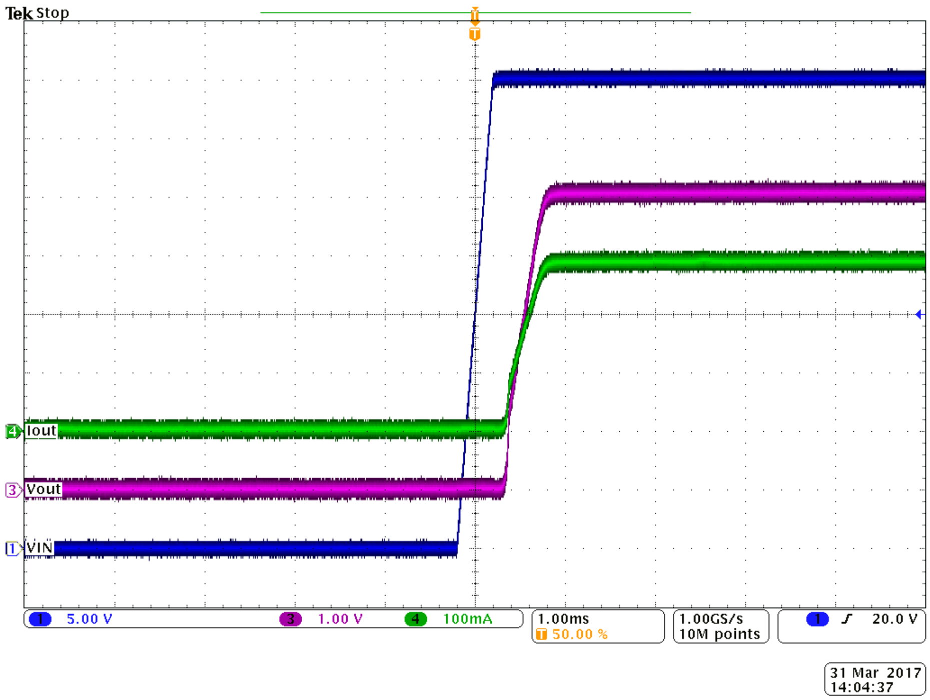


Figure 16. TPS7B82-Q1 Power-Up Waveform (5 V)

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B82-Q1, TI recommends adding a capacitor with a value greater than or equal to 10 µF with a 0.1-µF bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially these high-voltage and large-output-current ones, layout is an important step. If layout is not carefully designed, the regulator could fail to deliver enough output current because of thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad. Figure 17 shows an example layout.

10.2 Layout Example

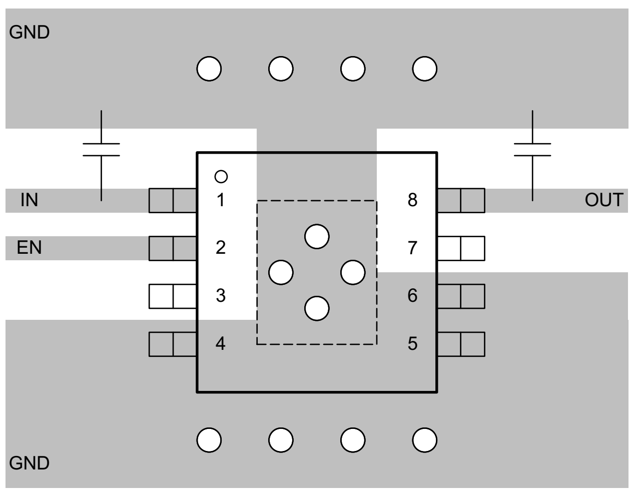


Figure 17. TPSB82-Q1 Example Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B8233QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	1GGX	Samples
TPS7B8233QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1ORH	Samples
TPS7B8250QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	19TX	Samples
TPS7B8250QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1UFH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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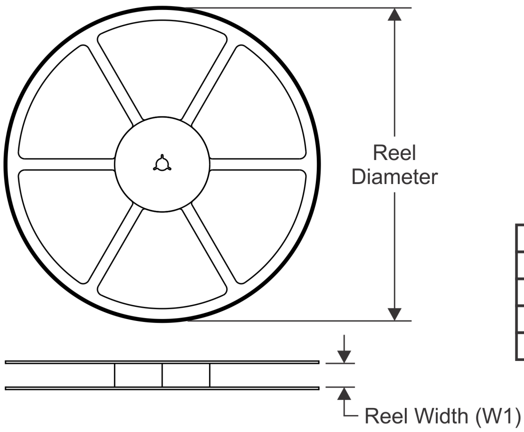
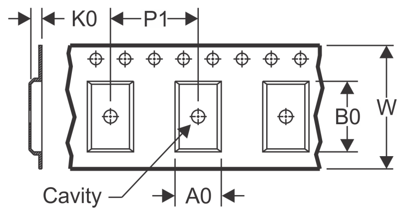
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

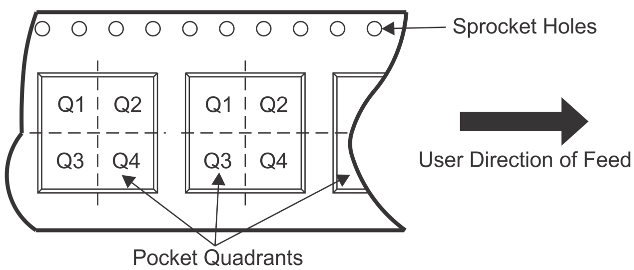


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

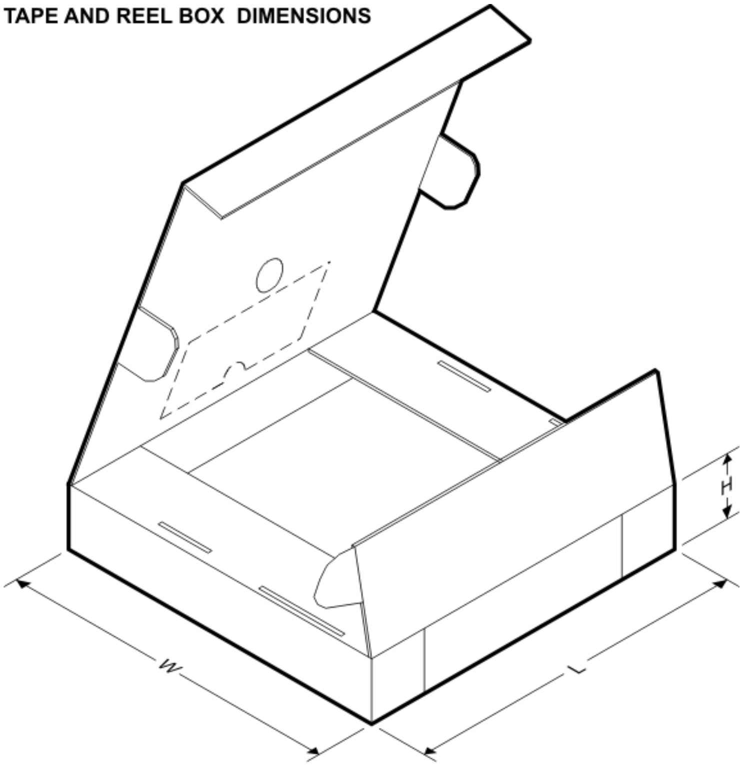
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B8233QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7B8250QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

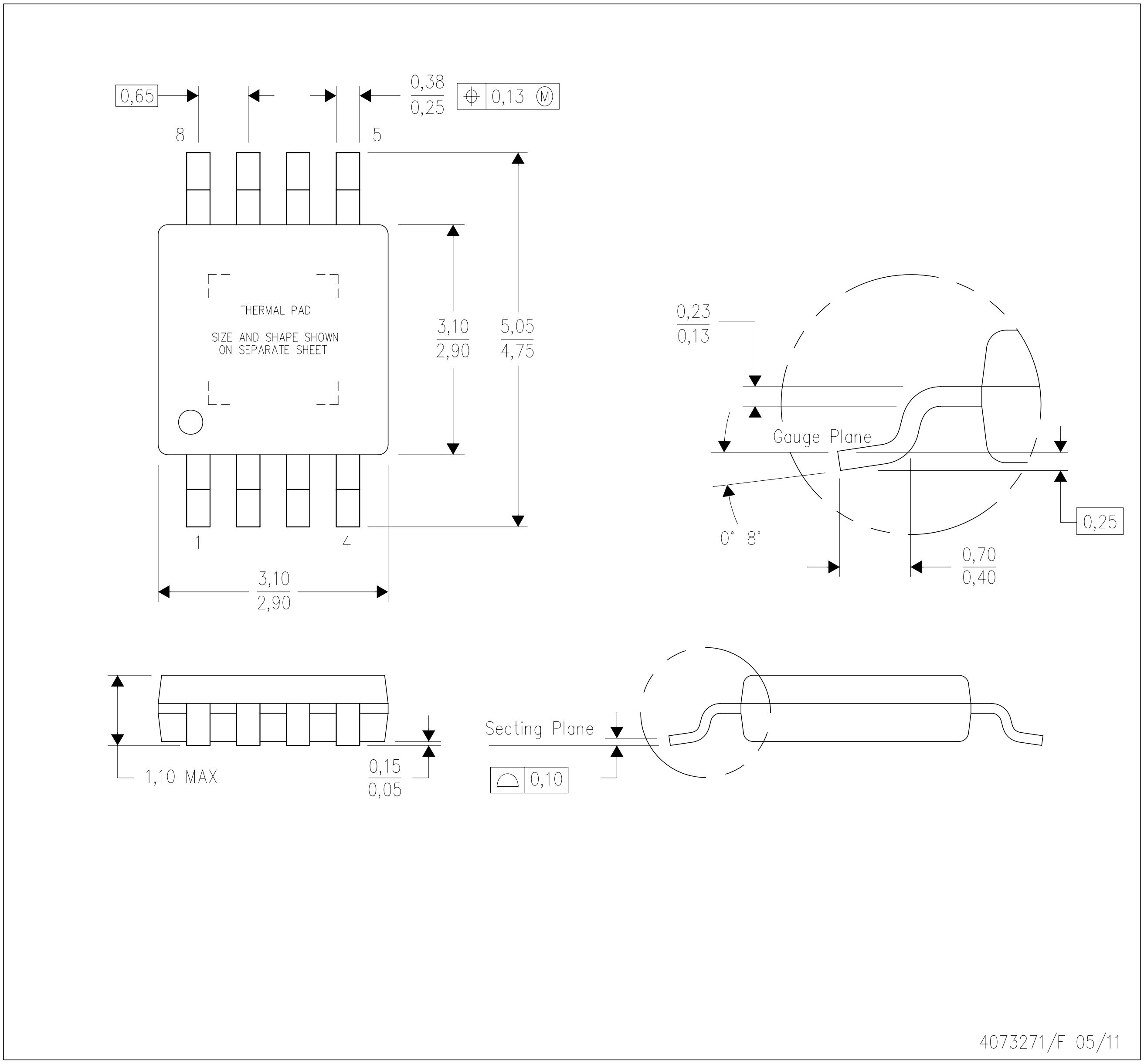
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B8233QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7B8233QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7B8250QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7B8250QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

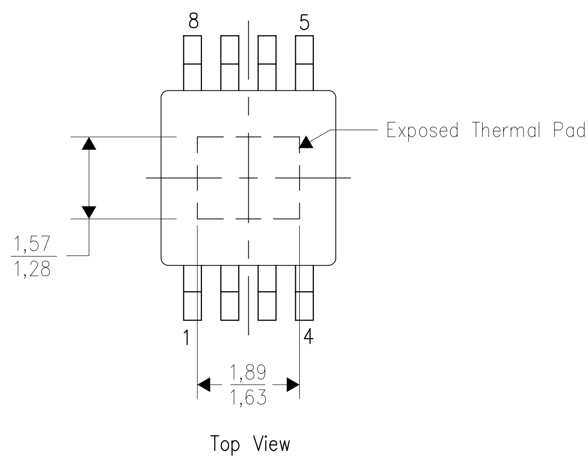
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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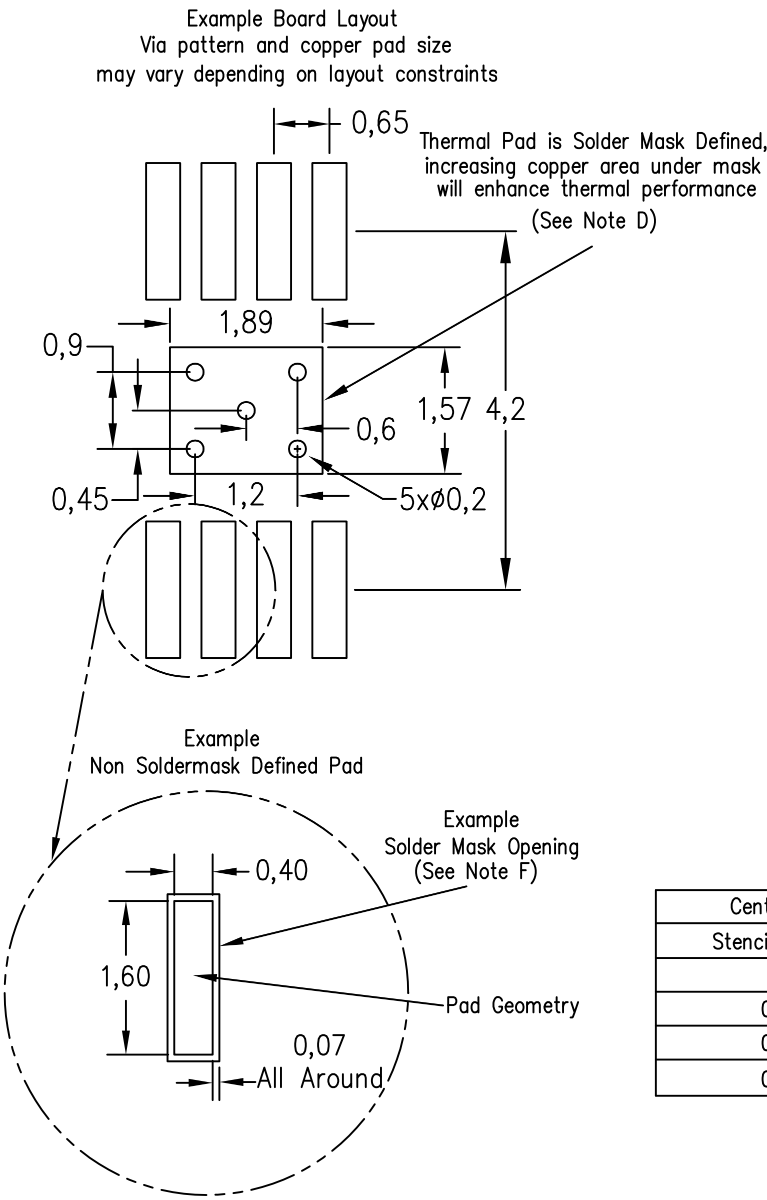
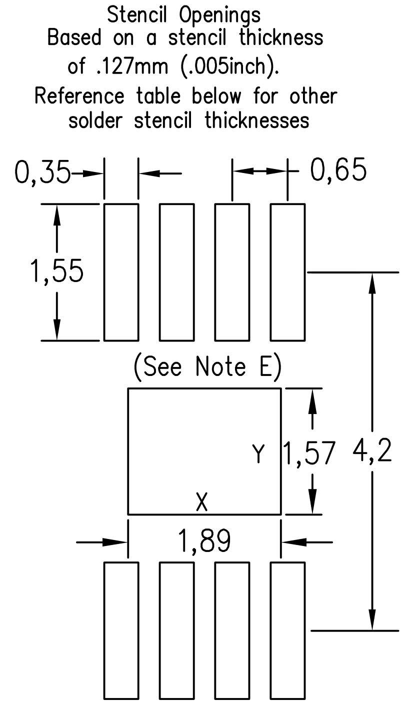
NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

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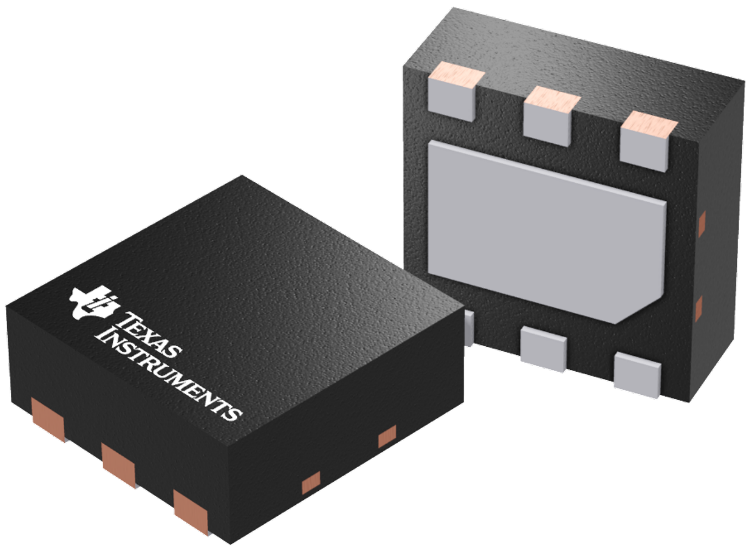
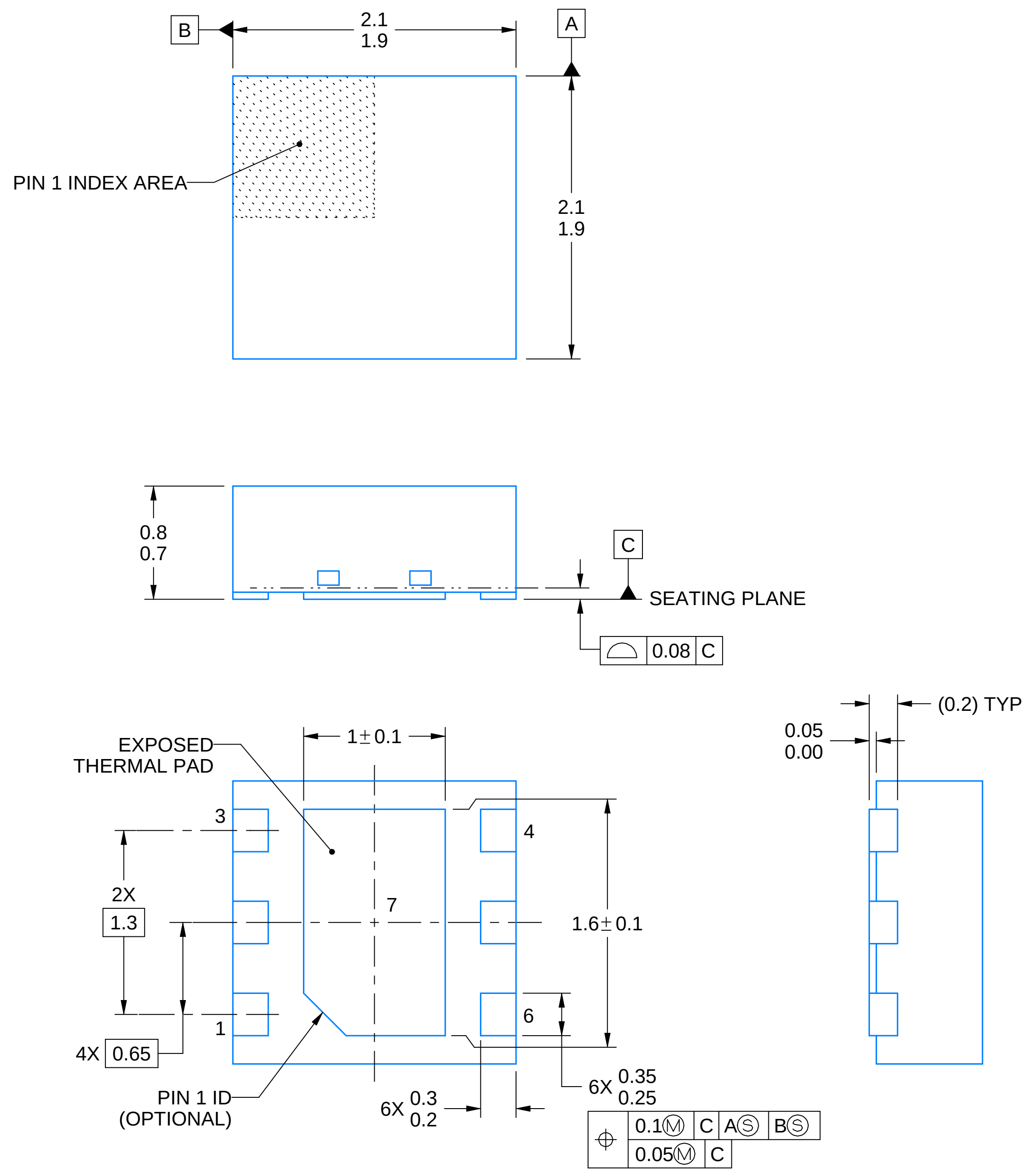
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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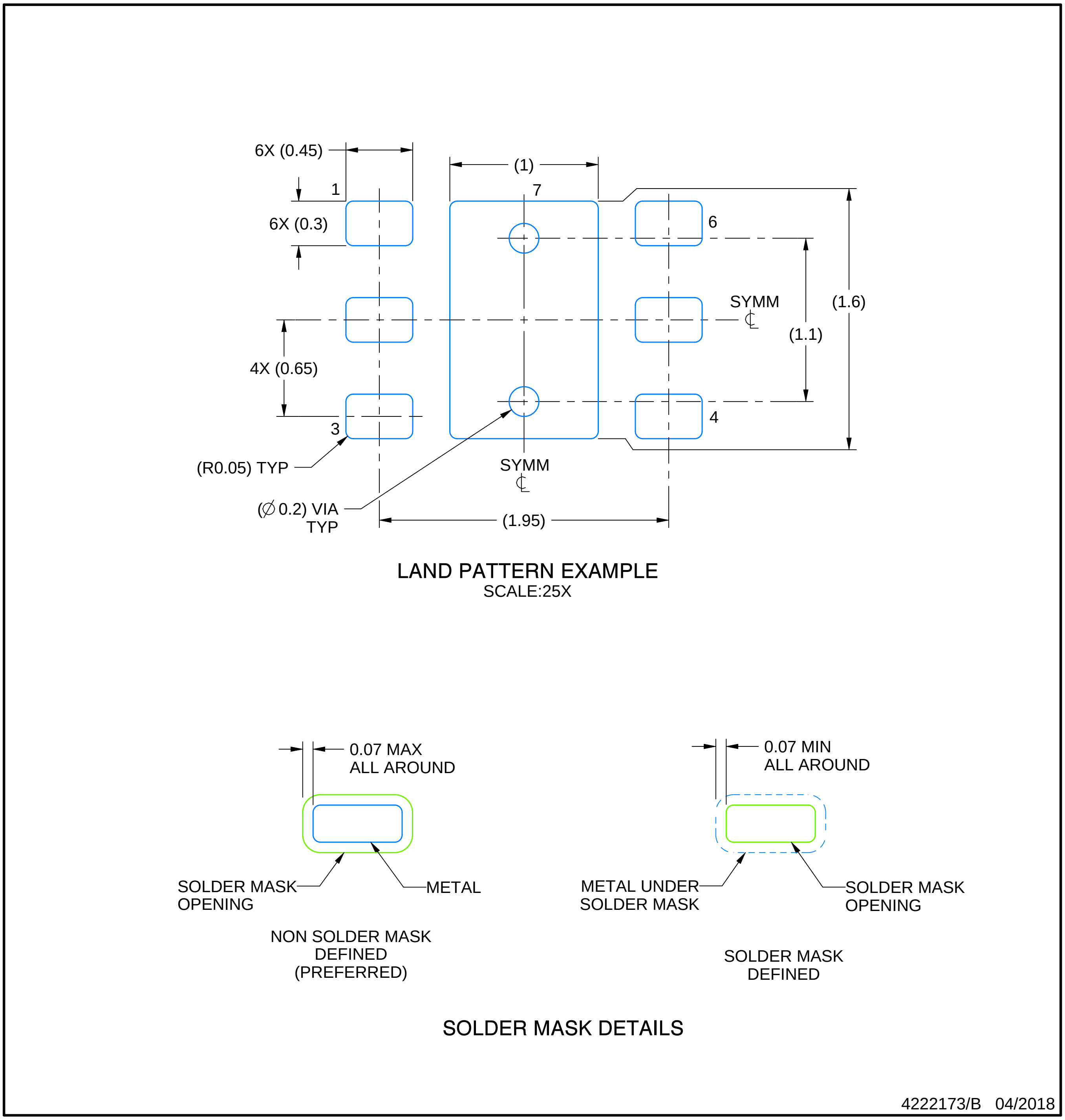
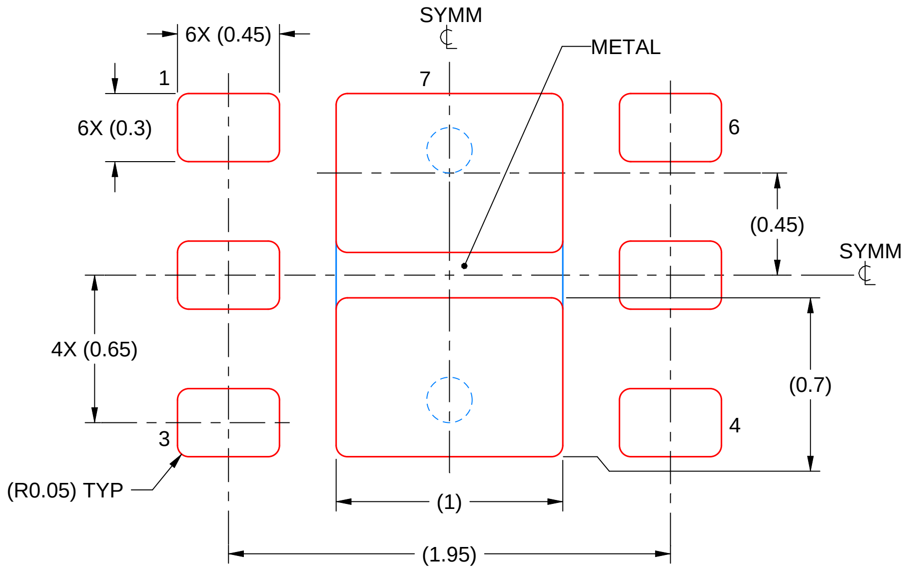
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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