

# TLV185x and TLV186x Family of 40V, Nanopower Comparators

## 1 Features

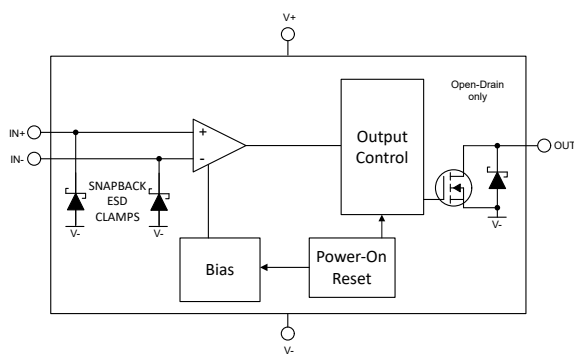
- Low supply current: 440nA per channel
- Wide supply range: 1.8V to 40V
- Over-the-rail inputs: common-mode range extends 40V above (V-) independent of (V+)
- Fail-safe: high impedance inputs with no supply
- Power-on-reset provides a known startup condition
- No phase reversal for overdriven inputs
- Reverse battery protection up to 40V
- Push-pull output option (TLV185x)
- Open-drain output option (TLV186x)
- Temperature range: -40°C to +125°C

## 2 Applications

- [Mobile phones & tablets](#)
- [Headsets/headphones & earbuds](#)
- [PC & notebooks](#)
- [Gas detector](#)
- [Smoke & heat detector](#)
- [Motion Detector](#)
- [Gas meter](#)
- [Servo drive position sensor](#)

## 3 Description

The TLV185x and TLV186x are a family of nanopower, 40V comparators with single, dual and quad channel options. The family offers fail-safe (FS) inputs with push-pull and open-drain output options. These features coupled with nanopower operation over the wide supply range of 1.8V to 40V make this family well-suited for house-keeping functions such as voltage and temperature monitoring in low-power, always-on systems.



**Block Diagram**

All devices include a Power-On Reset (POR) feature that makes sure that the output is in a known state until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

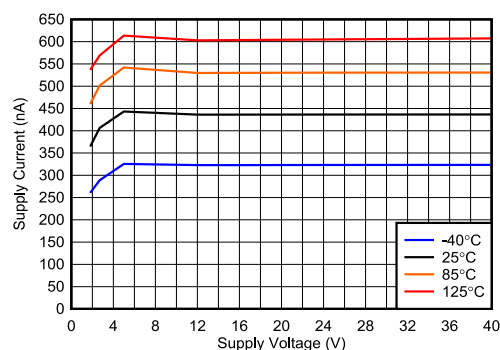
The inputs have over-the-rail capability where both inputs can exceed the supply voltage up to 40V and still operate properly. This makes the comparators well suited for both high and low supply voltage systems without limiting the range of input voltages that can be compared. Likewise, the internal reverse battery protection feature prevents damage to the comparator in the event of improper battery installation to the supply pins.

The TLV185x comparators have a push-pull output stage where as the TLV186x comparators have an open-drain output stage, making it appropriate for level translation.

### Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV1851, TLV1861	SOT-23 (5)	1.60mm x 2.90mm
TLV1852, TLV1862	VSSOP (8)	3.00mm x 3.00mm
TLV1854, TLV1864	TSSOP (14)	4.40mm x 5.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.



**Supply Current vs. Supply Voltage**

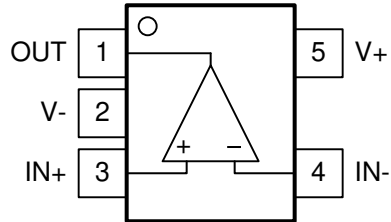


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## 4 Pin Configuration and Functions

### Pin Configuration: TLV1831 and TLV1841

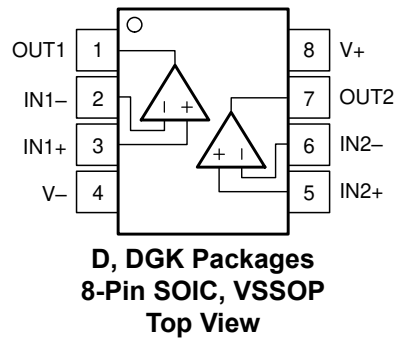


**DBV, DCK Packages**  
**SOT-23-5, SC-70-5**  
**Top View**  
**(Standard "north west" pinout)**

**Table 4-1. Pin Functions: TLV1831 and TLV1841**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage

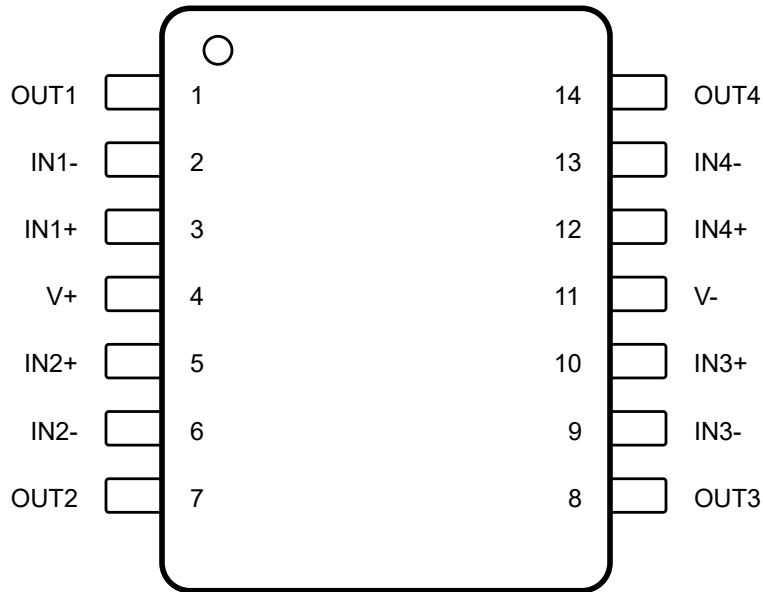
## Pin Configurations: TLV1852 and TLV1862



**Table 4-2. Pin Functions: TLV1852 and TLV1862**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Inverting input pin of comparator 1
IN1+	3	I	Noninverting input pin of comparator 1
V-	4	—	Negative supply voltage
IN2+	5	I	Noninverting input pin of comparator 2
IN2-	6	I	Inverting input pin of comparator 2
OUT2	7	O	Output pin of the comparator 2
V+	8	—	Positive supply voltage

## Pin Configurations: TLV1854 and TLV1864



Not to scale

**D, PW Packages**  
**14-Pin SOIC, TSSOP**  
**Top View**

**Table 4-3. Pin Functions: TLV1854 and TLV1864**

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT1	1	O	Output pin of the comparator 1
IN1-	2	I	Negative input pin of the comparator 1
IN1+	3	I	Positive input pin of the comparator 1
V+	4	-	Positive supply voltage
IN2+	5	I	Positive input pin of the comparator 2
IN2-	6	I	Negative input pin of the comparator 2
OUT2	7	O	Output pin of the comparator 2
OUT3	8	O	Output pin of the comparator 3
IN3-	9	I	Negative input pin of the comparator 3
IN3+	10	I	Positive input pin of the comparator 3
V-	11	-	Negative supply voltage
IN4+	12	I	Positive input pin of the comparator 4
IN4-	13	I	Negative input pin of the comparator 4
OUT4	14	O	Output pin of the comparator 4

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$		42	V
Differential Input Voltage, VID	-42	42	V
Input pins (IN+, IN-) from (V-) <sup>(2)</sup>	-0.3	42	V
Current into Input pins (IN+, IN-) <sup>(3)</sup>	-10	10	mA
Output (Open-drain version only) from (V-) <sup>(4)</sup>	-0.3	42	V
Output (OUT) (Push-Pull) from (V-)	-0.3	(V+) + 0.3	V
Output short circuit current <sup>(5)</sup>	-10	10	mA
Junction temperature, $T_J$		150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to (V-). Inputs (IN+, IN-) can be greater than (V+) and OUT as long as it is within the -0.3V to 42V range
- (3) Input terminals are diode-clamped to (V-). Input signals that swing more than 0.3 V below (V-) must be current-limited to 10mA or less.
- (4) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN-) as long as it is within the -0.3V to 42V range
- (5) Short-circuit to (V-) or (V+).

### 5.2 ESD Ratings

			VALUE	UNIT
TLV1851, TLV1861				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1500	V
TLV1852, TLV1862				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	V
TLV1854, TLV1864				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV185x/6x			UNIT
		DBV (SOT-23)	DGK (VSSOP)	PW (TSSOP)	
		5 Pins	8 Pins	14 Pins	
R <sub>qJA</sub>	Junction-to-ambient thermal resistance	168.1	163.1	94.2	°C/W
R <sub>qJC(top)</sub>	Junction-to-case (top) thermal resistance	68.1	55.5	29	°C/W
R <sub>qJB</sub>	Junction-to-board thermal resistance	37.4	84.7	51.8	°C/W
Y <sub>JT</sub>	Junction-to-top characterization parameter	11.4	5.7	1.3	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	37.1	83.1	51.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V <sub>S</sub> = (V+) – (V–)	1.8	40	V
Input voltage range from (V–)	–0.1	40	V
Common-mode input voltage range from (V–)	0	40	V
Output voltage for open drain from (V–)	–0.1	40	V
Ambient temperature, T <sub>A</sub>	–40	125	°C

## 5.5 Electrical Characteristics

For  $V_S = (V+) - (V-) = 12V$ ,  $V_{CM} = V_S/2$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage		-3.6	$\pm 0.25$	3.6	mV
$V_{OS}$	Input offset voltage	$T_A = -40^\circ C$ to $+125^\circ C$	-4.4		4.4	mV
$dV_{IO}/dT$	Input offset voltage drift			3		$\mu V/^\circ C$
$V_{HYS}$	Input hysteresis voltage		1	2.8	5	mV
$V_{CM-Range}$	Common-mode voltage range from (V-)	$V_S = 1.8V$ to $40V$ $T_A = -40^\circ C$ to $+125^\circ C$	0		40	V
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per comparator (output high)	Push Pull Output Option		520	750	nA
$I_Q$	Quiescent current per comparator (output high)	Push Pull Output Option, $T_A = -40^\circ C$ to $125^\circ C$			1000	nA
$I_Q$	Quiescent current per comparator (output high)	Open Drain Output option, no pull-up resistor		440	640	nA
$I_Q$	Quiescent current per comparator (output high)	Open Drain Output option, no pull-up resistor, $T_A = -40^\circ C$ to $125^\circ C$			850	nA
$V_{POR}$		During power on, $V_S$ must exceed $V_{POR}$ for $t_{ON}$ before the output will reflect the input.		1.5		V
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current <sup>(1)</sup>			1	250	pA
		$T_A = -40^\circ C$ to $+125^\circ C$			1500	pA
$I_{OS}$	Input offset current <sup>(1)</sup>			0.1	100	pA
		$T_A = -40^\circ C$ to $+125^\circ C$			1000	pA
<b>OUTPUT</b>						
$V_{OL}$	Voltage swing from (V-)	$I_{SINK} = 2\mu A$		1		mV
$V_{OL}$	Voltage swing from (V-)	$I_{SINK} = 50\mu A$		20	60	mV
		$I_{SINK} = 50\mu A$ $T_A = -40^\circ C$ to $+125^\circ C$			100	mV
$V_{OH}$	Voltage swing from (V+) (Push Pull only)	$I_{SOURCE} = 2\mu A$		1		mV
$V_{OH}$	Voltage swing from (V+) (Push Pull only)	$I_{SOURCE} = 50\mu A$		25	60	mV
		$I_{SOURCE} = 50\mu A$ $T_A = -40^\circ C$ to $+125^\circ C$			100	mV
$I_{LKG}$	Open-drain output leakage current	$V_{ID} = +0.1V$ , $V_{PULLUP} = (V+)$		0.3		pA
$I_{OL}$	Short-circuit current	Sinking $T_A = -40^\circ C$ to $+125^\circ C$		7		mA



## 5.5 Electrical Characteristics (continued)

For  $V_S = (V+) - (V-) = 12V$ ,  $V_{CM} = V_S/2$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OH}$	Short-circuit current	Sourcing (for Push-Pull only) $T_A = -40^\circ C$ to $+125^\circ C$		5		mA

(1) This parameter is ensured by design and/or characterization and is not tested in production.

## 5.6 Switching Characteristics

For  $V_S = (V+) - (V-) = 12V$ ,  $V_{CM} = V_S/2$  at  $T_A = 25^\circ C$  (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
$T_{PD-HL}$	Propagation delay time, high-to-low	$V_{OD} = 10mV$ , $C_L = 25pF$ , $V_{STEP} = 100mV$		45		$\mu s$
		$V_{OD} = 50mV$ , $C_L = 25pF$ , $V_{STEP} = 100mV$		16		$\mu s$
		$V_{OD} = 100mV$ , $C_L = 25pF$ , $V_{STEP} = 200mV$		13		$\mu s$
$T_{PD-LH}$	Propagation delay time, low-to-high (Push-Pull output)	$V_{OD} = 10mV$ , $C_L = 10pF$ , $V_{STEP} = 100mV$		34		$\mu s$
$T_{PD-LH}$	Propagation delay time, low-to-high (Push-Pull output)	$V_{OD} = 50mV$ , $C_L = 10pF$ , $V_{STEP} = 100mV$		16		$\mu s$
$T_{PD-LH}$	Propagation delay time, low-to-high (Push-Pull output)	$V_{OD} = 100mV$ , $C_L = 10pF$ , $V_{STEP} = 200mV$		14		$\mu s$
$T_{PD-LH}$	Propagation delay time, low-to-high (Open-Drain output)	$V_{OD} = 10mV$ , $C_L = 25pF$ , $R_P = 1M\Omega$ , $V_{STEP} = 100mV$		57		$\mu s$
		$V_{OD} = 50mV$ , $C_L = 25pF$ , $R_P = 1M\Omega$ , $V_{STEP} = 100mV$		36		$\mu s$
		$V_{OD} = 100mV$ , $C_L = 25pF$ , $R_P = 1M\Omega$ , $V_{STEP} = 200mV$		35		$\mu s$
$T_{RISE}$	Output Rise Time, 20% to 80%, push-pull output	$C_L = 25pF$		0.2		$\mu s$
$T_{FALL}$	Output Fall Time, 80% to 20%	$C_L = 25pF$		0.2		$\mu s$
<b>POWER ON TIME</b>						
$T_{ON}$	Power on-time			3		ms

## 5.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 12\text{V}$ ,  $V_{CM} = V_S/2\text{ V}$ ,  $R_P = 1\text{M}\Omega$  (Open Drain only),  $C_L = 25\text{pF}$ ,  $V_{\text{OVERDRIVE}} = 100\text{mV}$  unless otherwise noted.

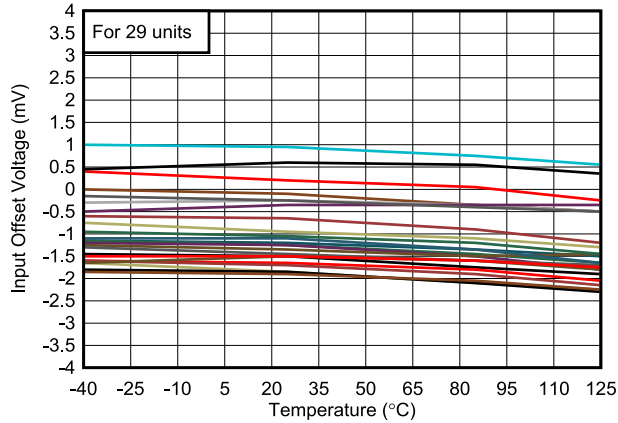


Figure 5-1. Offset vs. Temperature

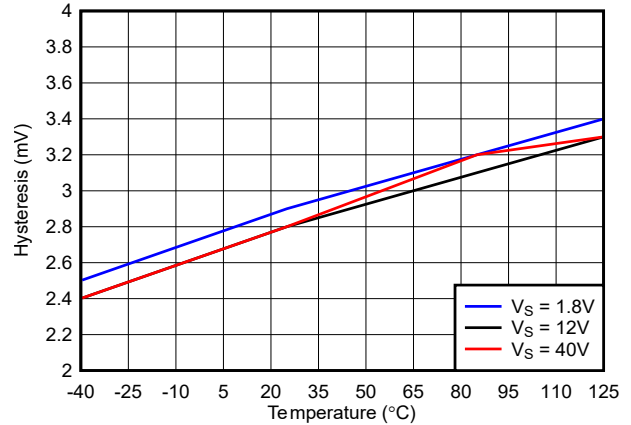


Figure 5-2. Hysteresis vs. Temperature

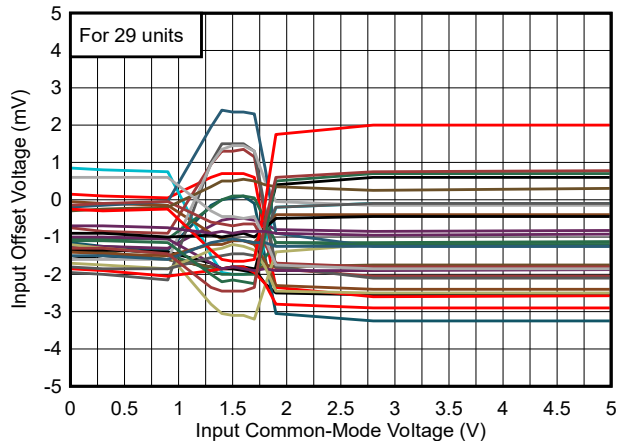


Figure 5-3. Offset vs. Common-Mode, 1.8V

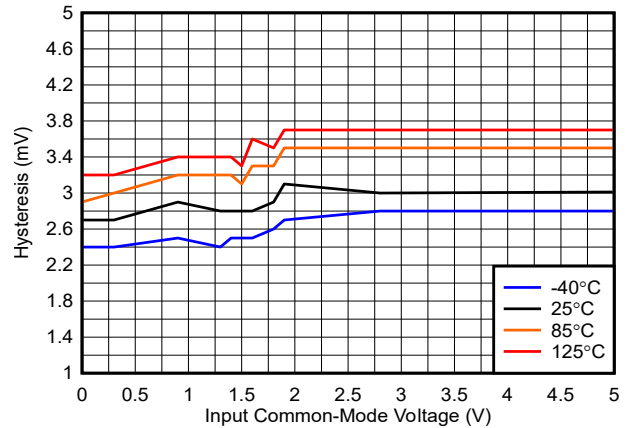


Figure 5-4. Hysteresis vs. Common-Mode, 1.8V

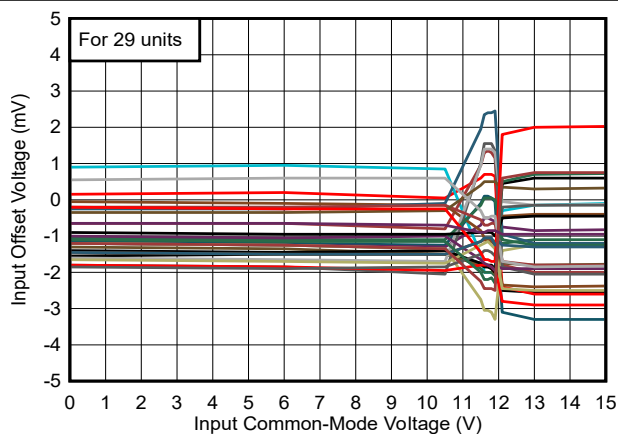


Figure 5-5. Offset vs. Common-Mode, 12V

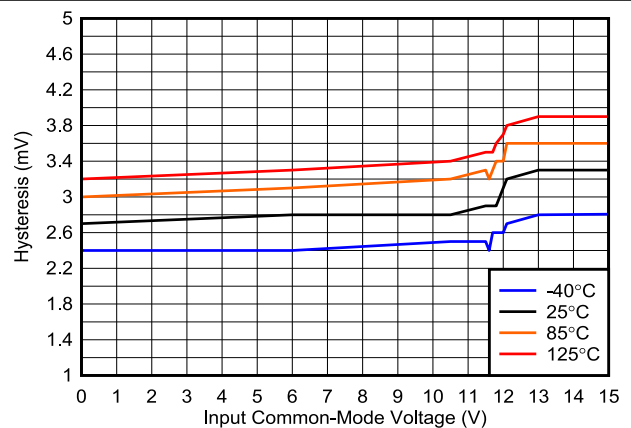


Figure 5-6. Hysteresis vs. Common-Mode, 12V

### 5.7 Typical Characteristics (continued)

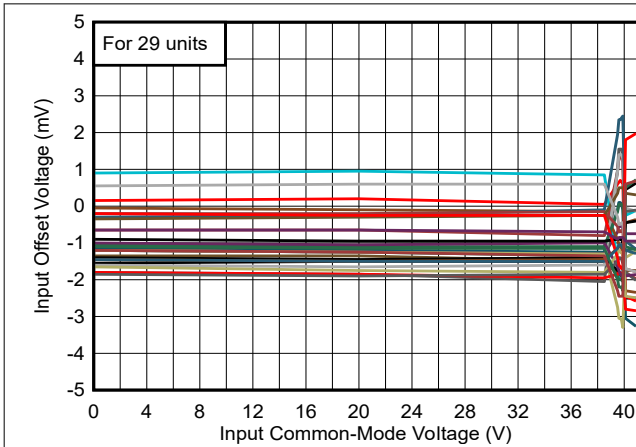


Figure 5-7. Offset vs. Common-Mode, 40V

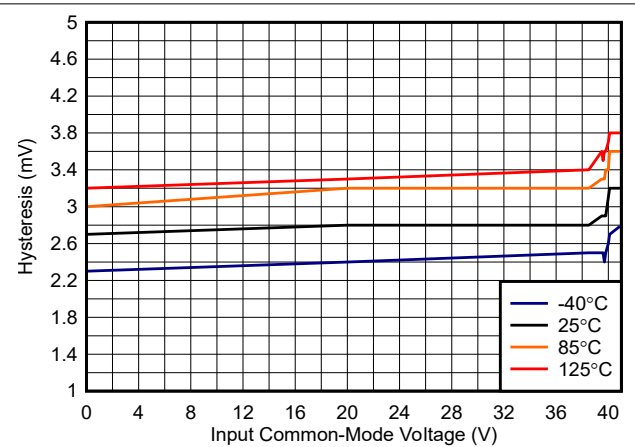


Figure 5-8. Hysteresis vs. Common-Mode, 40V

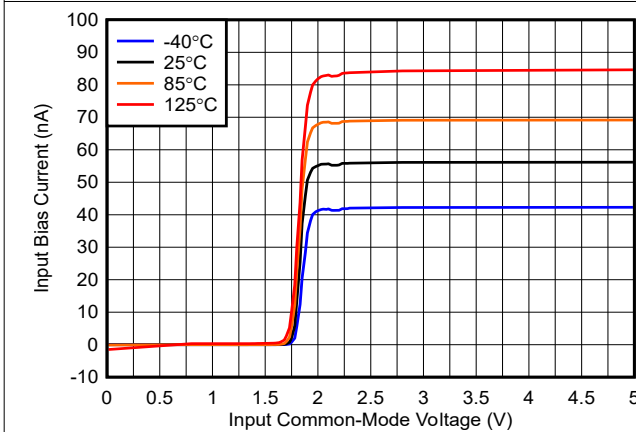


Figure 5-9. Bias Current vs. Common-Mode, 1.8V

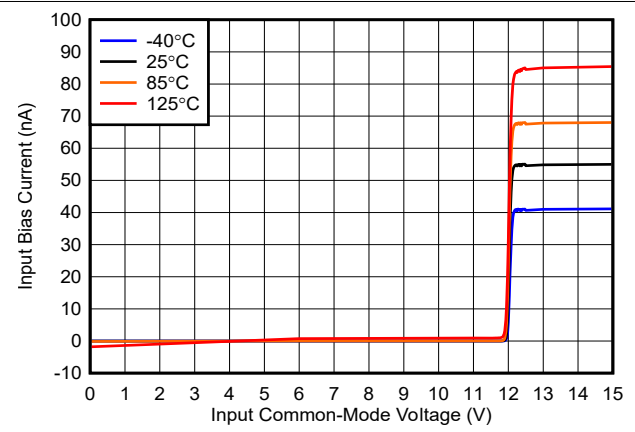


Figure 5-10. Bias Current vs. Common-Mode, 12V

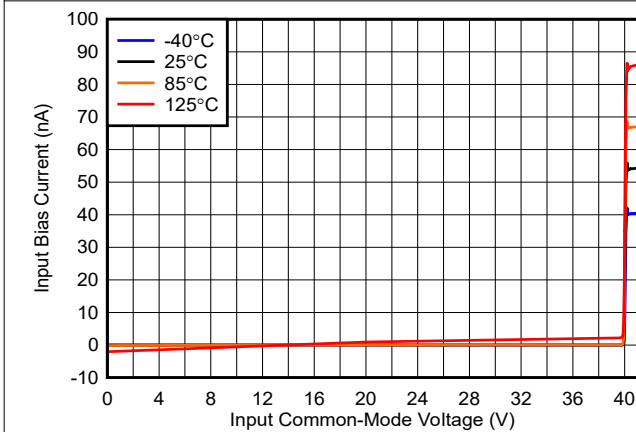


Figure 5-11. Bias Current vs. Common-Mode, 40V

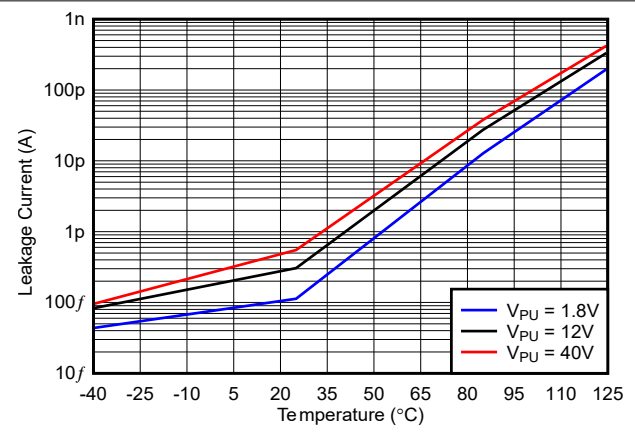


Figure 5-12. Leakage Current vs. Temperature (Open Drain only)

### 5.7 Typical Characteristics (continued)

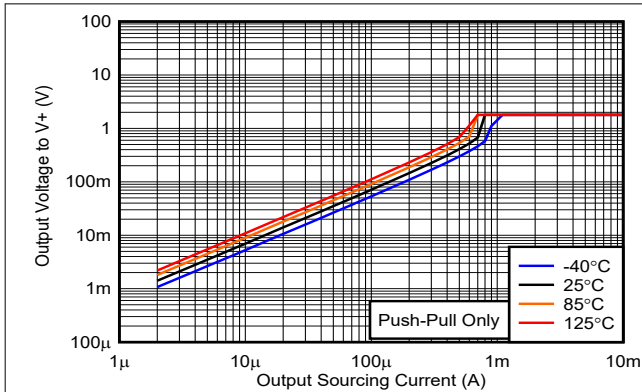


Figure 5-13. Output Voltage vs. Output Sourcing Current, 1.8V

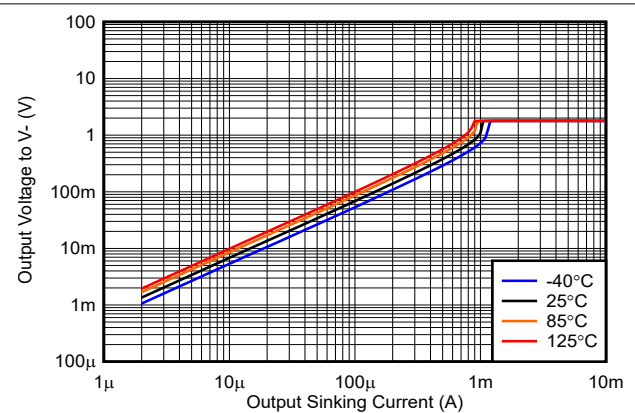


Figure 5-14. Output Voltage vs. Output Sinking Current, 1.8V

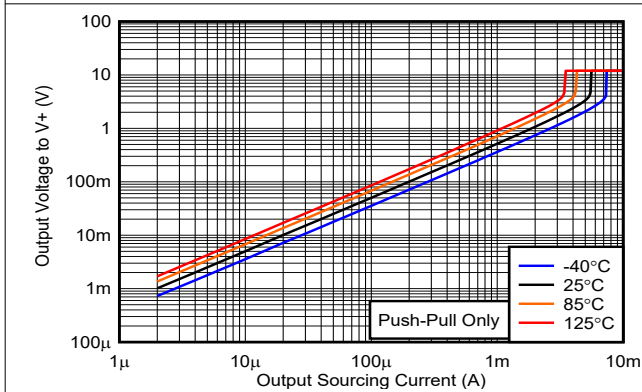


Figure 5-15. Output Voltage vs. Output Sourcing Current, 12V

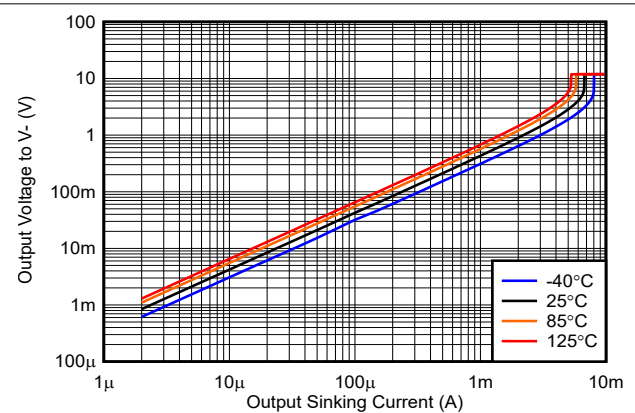


Figure 5-16. Output Voltage vs. Output Sinking Current, 12V

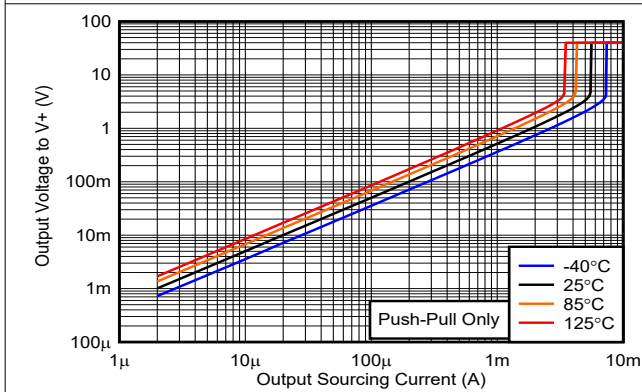


Figure 5-17. Output Voltage vs. Output Sourcing Current, 40V

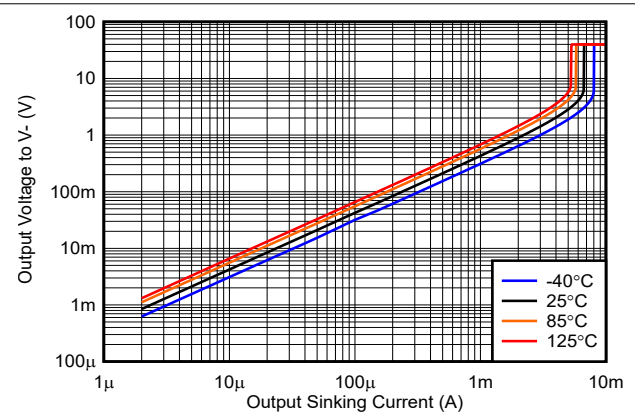
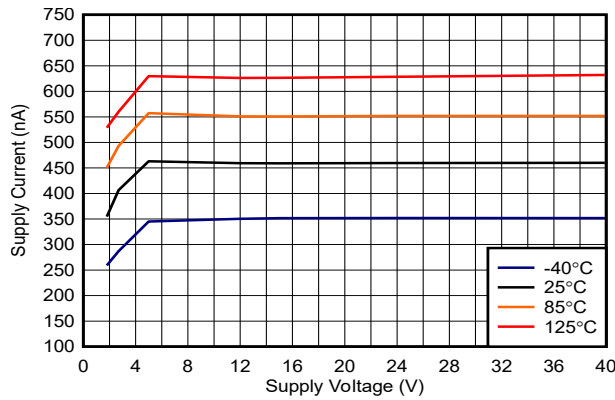
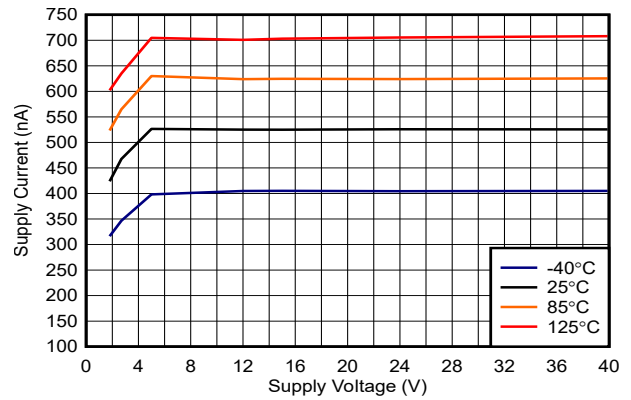


Figure 5-18. Output Voltage vs. Output Sinking Current, 40V

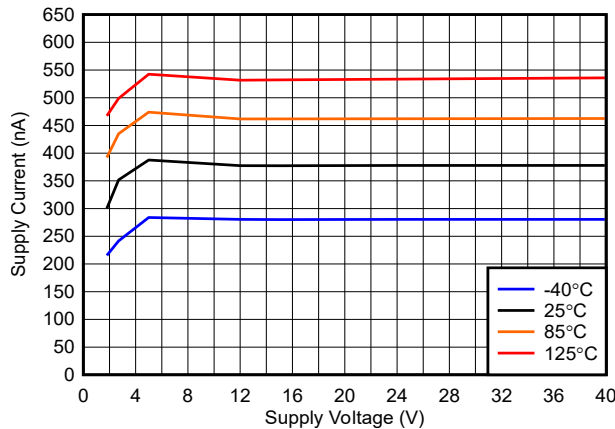
### 5.7 Typical Characteristics (continued)



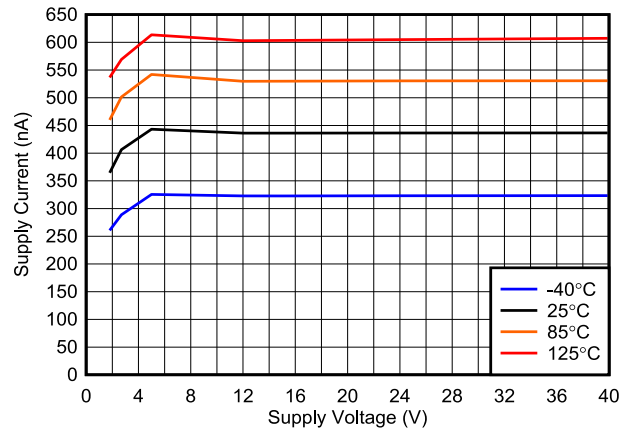
**Figure 5-19. Supply Current vs. Supply Voltage (Output Low), Push-Pull**



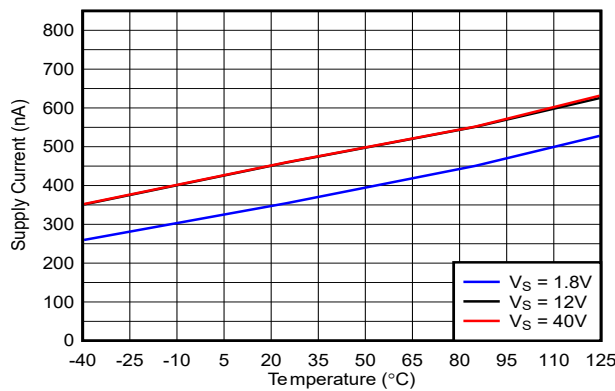
**Figure 5-20. Supply Current vs. Supply Voltage (Output High), Push-Pull**



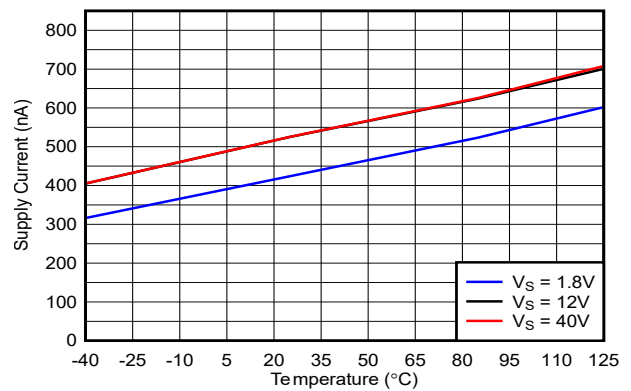
**Figure 5-21. Supply Current vs. Supply Voltage (Output Low), Open Drain**



**Figure 5-22. Supply Current vs. Supply Voltage (Output High), Open Drain**

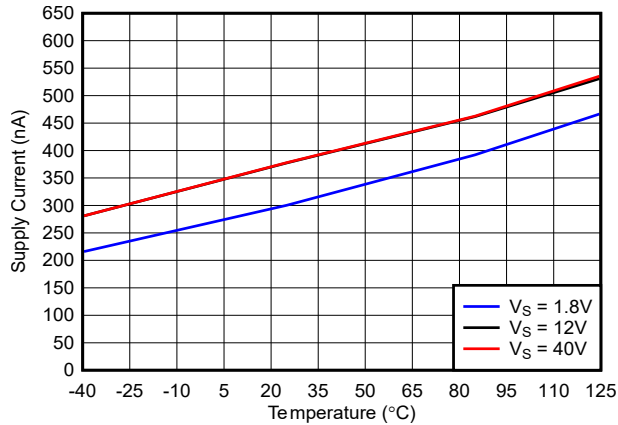


**Figure 5-23. Supply Current vs. Temperature (Output Low), Push-Pull**

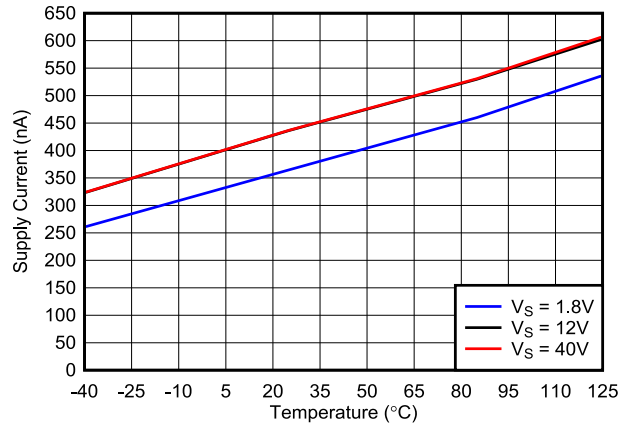


**Figure 5-24. Supply Current vs. Temperature (Output High), Push-Pull**

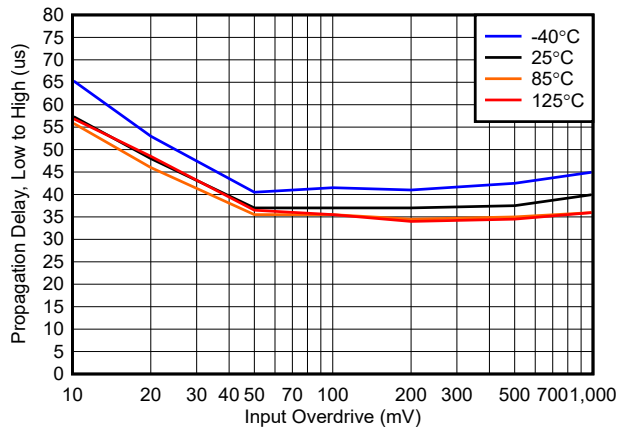
### 5.7 Typical Characteristics (continued)



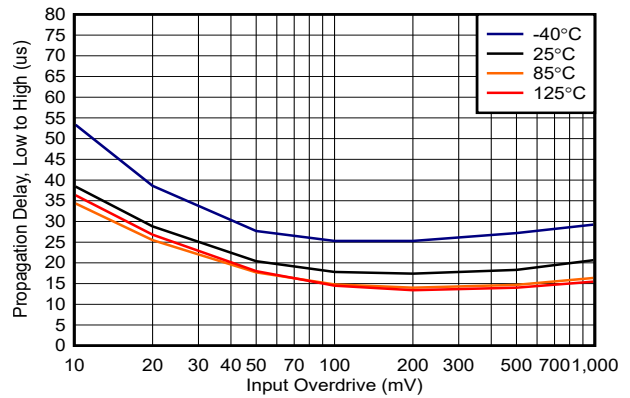
**Figure 5-25. Supply Current vs. Temperature (Output Low), Open Drain**



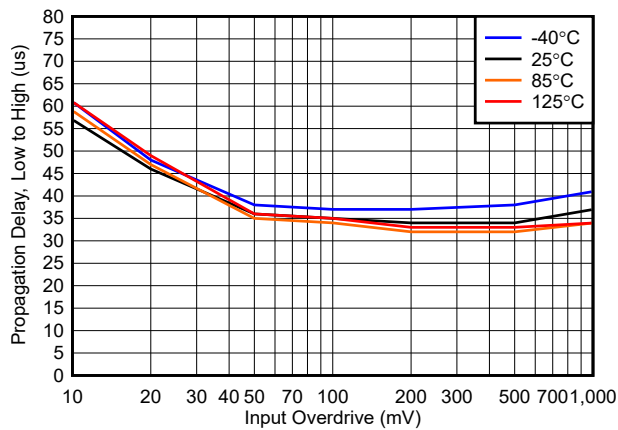
**Figure 5-26. Supply Current vs. Temperature (Output High), Open Drain**



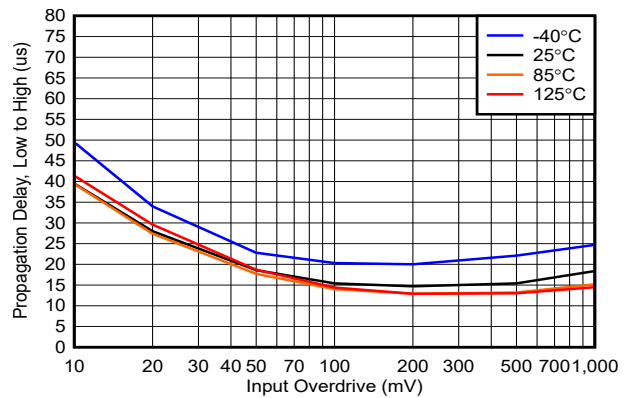
**Figure 5-27. Propagation Delay, Low to High, 1.8V, Open Drain**



**Figure 5-28. Propagation Delay, Low to High, 1.8V, Push-Pull**

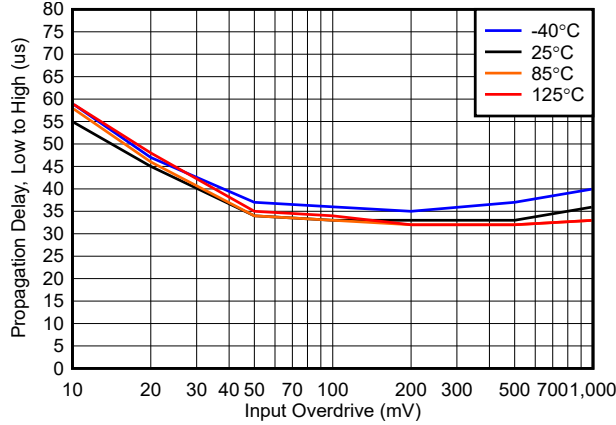


**Figure 5-29. Propagation Delay, Low to High, 12V, Open Drain**

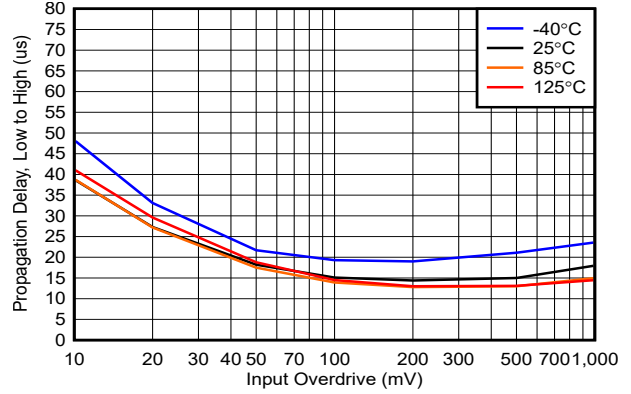


**Figure 5-30. Propagation Delay, Low to High, 12V, Push-Pull**

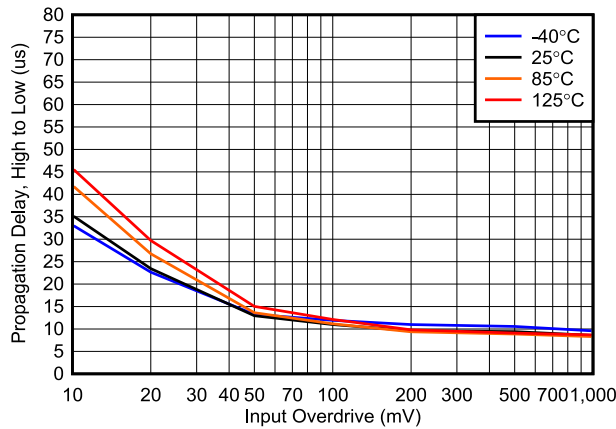
### 5.7 Typical Characteristics (continued)



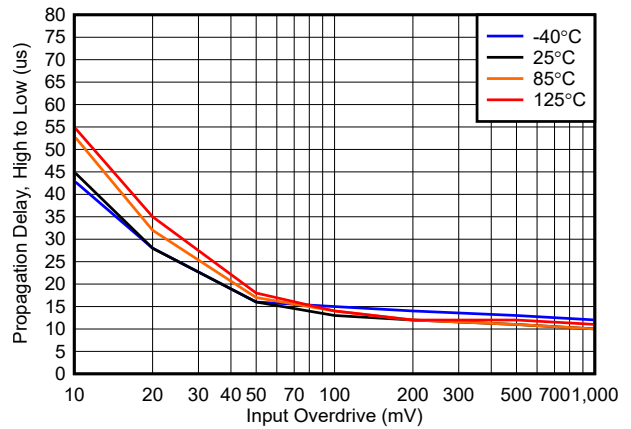
**Figure 5-31. Propagation Delay, Low to High, 40V, Open Drain**



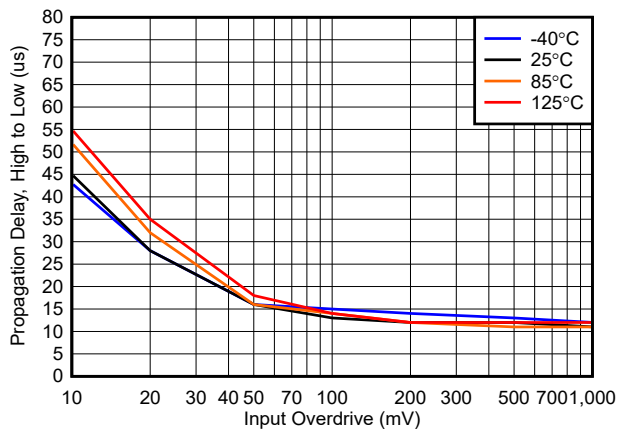
**Figure 5-32. Propagation Delay, Low to High, 40V, Push-Pull**



**Figure 5-33. Propagation Delay, High to Low, 1.8V**



**Figure 5-34. Propagation Delay, High to Low, 12V**



**Figure 5-35. Propagation Delay, High to Low, 40V**

## 6 Detailed Description

### 6.1 Overview

The TLV185x and TLV186x devices are nanopower comparators with push-pull and open-drain output options. Operating down to 1.8V while only consuming only 440nA per channel, the TLV185x and TLV186x are well suited for voltage, current, and temperature sensing in low and high voltage low-power, always-on systems. An internal power-on reset circuit ensures that the output remains in a known state during power-up and power-down. Inputs have fail-safe inputs that can tolerate input transients without damage or false outputs.

### 6.2 Functional Block Diagrams

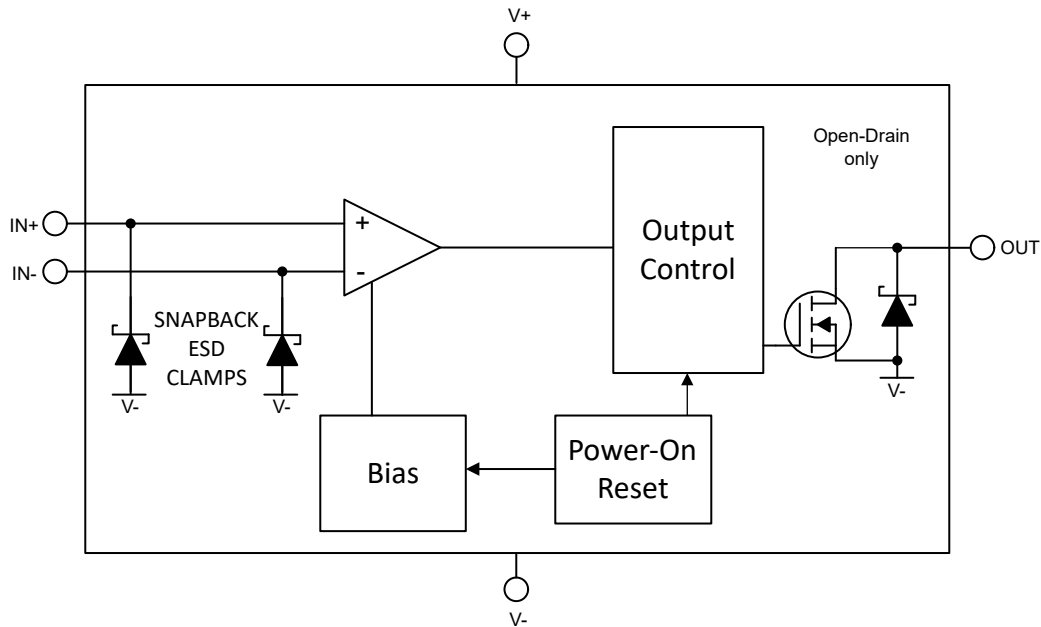


Figure 6-1. Block Diagram

### 6.3 Feature Description

The TLV185x (push-pull output) and TLV186x (open-drain output) devices are nano-power comparators that are capable of operating at high voltages. This family of comparators feature a fail safe input stage and over the rail operating condition mode capable of operating up to 40V, independent of V+. The comparators also have an internal reverse battery protection feature and Power-On-Reset for known start-up conditions.

### 6.4 Device Functional Modes

#### 6.4.1 Inputs

##### 6.4.1.1 Operating Common-Mode Ranges

The TLV185x and TLV186x devices have two operating common-mode ranges: within-the-rail and over-the-rail.

#### Within-the-Rail Operation: IN+ and IN- are less than (V+)

When an input pin is operating less than (V+), there are two operating regions defined where input voltages can be compared: low common-mode and high-common mode. In low-common mode which extends typically from 0V to (V+) - 1V, the typical input bias current is less than 1pA. In high common-mode which extends typically from (V+) - 1V to (V+), the typical input bias current is less than 14nA.

#### Over-the-Rail Operation: IN+ and/or IN- are greater than (V+)

The TLV185x and TLV186x devices have a distinctive input stage that allows the input common mode range to extend from 0V to 40V independent of the supply voltage. This feature means that operation at low supply



voltages does not limit the range of input voltages that can be compared. When an input pin is operating over-the-rail (above (V+)), the bias current increases to a typical value of 55nA.

See Figure 6-9 to 6-11 in the [Typical Characteristics](#) section for input bias current vs. common-mode voltages.

#### 6.4.1.2 Fail-Safe Inputs

A feature of the TLV185x and TLV186x family is that the inputs are fail safe up to 40V, independent of (V+). The inputs are maintained as high input impedance and can be of any value between -0.1V and 40V, even while (V+) is unpowered or below the minimum supply voltage. This feature avoids power sequencing or transient issues since the inputs are not diode clamped to (V+).

#### 6.4.1.3 Unused Inputs

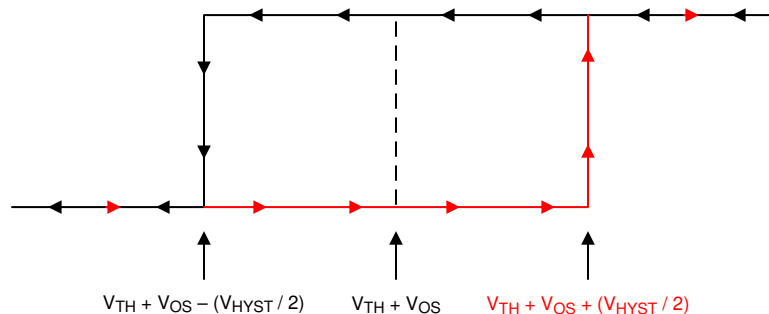
If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

### 6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in [Figure 6-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

(2.8 mV for the TLV185x/6x family)



**Figure 6-2. Hysteresis Transfer Curve**

### 6.4.3 Outputs

#### 6.4.3.1 TLV185x Push-Pull Output

The TLV185x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs should be left floating, and never tied to a supply, ground, or another output.

#### 6.4.3.2 TLV186x Open-Drain Output

The TLV186x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 40V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic

level translation. TI recommends setting the pull-up resistor current to less than 100uA to optimize  $V_{OL}$  logic levels. Lower pull-up resistor values will help increase the rising edge risetime, but at the expense of increasing  $V_{OL}$  and higher power dissipation. The risetime will be dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors ( $>1M\Omega$ ) will create an exponential rising edge due to the output RC time constant and increase the risetime.

Directly shorting the output to ( $V+$ ) can result in thermal runaway and eventual device destruction at high ( $>12V$ ) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs should be left floating, or can be tied to the ( $V-$ ) pin if floating pins are not desired.

#### 6.4.4 ESD Protection

##### 6.4.4.1 Inputs

The fail-safe inputs incorporates internal ESD protection circuits on all pins. The fail-safe inputs have ESD protection from each pin to ( $V-$ ) which allows these pins to exceed the supply voltage ( $V+$ ) up to 40V. If input voltages are to exceed 40V, an external clamp would be required. Likewise, negative voltages on the inputs are ESD clamped to ( $V-$ ) and should be limited to less than -0.1V.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents should the clamps conduct. The current should be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

##### 6.4.4.2 Outputs

The TLV185x push-pull output protection also contains a conventional diode-type ESD clamps between the output and ( $V-$ ), as the output should not exceed the supply rails.

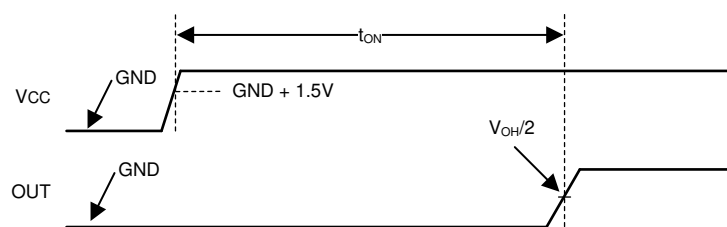
The TLV186x open-drain output ESD protection also consists of a snapback ESD clamp between the output and ( $V-$ ) to allow the output to be pulled above ( $V+$ ) to a maximum of 40V.

#### 6.4.5 Power-On Reset (POR)

The TLV185x and TLV186x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply ( $V+$ ) is ramping up or ramping down, the POR circuitry will be activated for up to 2ms after the  $V_{POR}$  of 1.5V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input ( $V_{ID}$ ).

For the TLV185x push-pull output devices, the output is held low during the POR period ( $t_{on}$ ).

For the TLV186x open drain output devices, the POR circuit will keep the output high impedance (Hi-Z) during the POR period ( $t_{on}$ ).



**Figure 6-3. Power-On Reset Timing Diagram**

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the POR period.

#### **6.4.6 Reverse Battery Protection**

The TLV185x and TLV186x devices have an internal reverse battery protection feature that prevents damage to the comparator in the event of improper battery installation to the supply pins. This protection feature works up to 40V.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

#### 7.1.1 Basic Comparator Definitions

##### 7.1.1.1 Operation

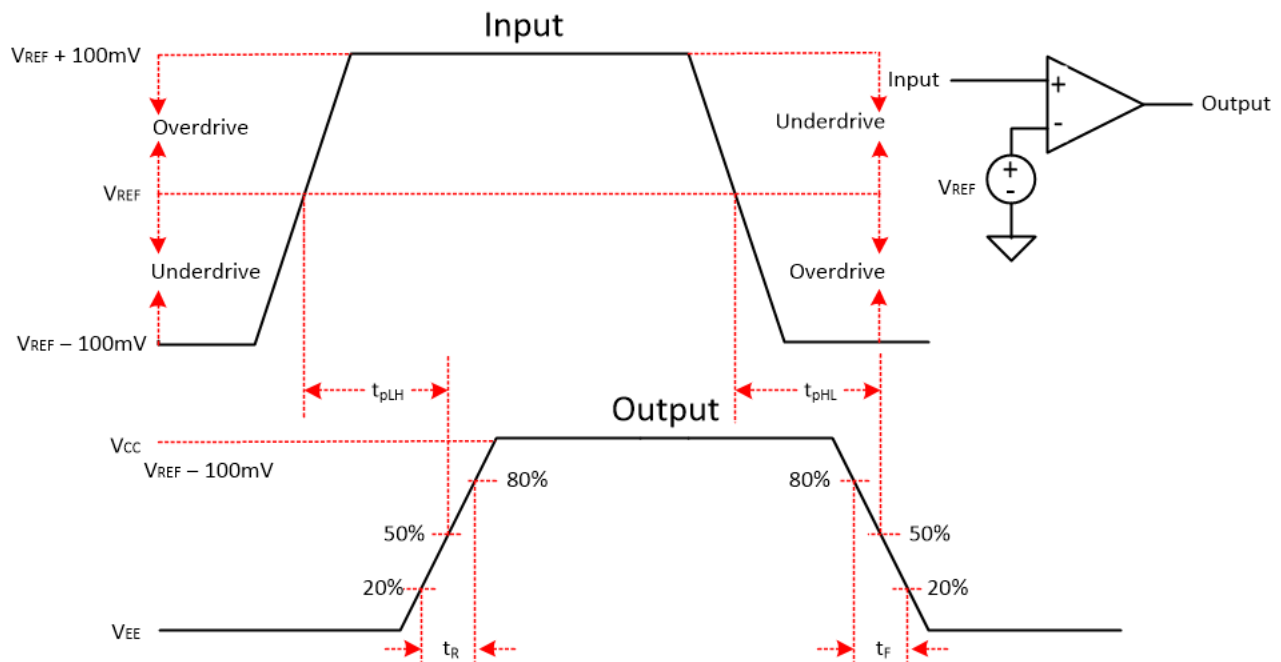
The basic comparator compares the input voltage ( $V_{IN}$ ) on one input to a reference voltage ( $V_{REF}$ ) on the other input. In the [Figure 7-1](#) example below, if  $V_{IN}$  is less than  $V_{REF}$ , the output voltage ( $V_O$ ) is logic low ( $V_{OL}$ ). If  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is at logic high ( $V_{OH}$ ). [Table 7-1](#) summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

**Table 7-1. Output Conditions**

Inputs Condition	Output
$IN+ > IN-$	HIGH ( $V_{OH}$ )
$IN+ = IN-$	Indeterminate (chatters - see <a href="#">Hysteresis</a> )
$IN+ < IN-$	LOW ( $V_{OL}$ )

##### 7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as  $t_{pLH}$  and  $t_{pHL}$  in [Figure 7-1](#) and is measured from the mid-point of the input to the midpoint of the output.



**Figure 7-1. Comparator Timing Diagram**

### 7.1.1.3 Overdrive Voltage

The overdrive voltage,  $V_{OD}$ , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the [Figure 7-1](#) example. The overdrive voltage can influence the propagation delay ( $t_p$ ). The smaller the overdrive voltage, the longer the propagation delay, particularly when  $<100\text{mV}$ . If the fastest speeds are desired, it is recommended to apply the highest amount of overdrive possible.

The risetime ( $t_r$ ) and falltime ( $t_f$ ) is the time from the 20% and 80% points of the output waveform.

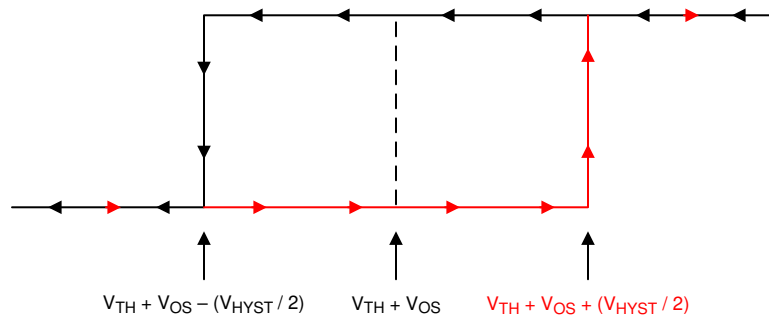
### 7.1.2 Hysteresis

The basic comparator configuration may produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV185x and TLV186x devices only have a minimal amount of internal hysteresis of 2.7mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state.

The hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components:  $V_{TH}$ ,  $V_{OS}$ , and  $V_{HYST}$ :

- $V_{TH}$  is the actual set voltage or threshold trip voltage.
- $V_{OS}$  is the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$  is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

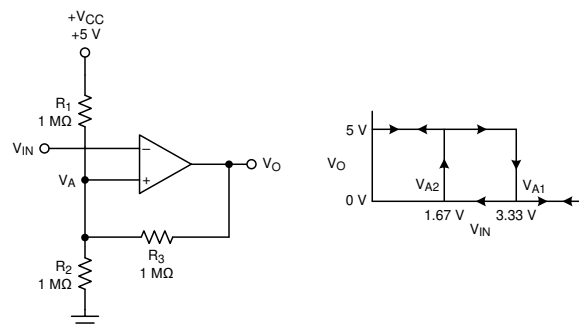


**Figure 7-2. Hysteresis Transfer Curve**

For more information, please see Application Note SBOA219 "[Comparator with and without hysteresis circuit](#)".

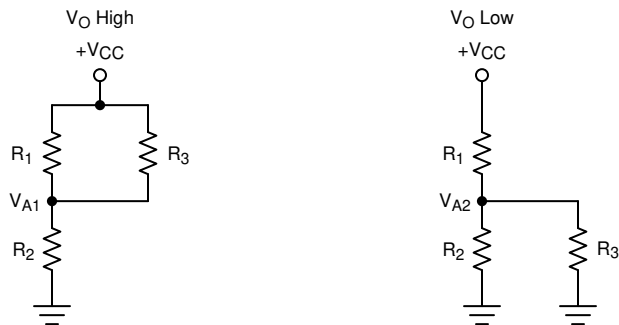
#### 7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_{CC}$ ), as shown in [Figure 7-3](#).



**Figure 7-3. TLV185x in an Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 7-3](#).



**Figure 7-4. Inverting Configuration Resistor Equivalent Networks**

When  $V_{IN}$  is less than  $V_A$ , the output voltage is high (for simplicity, assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ , as shown in [Figure 7-4](#).

[Equation 1](#) below defines the high-to-low trip voltage ( $V_{A1}$ ).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than  $V_A$ , the output voltage is low. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ , as shown in [Equation 2](#).

Use [Equation 2](#) to define the low to high trip voltage ( $V_{A2}$ ).

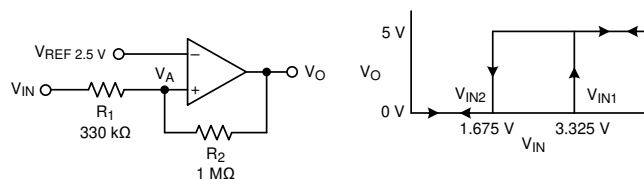
$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

[Equation 3](#) defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

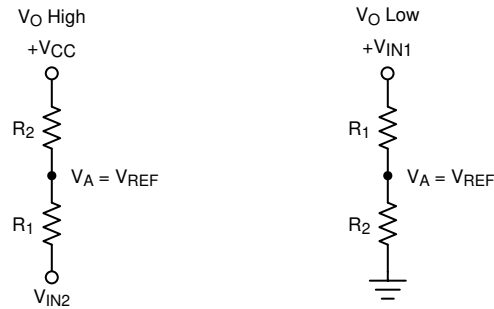
### 7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference ( $V_{REF}$ ) at the inverting input, as shown in [Figure 7-5](#),



**Figure 7-5. TLV185x in a Non-Inverting Configuration With Hysteresis**

The equivalent resistor networks when the output is high and low are shown in [Figure 7-6](#).



**Figure 7-6. Non-Inverting Configuration Resistor Networks**

When  $V_{IN}$  is less than  $V_{REF}$ , the output is low. For the output to switch from low to high,  $V_{IN}$  must rise above the  $V_{IN1}$  threshold. Use [Equation 4](#) to calculate  $V_{IN1}$ .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \quad (4)$$

When  $V_{IN}$  is greater than  $V_{REF}$ , the output is high. For the comparator to switch back to a low state,  $V_{IN}$  must drop below  $V_{IN2}$ . Use [Equation 5](#) to calculate  $V_{IN2}$ .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as shown in [Equation 6](#).

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

For more information, please see Application Notes SNOA997 "[Inverting comparator with hysteresis circuit](#)" and SBOA313 "[Non-Inverting Comparator With Hysteresis Circuit](#)".

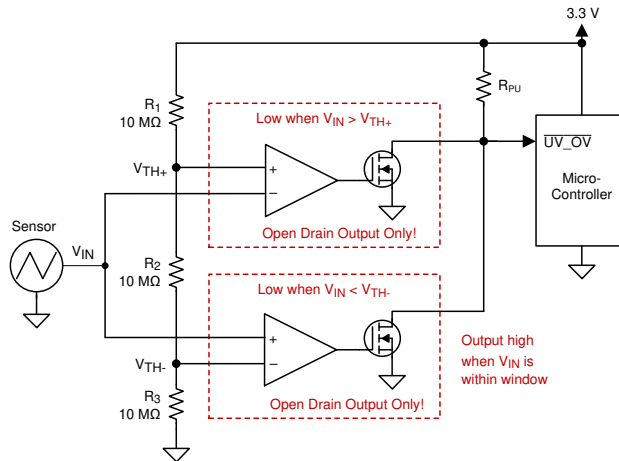
### 7.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

It is also possible to use an open drain output device, such as the TLV186x, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as  $R2 + R_{PULLUP}$ . TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

## 7.2 Typical Applications

### 7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. [Figure 7-7](#) shows a simple window comparator circuit. Window comparators require open drain outputs (TLV186x if the outputs are directly connected together).



**Figure 7-7. Window Comparator**

### 7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

### 7.2.1.2 Detailed Design Procedure

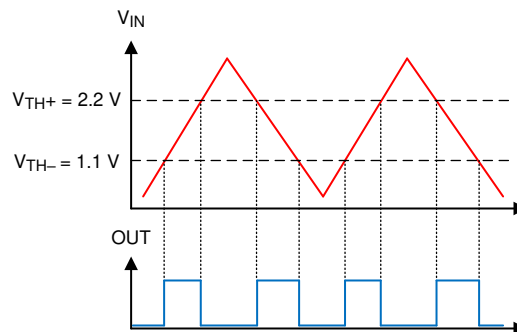
Configure the circuit as shown in [Figure 7-7](#). Connect  $V+$  to a 3.3V power supply and  $V_{EE}$  to ground. Make  $R_1$ ,  $R_2$  and  $R_3$  each  $10\text{M}\Omega$  resistors. These three resistors are used to create the positive and negative thresholds for the window comparator ( $V_{TH+}$  and  $V_{TH-}$ ).

With each resistor being equal,  $V_{TH+}$  is 2.2V and  $V_{TH-}$  is 1.1V. Large resistor values such as  $10\text{M}\Omega$  are used to minimize power consumption. The resistor values may be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and noninverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs will be low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs will be high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in [Figure 7-8](#).

### 7.2.1.3 Application Curve



**Figure 7-8. Window Comparator Results**

For more information, please see Application note SBOA221 "[Window comparator circuit](#)".



### 7.2.2 Undervoltage Detection

Undervoltage detection is frequently required in low-power, always-on systems to alert the downstream device that a battery or supply voltage has drooped below the nominal voltage level. The TLV185x and TLV186x devices have an over-the-rail capability which allows the comparator to monitor high voltages up to 40V on the inputs while operating at lower supply voltages such as 3.3V, as shown in Figure 7-9. The high voltage battery  $V_{BAT}$  is divided down to be compared against a reference voltage, which can be set by a shunt regulator such as the TL431. When the voltage on the non-inverting input drops below the reference voltage, then the output of the comparator will toggle and send an alert signal to a MCU.

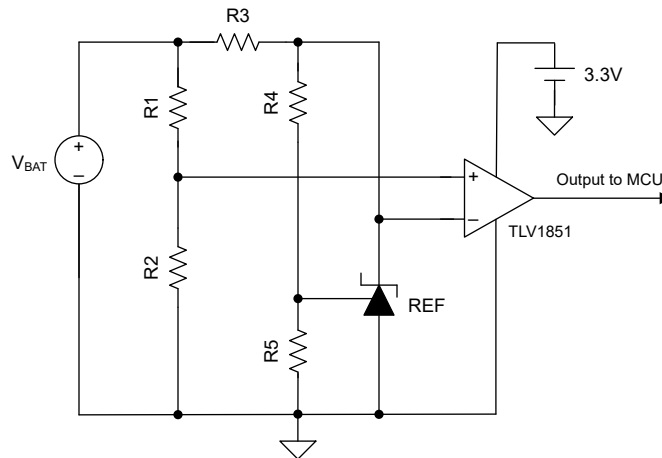


Figure 7-9. Undervoltage Detection

### 7.2.3 Reverse Battery and Overvoltage Protection Scheme

In battery powered applications, it is essential to have safeguards in place to protect the internal electronics against reverse battery connections. Figure 7-10 shows a protection scheme using TLV1851 to prevent damage to the overall system in the events of both improper battery installation and overvoltage conditions. Under either of these instances, Q1 and Q2 will open, thus protecting the system from ever seeing reverse battery or overvoltage conditions.

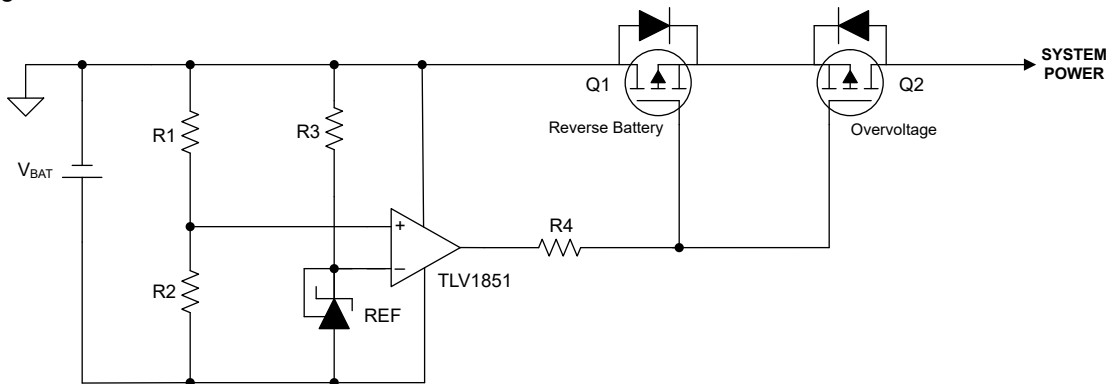


Figure 7-10. Reverse Battery and Overvoltage Protection Scheme

## 7.3 Power Supply Recommendations

Due to the fast output edges, it is critical to have bypass capacitors on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1 $\mu$ F ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents will be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device may be powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output will now swing "low" ( $V_{OL}$ ) to (V-) potential and not GND.

## 7.4 Layout

### 7.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and should be treated as high speed logic devices. The bypass capacitor should be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100ohms) resistor may also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations should be used when routing long distances.

### 7.4.2 Layout Example

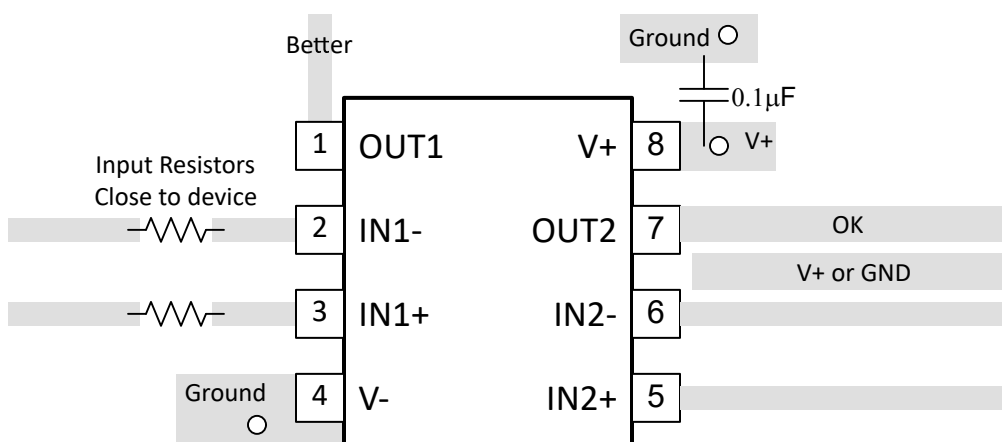


Figure 7-11. Dual Layout Example

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

[Analog Engineers Circuit Cookbook: Amplifiers \(See Comparators section\) - SLYY137](#)

[Precision Design, Comparator with Hysteresis Reference Design— TIDU020](#)

[Window comparator circuit - SBOA221](#)

[Reference Design, Window Comparator Reference Design— TIPD178](#)

[Comparator with and without hysteresis circuit - SBOA219](#)

[Inverting comparator with hysteresis circuit - SNOA997](#)

[Non-Inverting Comparator With Hysteresis Circuit - SBOA313](#)

[A Quad of Independently Func Comparators - SNOA654](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2023) to Revision B (September 2024)	Page
• Added dual and quad channel parts.....	1

Changes from Revision * (December 2022) to Revision A (January 2023)	Page
• Production Data Release of the TLV1851.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV1851DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1851
TLV1851DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1851
<a href="#">TLV1852DGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38OS
TLV1852DGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38OS
<a href="#">TLV1854PWR</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1854
TLV1854PWR.A	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1854
<a href="#">TLV1861DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1861
TLV1861DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1861
<a href="#">TLV1862DGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38PS
TLV1862DGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	38PS
<a href="#">TLV1864PWR</a>	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1864
TLV1864PWR.A	Active	Production	TSSOP (PW)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1864

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF TLV1851, TLV1861 :**

- Automotive : [TLV1851-Q1](#), [TLV1861-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1851DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1851DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1852DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1854PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV1861DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1861DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1862DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV1864PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1851DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1851DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1852DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1854PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TLV1861DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1861DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV1862DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1864PWR	TSSOP	PW	14	3000	353.0	353.0	32.0



PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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